ToroidMeeting-August-23-06

Toroid Electronics Meeting Minutes

August 23, 2006

Analog Electronics Design

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Attendees:

John Dusatko	Bob Simmmons	Michael Cecere
Steve Smith	Tim Montagne	

Agenda:

1. Schematics ready for layout
2. Next up: software development, CPLD code, hardware.

Presentation Materials:

PPT for meeting, August 23, 2006, M. Cecere

Schematics, Netlist, and BOM for BCM:

BCM Schematics, PDF, Aug 23, M. Cecere
BCM Schematics BOM, EXCEL, Aug 23, M. Cecere
BCM Schematics Netlist, PADSPCB, Aug 23, M. Cecere

Minutes:

- Circuit Discussion
  - Add header for access to Voffset cancellation circuitry
  - Slow down op-amps affter Integrator? maybe after board made
  - remove termination of EVR into CPLD, add some series resistance.
  - same for 119MHz into CPLD
  - check with Evgeny on EEIP issues for box layout
  - consider adding pi filter network between AC/DC PS and PCB
  - check PS current requirements
  - drawing numbers on front of box...

- Toroid Manufacture Update (Tim Montagne)
  - 3 braze failures so far
  - will try new process, fire ceramic with no metal to create eutectic braze alloy
  - expect to come out of furnace next monday
  - will due pull-test to check durability, coat
    - if fails, assemble for a electrical/mechanical test and deliver to CPE
    - step back and do traditional metallization process

Action Items:

1. **M. Cecere:** Adjust circuit as described above and put on v: drive, pdf's
2. **M. Cecere:** Deliver netlist to Tung

3. **M. Cecere:** See Jennifer about parts procurement
4. **M. Cecere:** Start Software Development!
5. **M. Cecere:** Continue overseeing box and cable designs