Cavity Testing

Programming FPGA

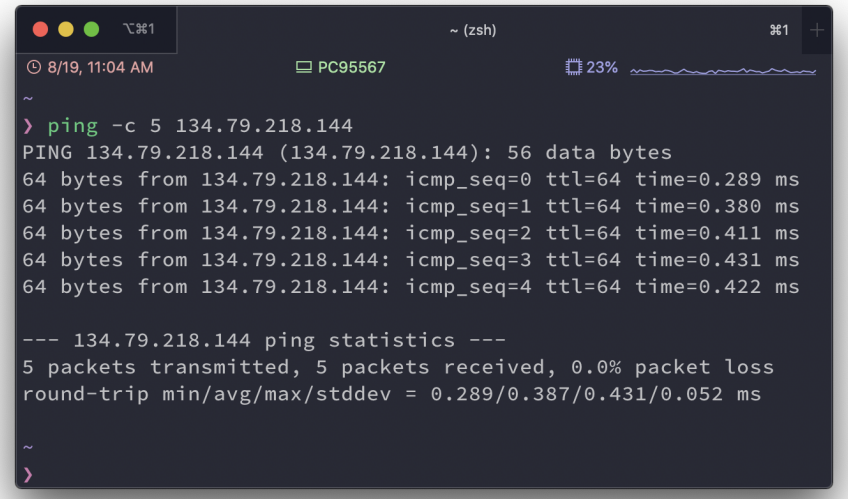
1. Before programming the FPGA check the to see if H2 has jumpers connecting pin 1 to 2 and 5 to 6.
2. Set both of dip switches to the 'F' position
3. Using Xilinx Impact program the FPGA with the attached MCS file. Xilinx Impact Document Github Link
4. Programming the FPGA should take about 5 minutes each.
5. Once complete power down the chassis and remove the Xilinx Platform Cable

Test points

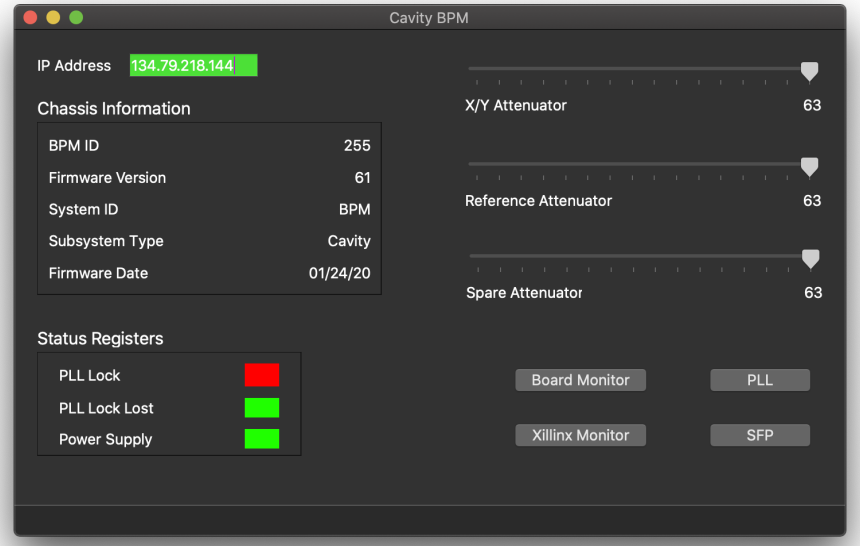
1. Using the Cavity BPM Excel file from the Cavity BPM Chassis Tracker
2. Add a new line for each new chassis
3. Verify the voltage at each test point

Connecting to The Chassis

1. Change the IP Settings to ping the chassis directly
    - Follow the guide from Hello Tech
    - Set the subnet to 255.255.0.0
    - Set the IP Address to 134.79.218.0
2. Open a command prompt and run the following command
    - `ping -c 5 134.79.218.144`
    - This should have responses in ms if the chassis is responding



3. To run the python GUI
    - While in command prompt go to the folder
    - `V:\groups\CD\disco\Cavity BPM GUI\`
    - Run the python application with `python3 main.py`
        - This requires PyQt5 and numpy to be installed
        - `python3 -m pip install -U PyQt5 numpy`
4. - From here verify that the following information is correct
    - IP Address: 134.79.218
    - Firmware Date: 01/24/20
    - Firmware Version: 61


Cavity BPM
IP Address
134.79.218.144
Chassis Information
BPM ID
255
Firmware Version
61
System ID
BPM
Subsystem Type
Cavity
Firmware Date
01/24/20
Status Registers
PLL Lock
PLL Lock Lost
Power Supply
X/Y Attenuator
63
Reference Attenuator
63
Spare Attenuator
63
Board Monitor
PLL
Xillinx Monitor
SFP