L0M17 Half-Module

20190419

L0M17 Half-Module with pinholes pulled

High Voltage Test

(V) (uA)

V:D/I:D

50 0.36

100 0.59

200 0.95

300 1.69

340 3.80

350 5.38

Low Voltage Test

(V) (A)

V:D/I:D

Pre-Config

AVDD; 2.50 0.106

DVDD: 2.50 0.239

V125: 1.25 0.000

Post-Config

AVDD: 2.50 0.304

DVDD: 2.50 0.245

V125: 1.25 0.226

Bad Channel Table

Sector B Sector A

pCH | apvCH | 128+apvCH | 2*128-apvCH-1| 128-apvCH-1

APV0

0 | 0 | 128 | 255 | 127

30 | 30 | 158 | 225 | 97

49 | 49 | 177 | 206 | 78

APV1

165 | 37 | 165 | 218 | 90

204 | 76 | 204 | 179 | 51

APV2

258 | 2 | 130 | 253 | 125

337 | 81 | 209 | 174 | 46

338 | 82 | 210 | 173 | 45

344 | 88 | 216 | 167 | 39

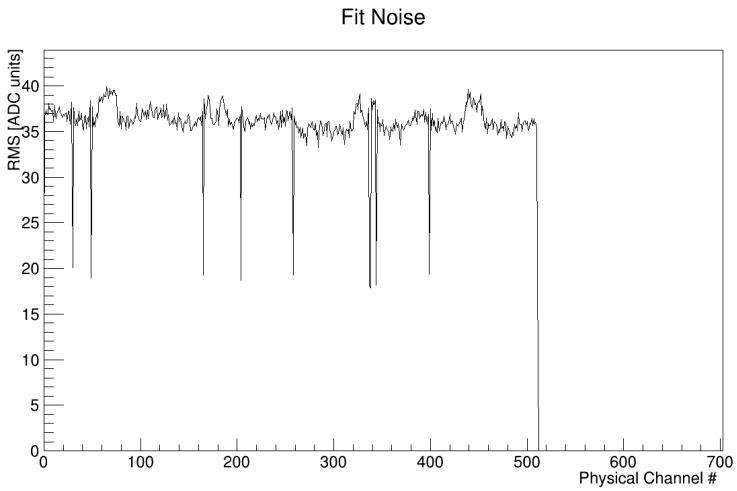
APV3

399 | 15 | 143 | 240 | 112

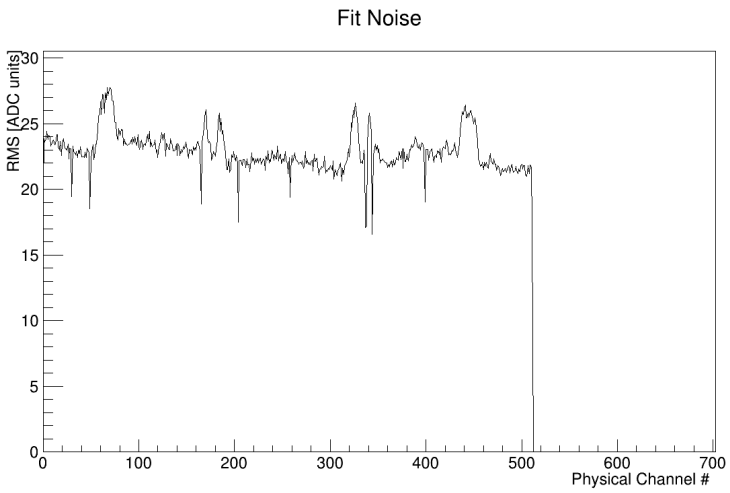
511 | 127 | 255 | 128 | 0

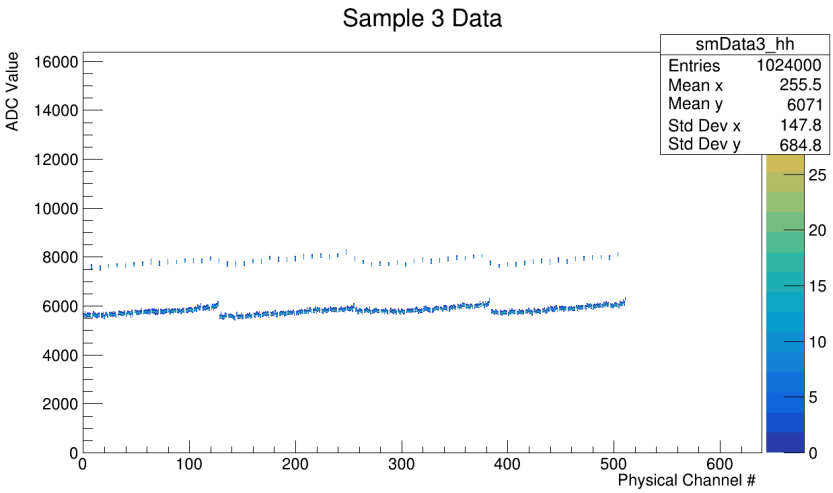
Nlow: 11

0V Bias:



50V Bias:





Tests after being put into Module 2 Axial:

High Voltage Test

(V) (uA)

V:D/I:D

50 0.28

100 0.44

150 0.57

200 0.69

250 0.90

300 1.20

350 1.72

400 2.55

420 3.02

Beyond here it begins to condition