L0M19 Half-Module

L0M19 half-module pretest, pinholes removed

High Voltage Test

(V) (uA)

V:D/I:D

10 0.27

50 0.39

100 0.46

200 0.81

250 1.03

300 3.47

400 12.00

430 13.97

Low Voltage Test

(V) (A)

V:D/I:D

Pre-Config

AVDD: 2.50 0.106

DVDD: 2.50 0.239

V125: 1.25 0.000

Post-Config

AVDD: 2.50 0.265

DVDD: 2.50 0.244

V125: 1.25 0.230

Bad Channel Table

Sector B Sector A

pCH | apvCH | 128+apvCH | 2*128-apvCH-1| 128-apvCH-1

APV0

0 | 0 | 128 | 255 | 127

118 | 118 | 246 | 137 | 9

APV1

204 | 76 | 204 | 179 | 51

APV2

302 | 46 | 174 | 209 | 81

305 | 49 | 177 | 206 | 78

308 | 52 | 180 | 203 | 75

340 | 84 | 212 | 171 | 43

352 | 96 | 224 | 159 | 31

APV3

406 | 22 | 150 | 233 | 105

462 | 78 | 206 | 177 | 49

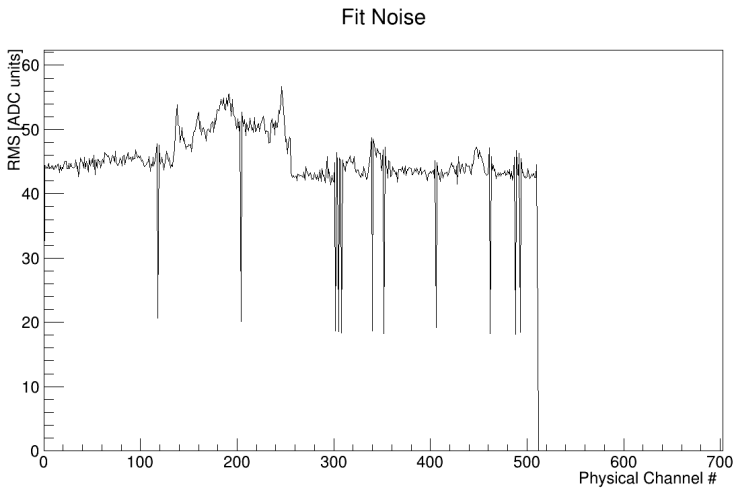
488 | 104 | 232 | 151 | 23

493 | 109 | 237 | 146 | 18

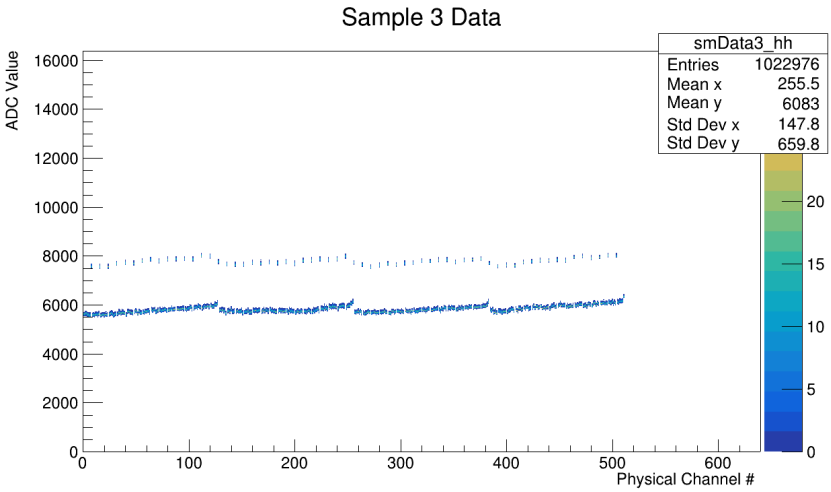
511 | 127 | 255 | 128 | 0

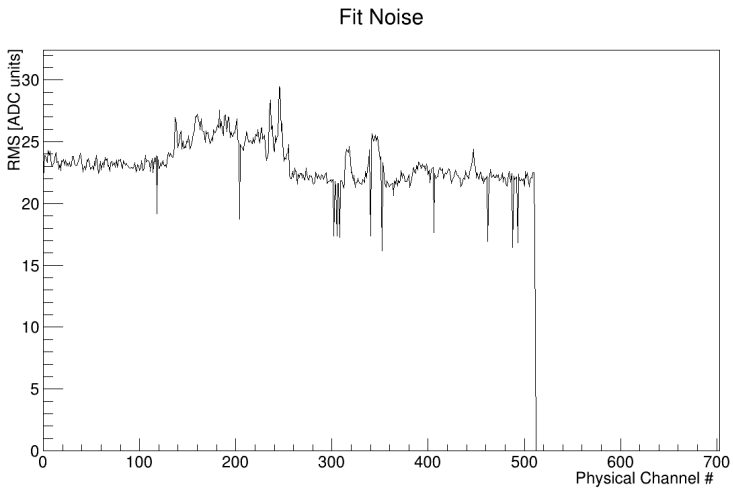
Nlow: 13

Baseline Configuration 0V Bias:



50V Bias:


Sample 3 Data
smData3_hh
Entries 1022976
Mean x 255.5
Mean y 6083
Std Dev x 147.8
Std Dev y 659.8
ADC Value
Physical Channel #


Fit Noise
RMS [ADC units]
Physical Channel #