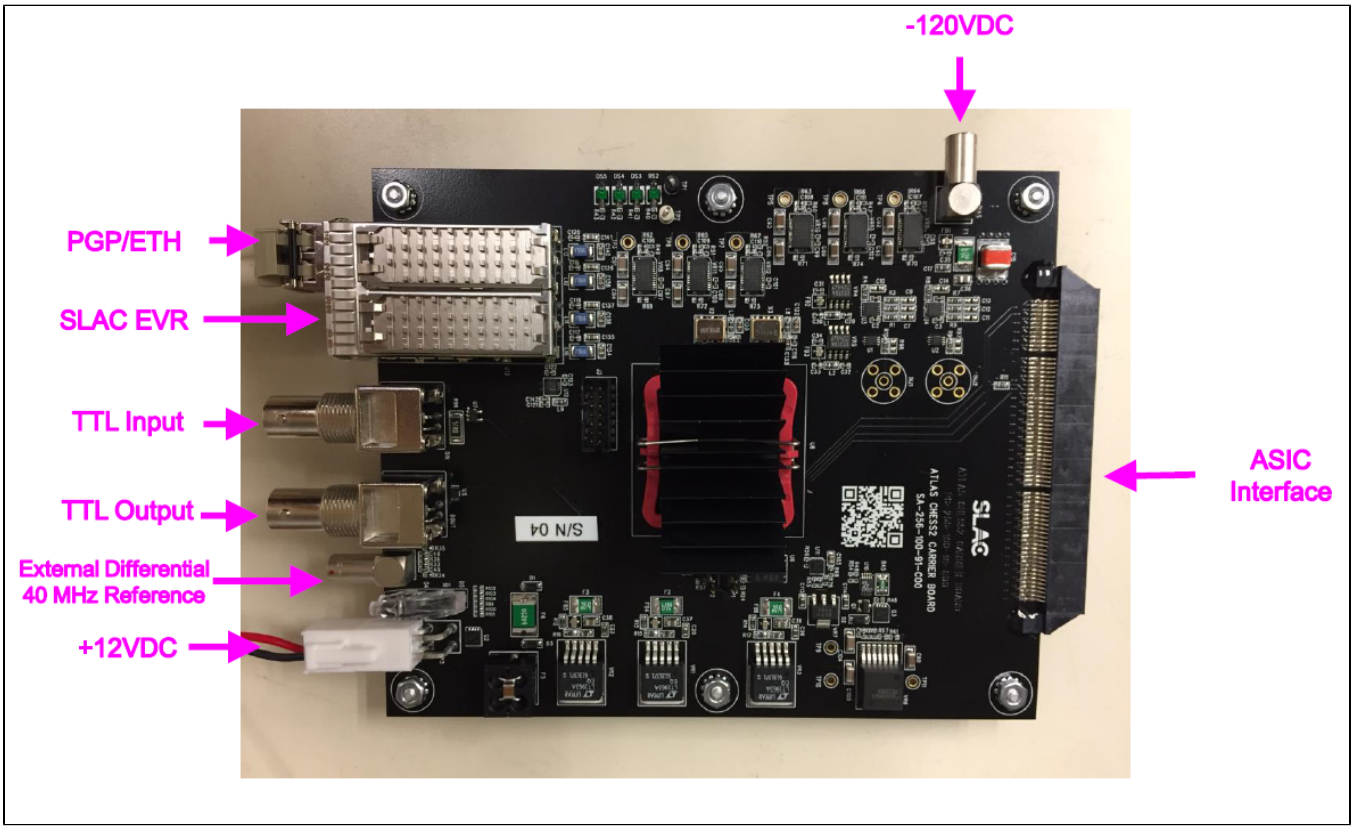
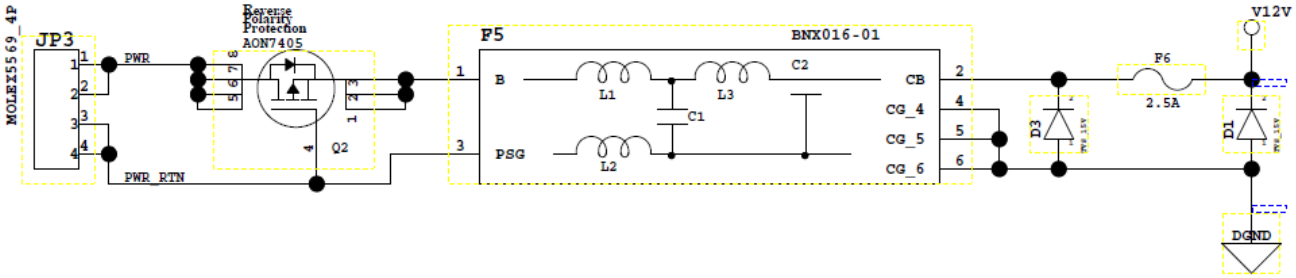
ATLAS: CHESS2: How to cable up the development board hardware

Carrier Board External Interfaces



+12VDC Power (Required)

- When the daugther board is plugged in, the total power draw is about 10W (+12VDC @ 0.8A)
  - Carrier Board is ~5W
  - Digital Daughter board is ~5W
- **To prevent the boards from overheating**, we require cool air to be blown on the carrier/daughter card
  - Using a thermal electric cool on the ASIC would be an acceptable thermal management solution as well
- The image below is the carrier board's input power circuit :
  - The mating connector to the carrier board's power connector is "MOLEX 39-01-3042" and the pinout is:
    - PIN1 = PWR (+12VDC)
    - PIN2 = PWR (+12VDC)
    - PIN3 = PWR_RTN (GND)
    - PIN4 = PWR_RTN (GND)



PGP/ETH (Required)

- This SFP interface is the PGP or ETH (depending on which firmware is loaded)
- When ETH firmware is load:
    - Ethernet PHY is 1000BASE-SX

ASIC (Required)

- This is the interface that the digital daughter board plugs into

-120V Bias (Optional)

- Single ended LEMO connector
- Drives the ASIC's high voltage bias
- Only required if you are doing laser testing or beam testing

SLAC EVR (Optional)

- Used for interfacing to the SLAC's linac timing system

TTL Input (Optional)

- Used for external triggering
- +5V TTL logic levels
- BNC Connector

TTL Output (Optional)

- Currently usued in the firmware
- +5V TTL logic levels
- BNC Connector

External Differential 40 MHz Reference (Optional)

- Used for external 40 MHz timing reference
- Differential LEMO

Contact

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