ATLAS: CHESS2: Carrier/Daughter Board Requirements

Daughter Board Requirements:

- Board must fit into a 7.8cm (3.071") wide x 4.6cm (1.811") high x 10cm (3.937") deep cavity
  - Drawing of the cavity
  - No cabling requiring
- Mounting hole requirements:
  - 4x non-plated mounting holes
    - 2x in-line ASIC
      - Herve will provide the dimensions for TCT
    - 2x in-line with mating connector (to stabilize)
- Board Material:
  - FR4
  - same as CHESS1
- Board Thickness:
  - standard 1.6mm thickness
  - same as CHESS1
- Allow board components:
  - ASIC, capacitors (wire bond only) , 100 ohm LVDS termination resistors (wire bond only)
    - **(Action Item for JJJ to get part number of wire bonded discretes)**
- Not allow board components:
  - Non-LVDS termination resistors, plastic/metal connectors
- HV through the connector
- ASIC-to-board epoxy material:
  - Arldite
- Wire bonds Material:
  - aluminum wedge wiring bonding
- ASIC Thermal Management Plan:
  - Needs to be able to add cold plate
  - Need to assign a mech. eng. to design the cold plate **(Action Item for Su Dong)**
- Board Connector:
  - Hard gold finger edge connector
- Able to test the daughter board before and after radiation without unsoldering/soldering any component:
  - Achieved via the edge connector
- Only implement the high speed digital signals
  - Off load the test structure testing to the CHESS1 carrier board
    - No right side wiring bonding pads
  - Requires a different CHESS2 daughter card design for CHESS1 board
- Place the chip 1mm from the edge of the board
- Able to support a hole underneath the ASIC by machining out the PCB board
- PCB plating:
  - Connectors are hard gold
  - Wire bonding pads soft gold
- Add test points for the digital test structure signals

Carrier Board Requirements:

- Support full 3+1, Pair only, 1+Test chip configurations (digital only)
- Socketed connector for an daughter card with an edge connector
  - High speed digital, SACI control, LV power, and HV control to/from the daughter board
- Flexible timing control for multi-chip operation
- Interface to backend readout with just one SFP fiber link should be the most flexible generic form for evolution
  - Primarily PGP
  - Capable of supporting 1 GigE (1000BASE-SX)
- Generic control/data interface for compatibility with main backend readout schemes of RCE and NEXYS video
  - RCE via SFP
  - NEXY via SFP