Silicon Sensor Testing

The silicon tracking detectors in the heart of ATLAS are facing the increasing challenge of higher luminosity accompanied by higher pileup, and the effect of radiation damage will also become more pronounced in the coming years. Better understanding of the radiation damage effects will enable the control over data quality for the present pixel detector. The High Luminosity LHC upgrade in 2023 further demands a complete replacement of the Inner Detector of ATLAS with a new all silicon design (ITk) that need to be more granular, more radiation hard and with higher bandwidth. Several projects along this theme will be available this summer:

1) Test beam for irradiated pixel sensor characterization

Heavily irradiated pixel sensor sensors designed for the recently installed pixel Insertable B-Layer (IBL) will be placed in the SLAC End Station A Test Beam (ESTB) in special configurations to collect data to best characterize the detailed performance of the IBL sensors and cross check the radiation damage model used in the simulation.

2) Test beam for ITk pixel sensors

Test beam activities at SLAC ESTB for prototype ITk pixel sensors. This includes the planar sensors bump-bonded to the IBL readout chip FE-I4 which will be a major step forward to qualify a new US vendor RTI for bump-bonding. Prototype ITk pixel modules using prototype RD53 65nm readout chip with similar logic design as FE-I4 modules will be another expected flavor of test subjects.

3) CMOS sensor Edge TCT tests

One major new sensor development for ITk is the fully monolithic CMOS sensor development program CHESS with a pixilated strip-like readout as potential alternative sensor technology in place of the conventional silicon strip detectors occupying most of the ITk tracking volume. CHESS1 prototypes with analog pixels are available since 2015 while CHESS2 with the full digital readout is to be submitted in May and with wafers back in August. The Edge TCT technique by shining laser edge on to the sensor scanning response at different depth has been a powerful characterization tool in the lab.

4) CMOS sensor test beam

The strip-like CMOS CHESS2 sensors are expected to be mounted to carrier boards to go in to test beam at ESTB. Readout implementation for this completely new type of detector is expected to require significant work.

There are many common elements between the projects, such as ESTB operation and RCE readout system for calibration and DAQ, and test beam data analyses. Both the test beam and Edge TCT work will offer extensive hands on experimental training.

Literature and documentations:

- Silicon Detector Simulation with TCAD (CERN seminar by Mathieu Benoit)
- Monolithic CMOS ASIC Development (Talk presented by Pietro Caragiulo at Trento workshop Feb/2016)
- TCT technique for sensor tests (Talk by Vladimir Cindro at Vertex-2015)
- SLAC ESTB ATLAS portal

- RCE readout test stand Twiki at CERN

Contact: Su Dong