

10.4.2013 Meeting

Webex meeting for those not at SLAC: <https://confluence.slac.stanford.edu/display/hpsg/Webex+connection+details>

Agenda

- News from FE board or hybrid layout?
- Power estimates for DAQ - Ben
- Initial results from NLCTA test beam
- AOB

Minutes

Ryan says that hybrid will go into layout on Monday and probably be ready by end of next week. FE board will start layout after that.

Ben reported that FE board firmware is about 90% done but nothing tested of course.

Ben is working on a power consumption estimate for the FE board. The digital seems to be about 4W and is a pretty solid number. He wasn't ready with the analog power but expected it to be close to 10W. A large part of the power comes from 12 linear regulators that dissipate 0.5W each when stepping down voltage.

After we have a more complete picture we might want to look into replacements that are less power hungry.

We should do a nominal and maximum estimate. Nominal based on test run measurements and the maximum based on estimates from Omar's studies of the 35ns shaping time operation.

The test run measurements of hybrid currents where:

	Low [mA]	High [mA]
DVD D	230	260
AVDD	380	420
V125	260	320

Pelle and Sho showed initial results from the NLCTA beam test. All info can be found on the confluence page: [NLCTA Test Beam](#)

The "step" like feature, identical, across each apv showed up at 10pC and 350V.

It increases with higher voltage and many individual short like channels show up after the run at 100pC.

The fact that the unbonded apv chip had no effect and that the bias voltage induces a threshold in the effect (at ~208V) indicates that there is a combination of sensor and chip damage.

One hypothesis was that perhaps we did create a conductive channel between the implant and strip on many channels which causes the apv to see a larger leakage current which it has trouble draining and thus effects the internal workings causing it to show this step like behavior.

From a coarse measurement there was no indication of a shift in the baseline that was ~50-100ADC.

Similarly there was no large change in leakage current.

Actions:

Pelle will go back and measure more precisely the leakage current.

Sho will look more carefully at the pedestals.

Pelle, Sho and Tim will look into how we can do probing of the sensor to look for pinholes. One issue is that there is encapsulation on the DC probe pads.

Tim mentioned that it is possible to remove the encapsulation and that we have equipment for this in the clean room. We'll look into it next week and make a plan.

Based on these studies we might want to check with Angelo on what his thoughts are and then approach the apv chip designers.