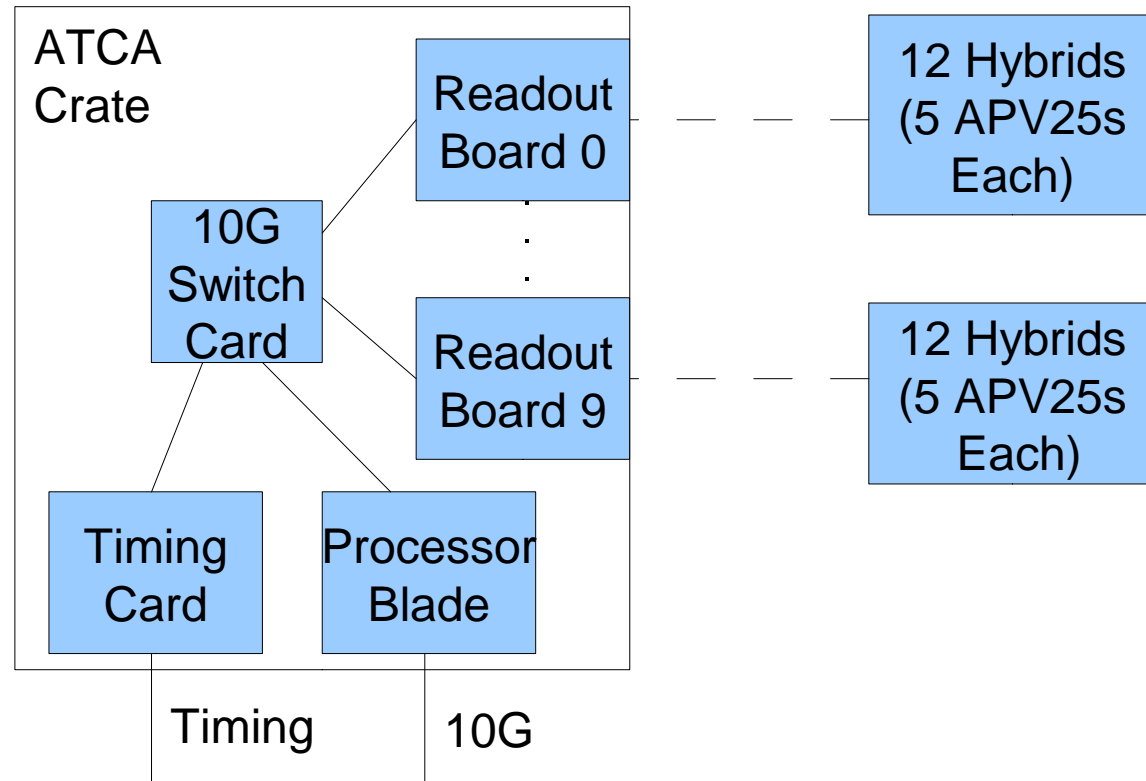# Heavy Photon
Data Acquisition Development
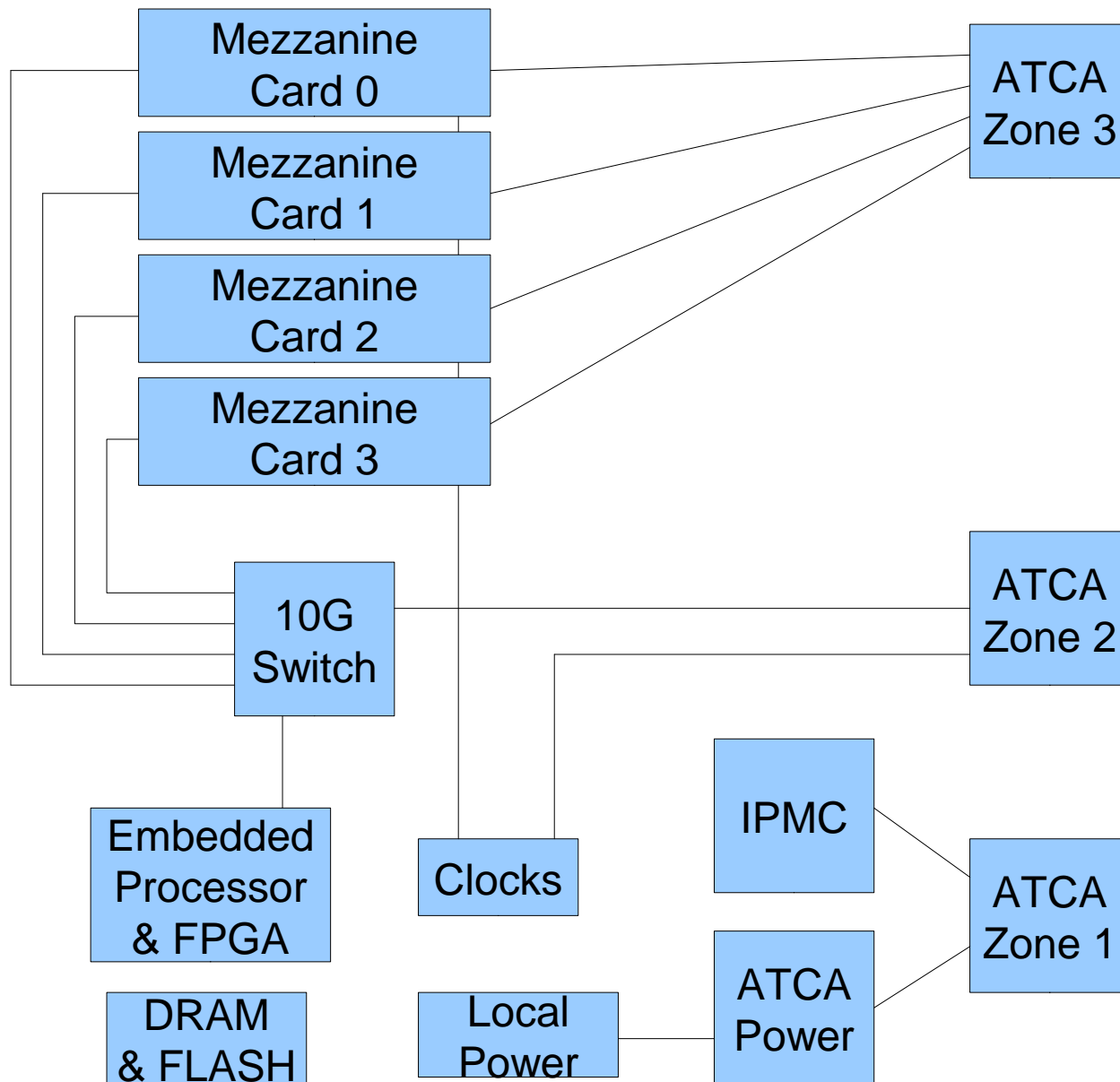
Presented by

Ryan Herbst

Heavy Photon Data Acquisition

- **ATCA based DAQ**
- **10 readout boards interface to 12 hybrids each**
- **Each hybrid supports 5 APV25s**
- **Timing card to receive timing & buffer control information**
- **Multi port 10G switch card**
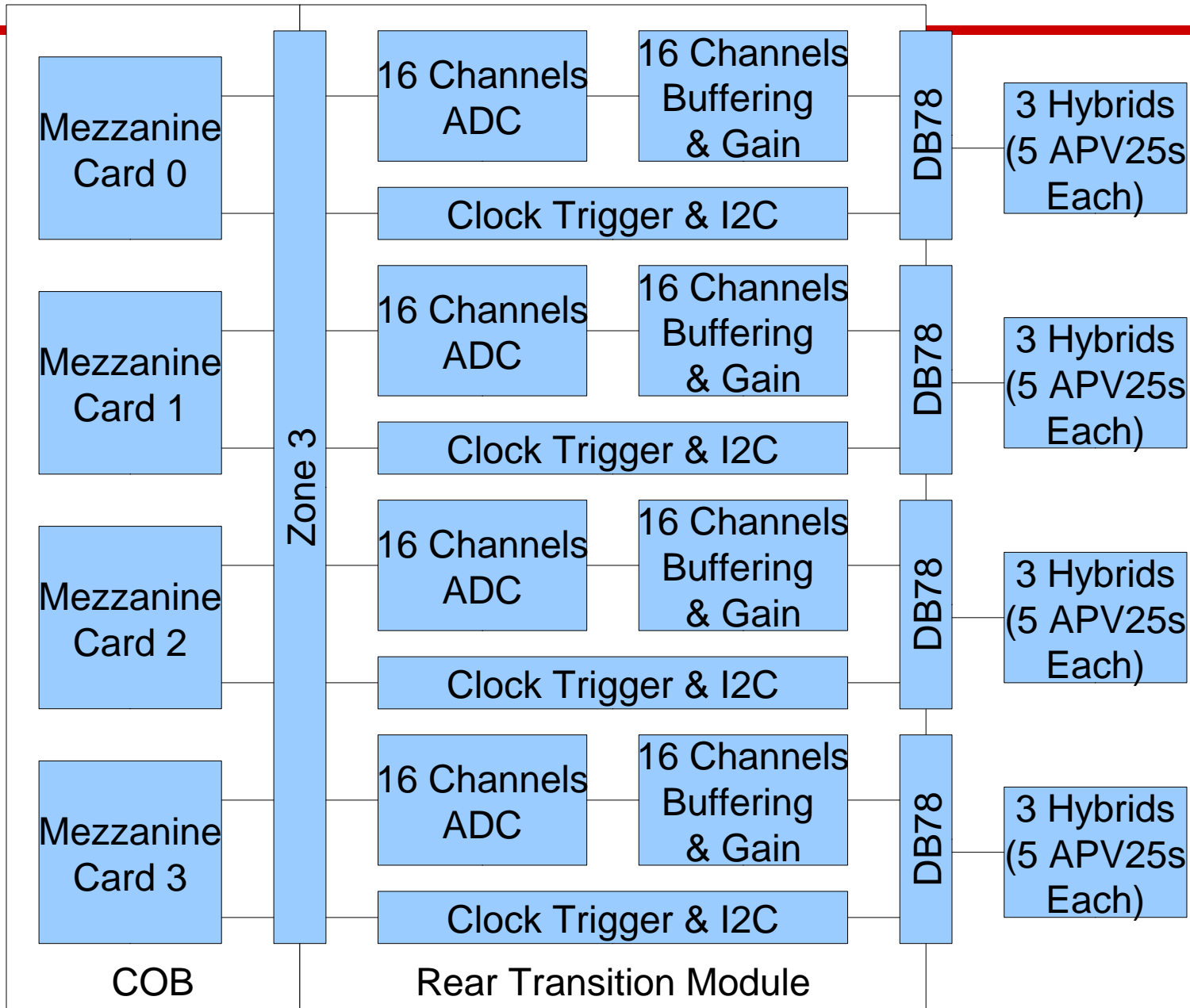- **Linux based processor blade for data collection and distribution**
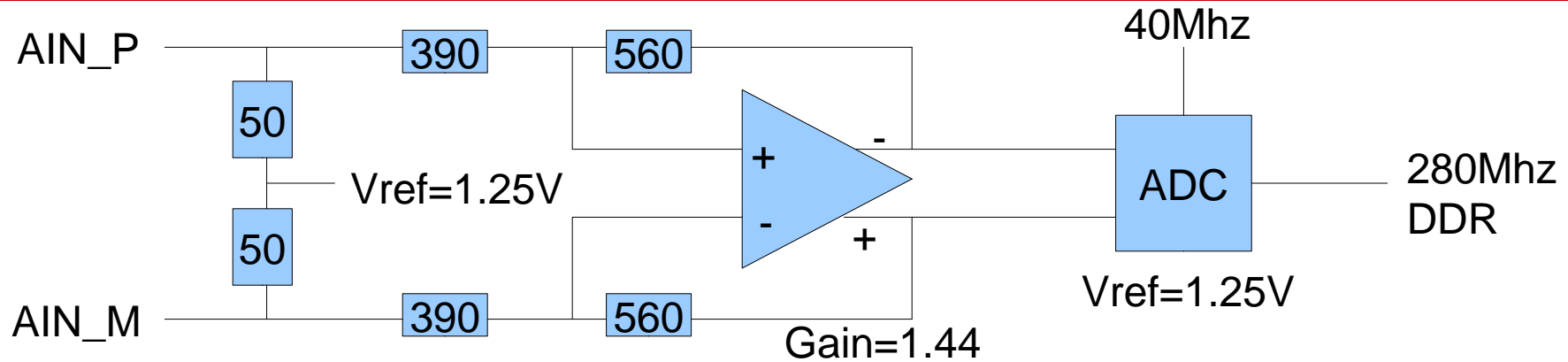
ATCA Carrier On Board (COB)

Carrier On Board (COB)

- Being developed as generic data acquisition platform for multiple projects
  - Primary target is second generation RCE platform
    - ATLAS
    - LSST
  - Fits well into Heavy Photon DAQ proposal
- Supports 4 mezzanine cards
  - 10G Ethernet interface to back plane
  - 28 differential pairs routed to zone 3 connector
  - Generic lines to COB FPGA (timing, management, etc)
  - Timing signals to/from zone 2 connector
  - AMC form factor and IPMC management (TBD)
- On board 24 port Ethernet switch
  - 2 10G interfaces to each mezzanine card
  - 13 10G interfaces to zone 2 back plane connector
    - Dual star compatible
    - Full mesh compatible
- Local FPGA with embedded processor
  - Switch management
  - Board specific firmware
- IPMC & power distribution
- Schematic in progress

Readout Board - Rear Transition Module

COB			Rear Transition Module	

Mezzanine Card 0 — Zone 3 — 16 Channels ADC → 16 Channels Buffering & Gain → DB78 → 3 Hybrids (5 APV25s Each)

Clock Trigger & I2C

Mezzanine Card 1 — 16 Channels ADC → 16 Channels Buffering & Gain → DB78 → 3 Hybrids (5 APV25s Each)

Clock Trigger & I2C

Mezzanine Card 2 — 16 Channels ADC → 16 Channels Buffering & Gain → DB78 → 3 Hybrids (5 APV25s Each)

Clock Trigger & I2C

Mezzanine Card 3 — 16 Channels ADC → 16 Channels Buffering & Gain → DB78 → 3 Hybrids (5 APV25s Each)
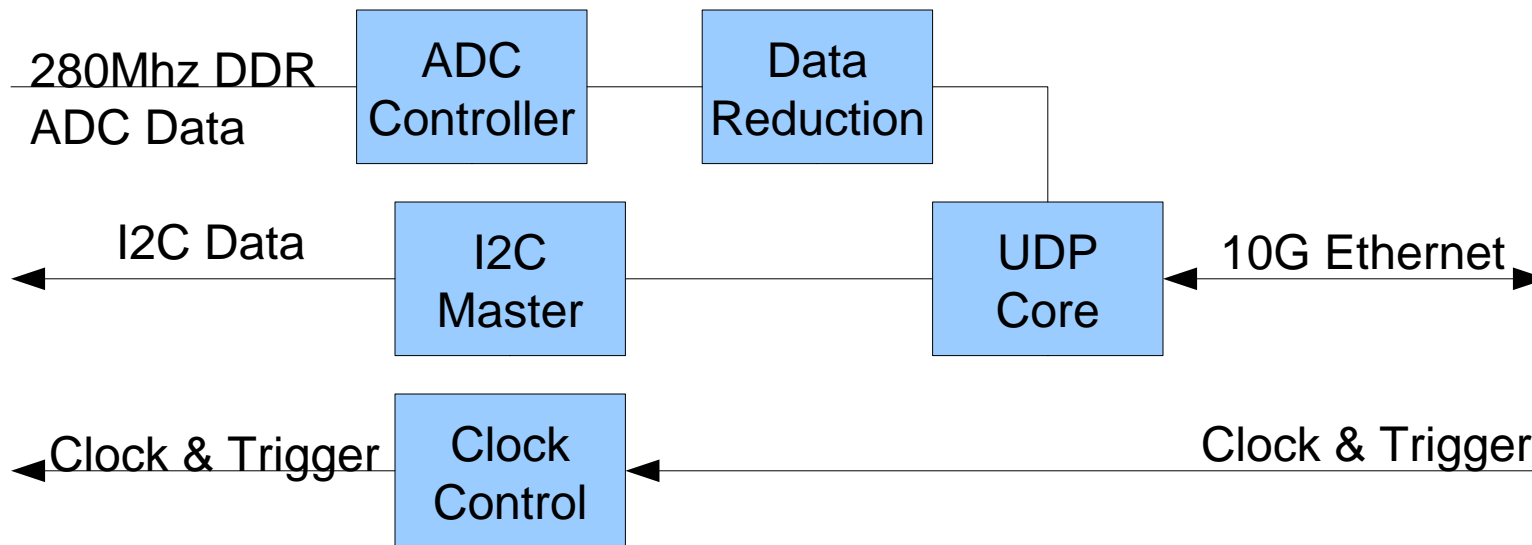
Clock Trigger & I2C

SLAC

Readout Board - Rear Transition Module

- **Hybrids arranged in groups of 3**
  - **15 ADC channels per group**
  - **Each group controlled by single FPGA on COB mezzanine**
  - **Clock, trigger & I2C buffering per group**
- **Signals from 3 hybrids brought in on DB89 connector**
- **Incoming signal centered around 1.25V reference terminated across 100ohms**
  - **Avoid negative supply voltage**
  - **Hybrid to drive centered around 1.25V**
- **Differential buffer with gain of 1.44 (replicated from ARC design)**
- **Differential ADC with 1.25V reference**
  - **One of eight channels**
  - **40Mhz sample clock (supports up to 50Mhz)**
  - **14-bit resolution, 280Mhz DDR data output**
- **Schematic completed, layout in January**

Mezzanine Card

```
280Mhz DDR          ┌──────────┐      ┌──────────┐
ADC Data            │   ADC    │──────│   Data   │
                    │Controller│      │Reduction │
                    └──────────┘      └──────────┘
                                                       │
                    ┌──────────┐      ┌──────────┐
I2C Data     ◄──────│   I2C    │──────│   UDP    │◄──── 10G Ethernet ────►
                    │  Master  │      │   Core   │
                    └──────────┘      └──────────┘
                    ┌──────────┐
Clock & Trigger ◄───│  Clock   │◄──────────────────── Clock & Trigger
                    │ Control  │
                    └──────────┘
```

- **Virtex 5 FPGA on custom mezzanine card**
- **Firmware UDP core for command/response and data transmission to ATCA processor blade**
- **Data reduction performed in firmware**
  - **Simple value over threshold comparison**
  - **5 sample event accepted if any of 5 samples over software defined threshold**
- **I2C master for APV25 register access**
- **Clocks from COB passed down to hybrid boards**
  - **System clocks distributed on back plane**
- **Same board with different firmware used for timing card**
  - **Timing card will used a different RTM with the appropriate connectors**