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LLRF Control Design Specification

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Brief Summary: This specification describes the LLRF control system which will control the phase and amplitude of the klystrons and the beam phase cavities at the 30 Hz commissioning frequency. Plans for the upgrade to 120 Hz are also described. In section 2, the LLRF control system is introduced. Requirements are stated and the system is presented, first as an overview and then in detail. Section 2 describes the phase and amplitude detector, section 3 describes the VME system and section 4 describes the phase and amplitude controller. These 3 sections include the hardware description, software requirements, the algorithms and the software design. Section 5 describes the interfaces between LLRF and other systems. Section 6 discusses related high level applications. The commissioning test plan follows next. Finally, plans are presented.

Keywords: LLRF, EPICS, PAD, PAC, VME

Key WBS#'s: x.x.x

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1 LLRF Controls System

1.1 Requirements

For LCLS, the general RF stability requirements are: 0.1 deg phase and 0.1% amplitude in L0 and L1 for S band. More specifically, the jitter specifications must be held for a period of 2 seconds and are shown in Table 1. Slow drift specifications must be held for periods of up to 2 days. Two days was chosen for this specification to keep the length of an acceptance test to a reasonable time frame and to include diurnal variations. These are listed in Table 2.

Table 1 Jitter specifications:
RMS tolerance budget for <12% rms peak-current jitter (column 3) or <0.1% rms final e− energy jitter (column 4). The tighter tolerance is in BOLD, underlined text and both criteria, |□I/I0| < 12% and |□□E/E0□| < 0.1%, are satisfied with the tighter tolerance applied. All tolerances are rms levels and the voltage and phase tolerances per klystron for L2 and L3 are □Nk larger, assuming uncorrelated errors, where Nk is the number of klystrons per linac.

Parameter	**Symbol**	**$\|\Delta I/I_0\| < 12$ %**	**$\|\langle \Delta E/E_0 \rangle\| < 0.1$ %**	**Unit**
mean L0 rf phase (2 klystrons)	$\varphi 0$	0.10	0.10	S-band deg
mean L1 rf phase (1 klystron)	$\varphi 1$	0.10	0.10	S-band deg
mean LX rf phase (1 klystron)	φx	0.5	0.5	X-band deg
mean L2 rf phase (28 klystrons)	$\varphi 2$	0.07	0.07	S-band deg

mean L3 rf phase (48 klystrons)	$\varphi 3$	0.5	0.15	S-band deg
mean L0 rf voltage (1-2 klystrons)	$\Delta V0/V0$	0.10	0.10	%
mean L1 rf voltage (1 klystron)	$\Delta V1/V1$	0.10	0.10	%
mean LX rf voltage (1 klystron)	$\Delta Vx/Vx$	0.25	0.25	%
mean L2 rf voltage (28 klystrons)	$\Delta V2/V2$	0.10	0.10	%
mean L3 rf voltage (48 klystrons)	$\Delta V3/V3$	0.5	0.08	%
BC1 chicane	$\Delta B1/B1$	0.01	0.01	%
C2 chicane	$\Delta B2/B2$	0.05	0.05	%
Gun timing jitter	Δt_0	0.8	0.8	psec
Initial bunch charge	$\Delta Q/Q_0$	2.0	4.0	%

Table 2 Slow Drift Tolerance Limits
(Top 4 rows for $\Delta\varepsilon/\varepsilon < 5\%$, bottom 4 limited by feedback dynamic range)

Gun-Laser Timing	±2.4*	deg-S
Bunch Charge	±3.2	%
Gun RF Phase	±2.3	deg-S
Gun Relative Voltage	±0.6	%
L0,1,X,2,3 RF Phase (approx.)	±5	deg-S
L0,1,X,2,3 RF Voltage (approx.)	±5	%

(Tolerances are peak values, not rms) **P. Emma, J, Wu**
* for synchronization, this tolerance might be set to ±1 ps (without arrival-time measurement)

1.2 Overview

The LLRF controls system includes of three main types of components: the phase and amplitude detector (PAD), the VME crate as a source of timing triggers and floating point processor and the phase and amplitude controller (PAC). Figure 1 and Figure 2 show the layout of the LLRF control system at sectors 20, 21, 24, 29 and 30. The number of hardware modules (PADs, VMEs and PACs) is shown as well as the klystrons (or other device) that they control. The locations of the modules are not given exactly, but

you can see which are in the RF hut and which are out in the gallery, near their respective klystron. Also shown is the subset of modules which are used in fast feedback. Finally, network connectivity and timing triggers can be seen.

The blue lines connecting the devices are for communication. For commissioning, each line represents 2 physical cables: serial console communication and 100baseT ethernet. Since the newest version of the PAD and PAC (in production, but not yet tested) both have an additional Ethernet port, a 2nd ethernet cable will be added. The motivation and plans for the second Ethernet port is described in section 9 Post-commissioning plans. The brown lines between the event receiver, EVR, and the PAD and PAC devices represent the timing triggers.

Final note: in the current design, there are two VME crates: one in the RF Hut at sector 20 (shown on Figure 1) and another in sector 24 in the klystron gallery (shown on Figure 2). Since longitudinal beam-based fast feedback may only run in a single CPU, the VME crate in sector 24 may not be needed. However, it is included for now, as a source of timing triggers.

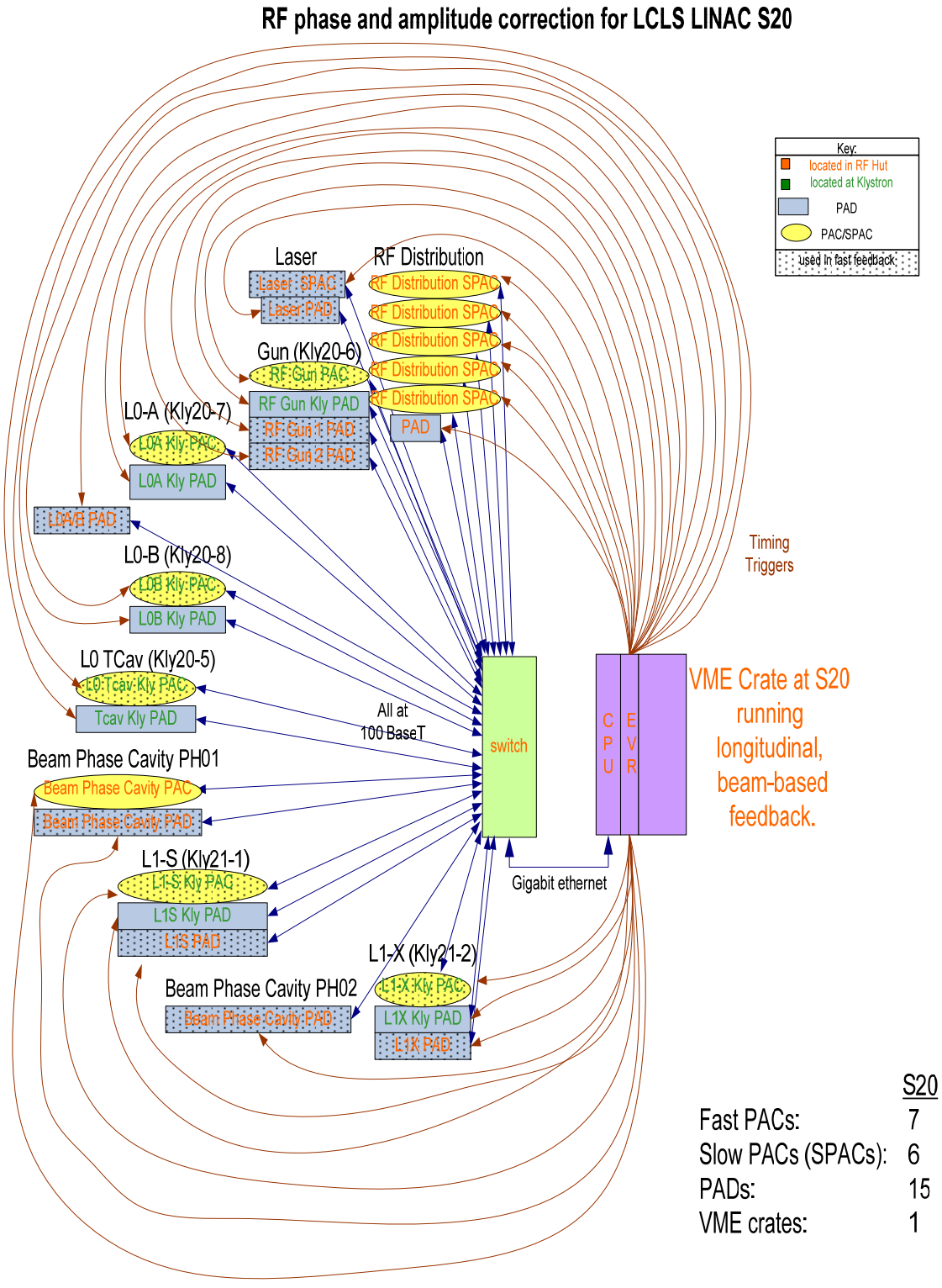

Figure 1 RF phase and amplitude correction for LCLS LINAC S20

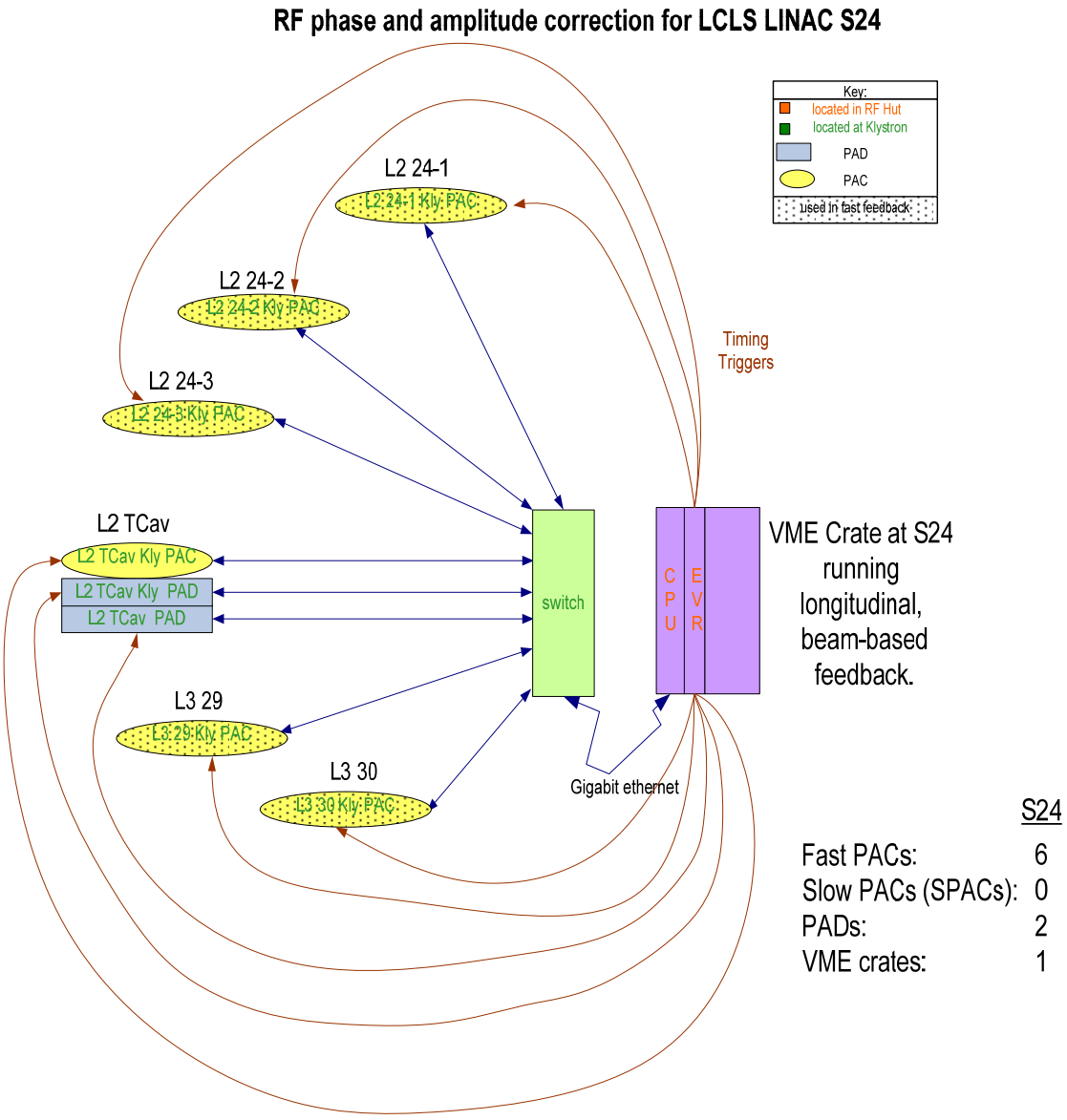

Figure 2 RF phase and amplitude correction for LCLS LINAC S24

1.3 Details

In Figure 3 and Figure 4, the components of the PAD, PAC and VME crate are shown in more detail. The interfaces between the PAC and the modulator and between the PAD and the accelerator structure (or laser) are also shown. Figure 3 shows the LLRF subsystems in L0 and L1, while Figure 4 shows that of L2 and L3. Now the two Ethernet connections are shown: local and global feedback travels on the blue, private Ethernet cable; diagnostic data is sent on the pink, public Ethernet cable. The serial cable is not shown. The network switch is also not shown.

The PAD and PAC modules were designed at SLAC. They both use an Arcturus uCdimm Coldfire 5282 (http://www.arcturusnetworks.com/coldfire5282.shtml). The processor runs the operating system, RTEMS (http://www.rtems.com) and EPICS (http://www.aps.anl.gov/epics).

The VME crate contains a Motorola PowerPC mvme6100 processor and also run RTEMS and EPICS. The VME crate contains an event receiver board (EVR) to receive timing events and data over fiber optic cable for the event generator.

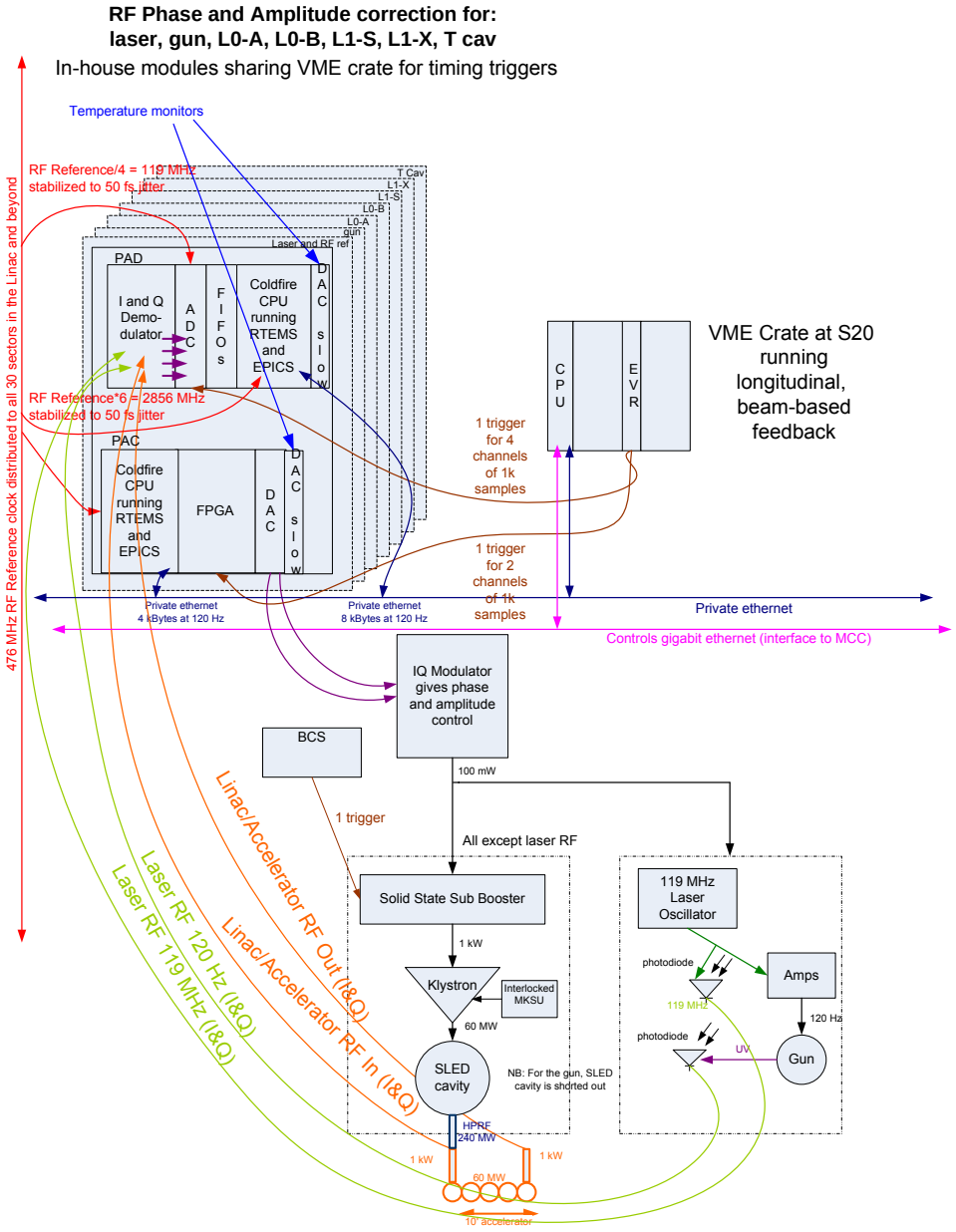

Figure 3 RF Phase and Amplitude correction for laser, gun, L0-A, L0-B, L1-S, L1-X, T cav

RF Phase and Amplitude correction for:
L2, L2 Tcav and L3

In-house modules sharing VME crate for timing triggers

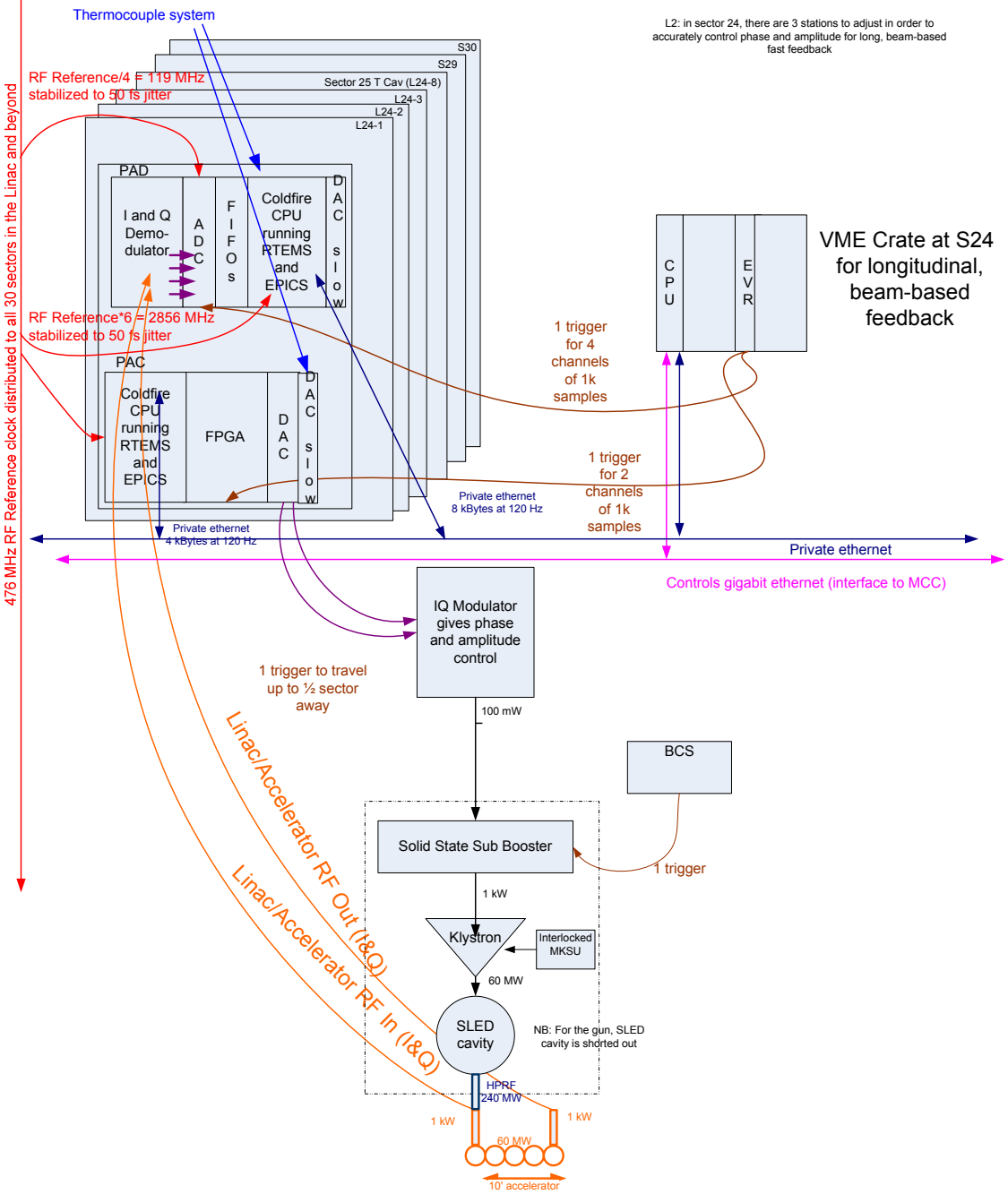

Figure 4 RF Phase and Amplitude correction for L2, L2 TCav and L3

1.4 Details of triggered data acquisition by generic LLRF control subsystem

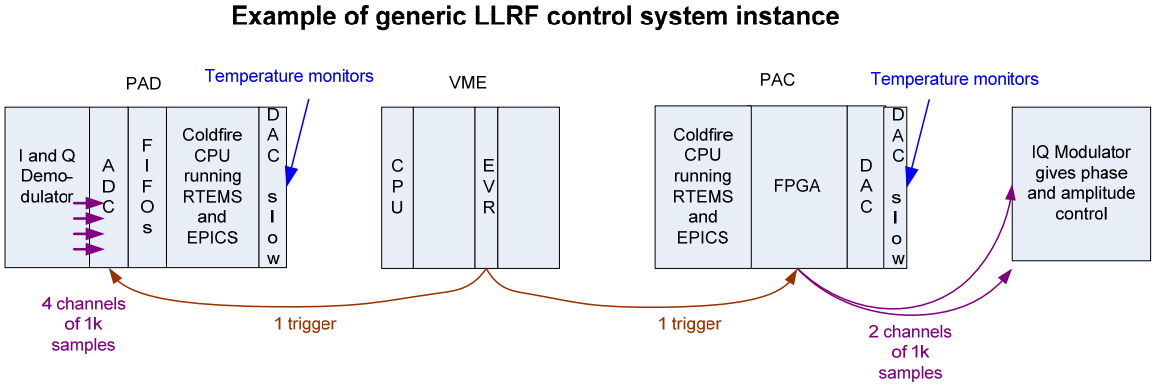

Figure 5 Example of generic LLRF control system instance

Upon receipt of a timing trigger, the PAD's FIFOs are filled. There are 4 channels of interlaced[1] I and Q values filling each of the four 64K sample FIFOs. The following steps are done for each of the 4 channels: A sample of points is read out. The number of points read depends on the operational mode of the PAD. An embedded processor on board the PAD applies a 1-D correction to the raw, interlaced I and Q data and computes independent sums and counts for each I and Q during the read. The resulting average I and Q values are sent over private Ethernet to the VME system.

Upon receipt of these values, the CPU in the VME crate converts I and Q to phase (arctan I/Q) and amplitude (sqrt(I^2 +Q^2)) and applies any correction that has been calculated from either the local feedback loop or from the global beam-based fast feedback. Still in the VME CPU, the corrected values are converted back to I and Q and then sent to the

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[1] Interlaced I and Q data: RF is at 2856 MHz. There is no digitizer that runs this fast. So work at IF (intermediate frequency) of 25.5 MHz and choose to "digitally downmix" (taking the sine and cosine) to the baseband frequency of DC (0 MHz). By choosing an ADC clock of 102 MHz, there are 4 points to each IF cycle. They are π/2 apart, so taking the sine and cosine has the result that:

0 sin(0)=0; Q=0 cos(0)=1; I=I
π/2 sin(π/2)=1; Q=Q cos(π/2)=0; I=0
π sin(π)=0, Q=0 cos(π)=-1; I=-I
3π/2 sin(3 π /2)=-1; Q=-Q cos(3π/2)=0; I=0

Since Q is non-zero only when I is zero, and vice versa, the two variables can be stored in a single array, in alternating positions

What is stored in "scalar" looks like: [1, 1, -1, -1, ...] and maps to the Qs and Is as: [Q1, I2, Q3, I4, ...] where
I1, Q2, I3 and Q4 are all zero. The scalar vector will also hold weighting functions, once determined, which will relate the measurement along the RF pulse to the affect the it has on beam energy gain. What is desired here is to get the best possible estimate of the average phase and amplitude the beam sees as is passes through a structure.

PAC which converts them into a waveform of I and Q and loads them into an FPGA. The sequence of steps described thus far must finish within one operational period (1/30 Hz for commissioning, 1/120 Hz for operations).

Upon receipt of the next timing trigger, the PAC, FPGA held, waveform is sent out.

2 LLRF Phase and Amplitude Detector (PAD)

2.1 PAD Hardware Design

The PAD (Phase and Amplitude Detector) was designed to give high speed analog input data with large dynamic range. The PAD is used to measure phase and amplitude of RF signals as well as klystron beam voltage. The specifications for the RF system of 0.1degree rms phase jitter at S-Band and 0.1% amplitude jitter required a device that can measure to these levels. The main components in the PAD chassis are the Control Board, two RF Modules, and a Slow ADC Board.

2.1.1 Control Board

The digitizer used is the Linear Technologies LTC2208. It was the first 16 bit digitizer chip on the market capable of running at 119MHz, it is specified to run up to 130MHz. Initially a 2 channel board was to be built for the RF system, but the BPM requirements pushed the design to 4 channels.

The PAD clock is run at 102MHz which is 4 times the IF frequency. This makes down conversion to DC multiplication by sines and cosines of multiples of 90 degrees, or ones and zeros. The LTC2208 has a built in dither DAC circuit which varies the location along the ADC transfer function that the signal is digitized at. In measuring low noise RF signals, especially CW signals digitized at a harmonic of the RF, nonlinearities in the ADC transfer function could show up as noise or errors in the measurements which do not average out. By adding in and then digitally subtracting out this dithered signal, the nonlinearities in the ADC transfer function can be averaged out.

For each channel, the 16 bit digitized signal from the LTC2208 is clocked into a 64k sample FIFO. Commercial FIFOs are available which store up to 256k samples in the same package. The data is then read from the FIFO into the Arcturus Coldfire uCDIMM. A CPLD is used to handle triggering, resetting the FIFO, interfacing the Coldfire processor to the 4 FIFOs, and interrupting the Coldfire processor.

A block diagram of this board is shown in Figure 6 and the preproduction version in Figure 7.

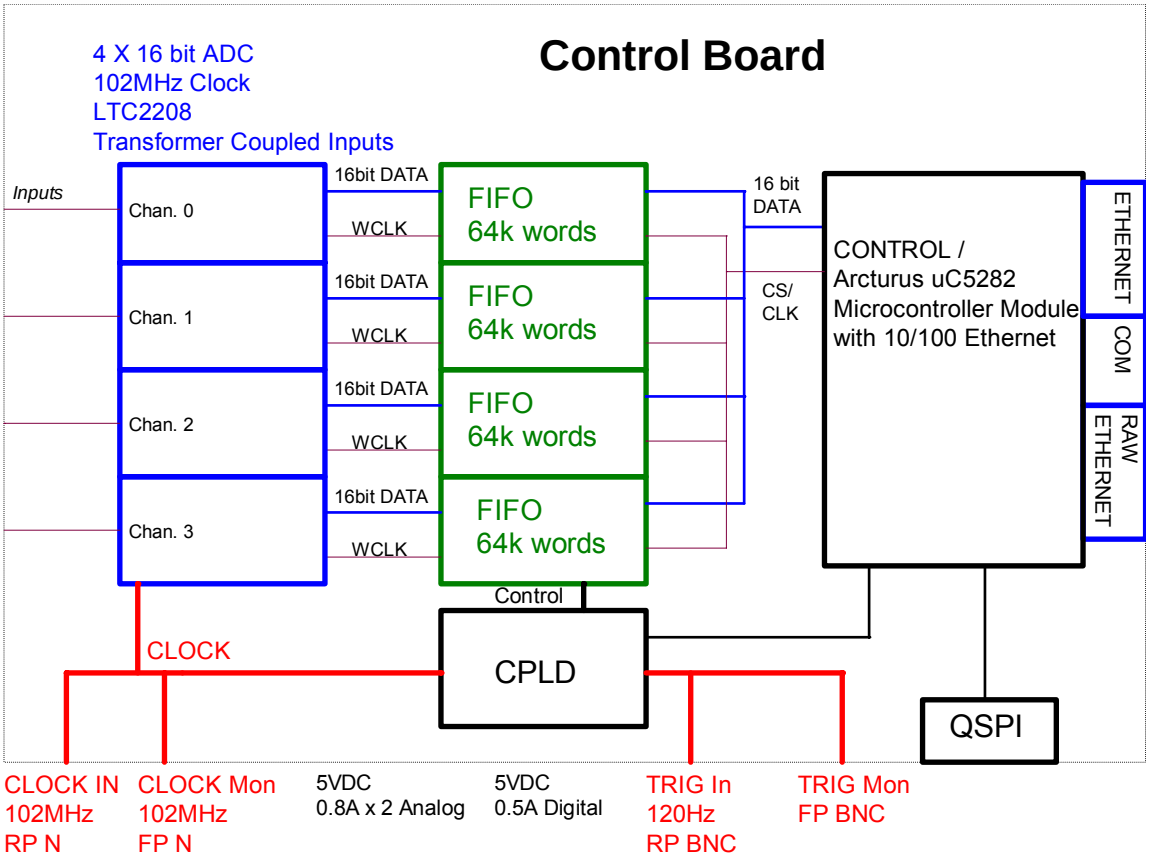


Figure 6 PAD block diagram

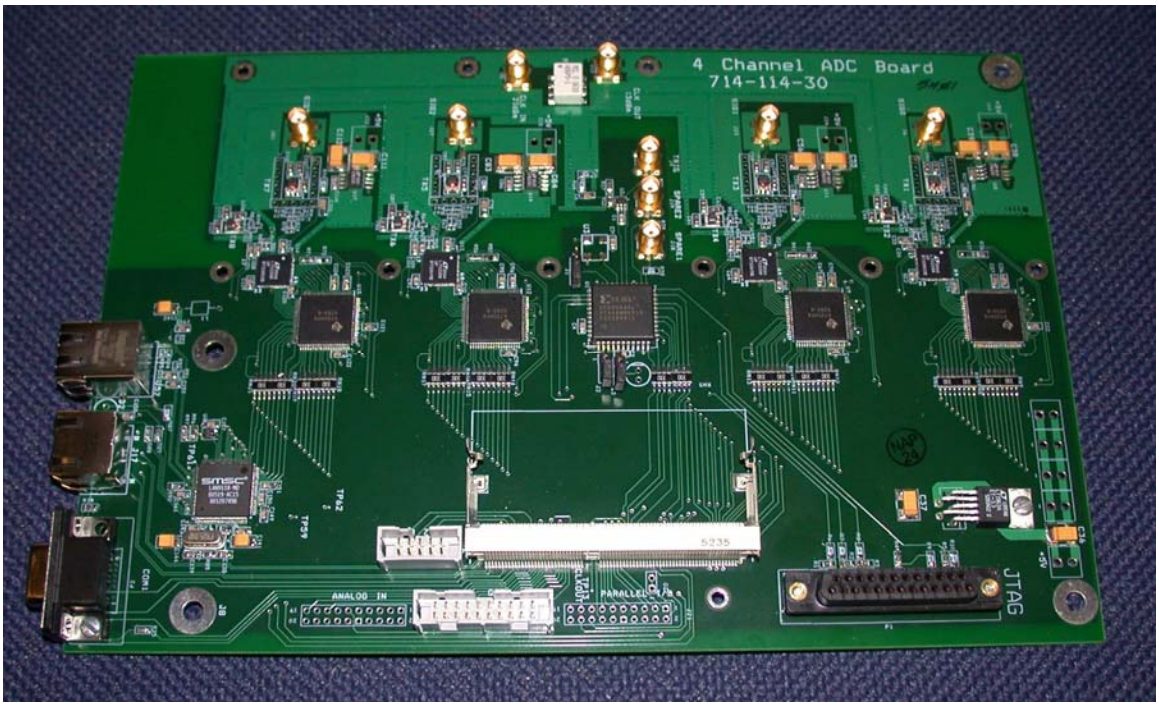


Figure 7 Preproduction PAD Board

2.1.2 Control Board Features

4 Chan - 130MSPS 16 bit ADCs LTC2208 - Data clocked into 64k Sample FIFOs

1 buffered clock input to CPLD
1 buffered trigger input to CPLD
2 unbuffered coax I/O from CPLD
3 digital I/O from CPLD
4 interrupts to uCdimm5282

Ethernet Port RJ45 connector
2nd Ethernet port using SMSC LAN9118 Ethernet Controller
1 COM Port to 9 pin D connector
1 COM Port to header
I2C Port to header
QSPI 4 wire Serial port with 4 chip selects to header
12 bit General Purpose I/O to header
6 10bit mux analog in or 4 digital I/O and 2 digital Outs to header

2.1.3 Control board tests

A low noise 25.5MHz signal was generated by dividing down 2856MHz. The 25.5MHz was split and half quadrupled to 102MHz. The 102MHz was used for the clock input and the 25.5MHz was used as a signal input to the 4 channel ADC board. The power levels for the 102MHz was +20dBm and +3.6dBm for the 25.5MHz. The signal level is about -6dBFS (Full Scale) of the ADC. Four 65k points of data sets were taken with the signal moved from channel to channel. For each data set, the FFT for each channel is shown in Appendix A. Channel to channel cross talk and signal to noise ratios (SNR) are measured for each data set.

The SNR is better than 63dB on all four channels as measured. If scaled to the ADC full scale this would be 69dBFS. It looks like the signal may have noise levels limiting the measurement, since it looks like the noise floor is raised in the signal channel from -79dB to about -70dB. If this is the case the board may be able to achieve 79dBFS SNRs. There is also the possibly that the board layout and/or power supply connections contributes to this raised noise floor. Further study will be done although the board will work as is for the RF system.

Channel to Channel cross talk is in all cases lower than -100dB at 25.5MHz.

2.1.4 RF Module

A block diagram of the RF Module is shown in Figure 8. The RF module has 2 channels. Each channel mixes a signals of 2856MHz with a Local Oscillator (LO) of 2830.5MHz to get an IF frequency of 25.5MHz. The input RF signal power level is about 10W peak. The signal is coupled down by 30dB and then attenuated by a 10dB PAD into the RF port of the mixer. The 2830.5MHz LO signal enters the module at 10dBm. The power is split, attenuated and amplified, to provide LO isolation between the two channels, and

drives the LO port of the mixer at +13dBm. The IF output of the mixer has a high frequency diplexer, which terminate the RF and LO feedthrough and the RF + LO frequency. The 25.5MHz is then amplified and Band pass filtered. A 10dB coupler is used to route the filtered 25.5MHz to a front panel test port and the control/digitizer board.

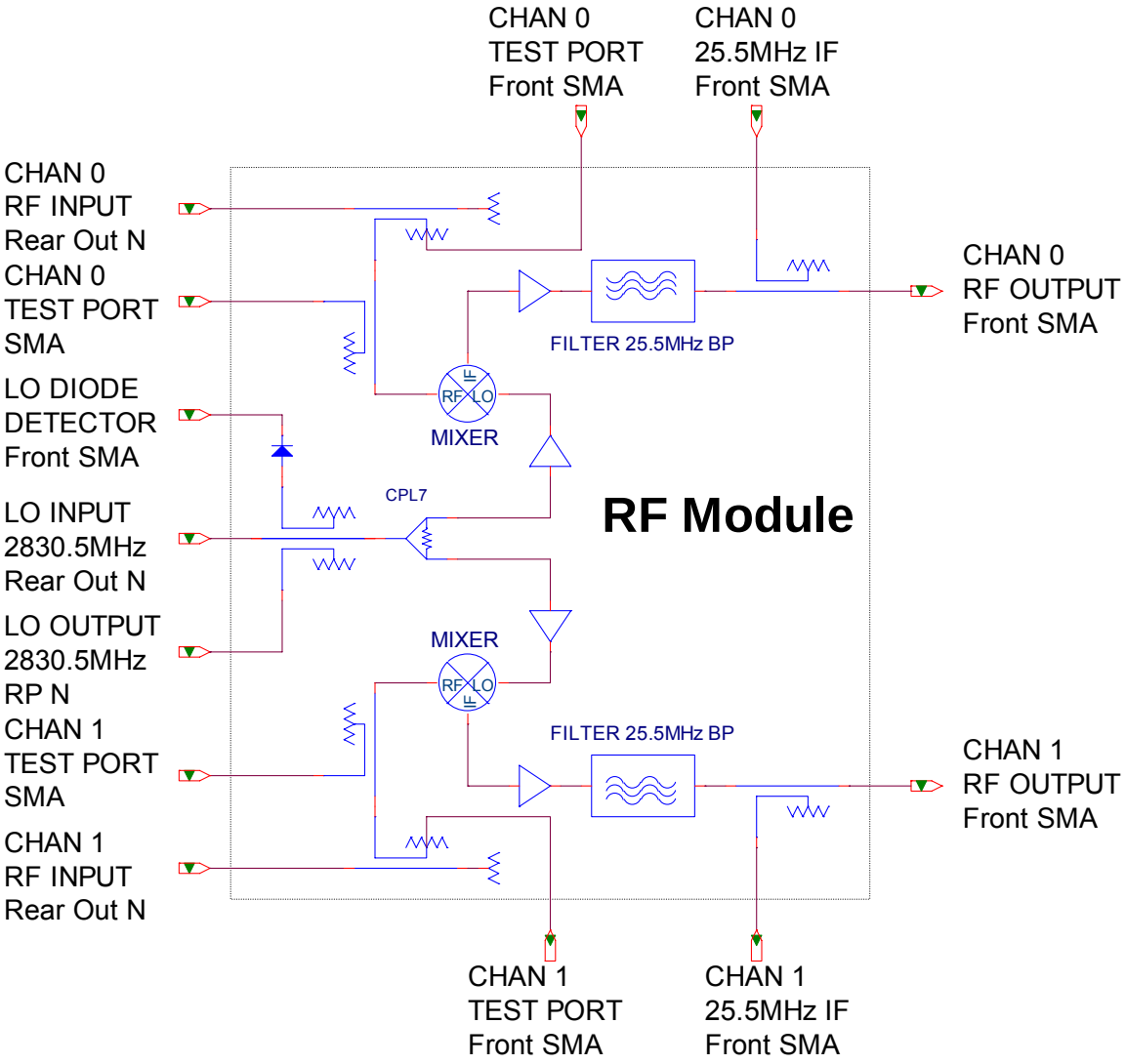


Figure 8 RF Module

2.1.5 Slow ADC Board

The slow ADC board uses a Burr-Brown ADS1218, 8 channel, 24 bit, ADC. The data is read from the ADC through the QSPI port of the control board. The 8 analog channels are fed out through 2 RJ45 jacks. The board is shown in Figure 9.

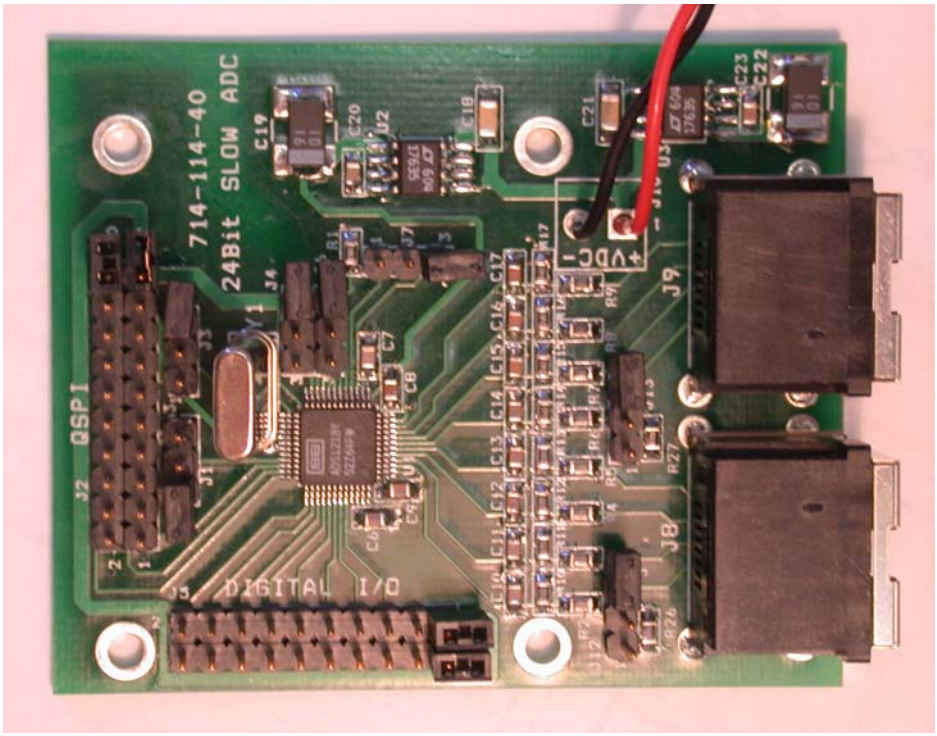


Figure 9 Slow ADC board

The ADS1218 is used with the following factory presets:

Most Significant Bit transferred first
Buffer Enabled
Internal Reference 2.5V
Speed fmod = fosc/128
Positive Ain = Ch0 Negative Ain = Ch1
Burnout Current Source disabled
PGA Gain = 1
IDACs Off
Digital I/O inputs
Decimation Register = 0780h = 1920
Format = Bipolar
Settling mode = auto
Flash Writing disabled
Offset = 000000h
FS Reg = 679024h

In this mode we expect to get over 20 effective bits.

The board has biasing for the AD590 temperature measuring device. The transfer function for this device is shown in figure ???, which gives 298.2uA + 1uA/degC. The 24bit ADC is reading the voltage across a 1.4k ohm resistor. With 20 effective bits over 2.5volt range the effective LSB is 2.4uV. 1uA/degC into 1.4k ohms is 1.4mV/degC. The effective temperature resolution of this device is 2e-3degC.

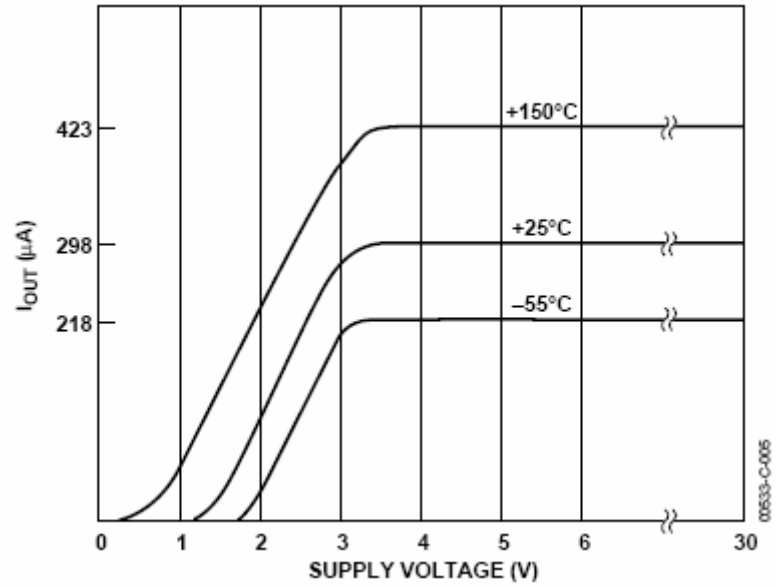


Figure 10 AD590 Transfer Function

2.2 Overview of PAD software requirements

The readout of all 4 channels and the processing must complete within 2 ms after the timing trigger.

The slow ADC values must be scaled, offset and updated at a rate of 1 Hz.

The digital data processing requirements for the beam phasing cavity are described on pages 6-10 of Phasing Cavity_ESD_04_24_06.pdf

2.3 PAD algorithms

The generic algorithm for the calculation of the average I and Q for a waveform was introduced in 1.4. A sample of the 64k 16-bit integers is read in, corrected, and independently summed over all I and all Q values in the sample. The averages are sent to the VME system. This algorithm is identified as "RF WF" in Table 3 in the next section. In general, "RF WF" is used where phase and amplitude corrections are needed. The sample size for RF devices ranges from 4 points in the Tcav to 356 points in a SLEDed RF station.

However, for the RF reference distribution, the standard deviation of the signal is also needed. The algorithm for the RF reference distribution is called "AVG + STD" in Table 3. It appends, onto the first algorithm, a second loop through the sample to determine σ^2. The standard deviation, σ, will give an indication of the noise level in the reference system since it is a continuous wave, CW, system and not a pulsed system[2]. The longer the data set, the lower the frequency of noise can be measured by σ.

[2] In a pulsed system, the phase and amplitude are changing rapidly and σ is not as useful.

Next is the algorithm used by the beam phasing cavity, called “RF WF2”. As shown in

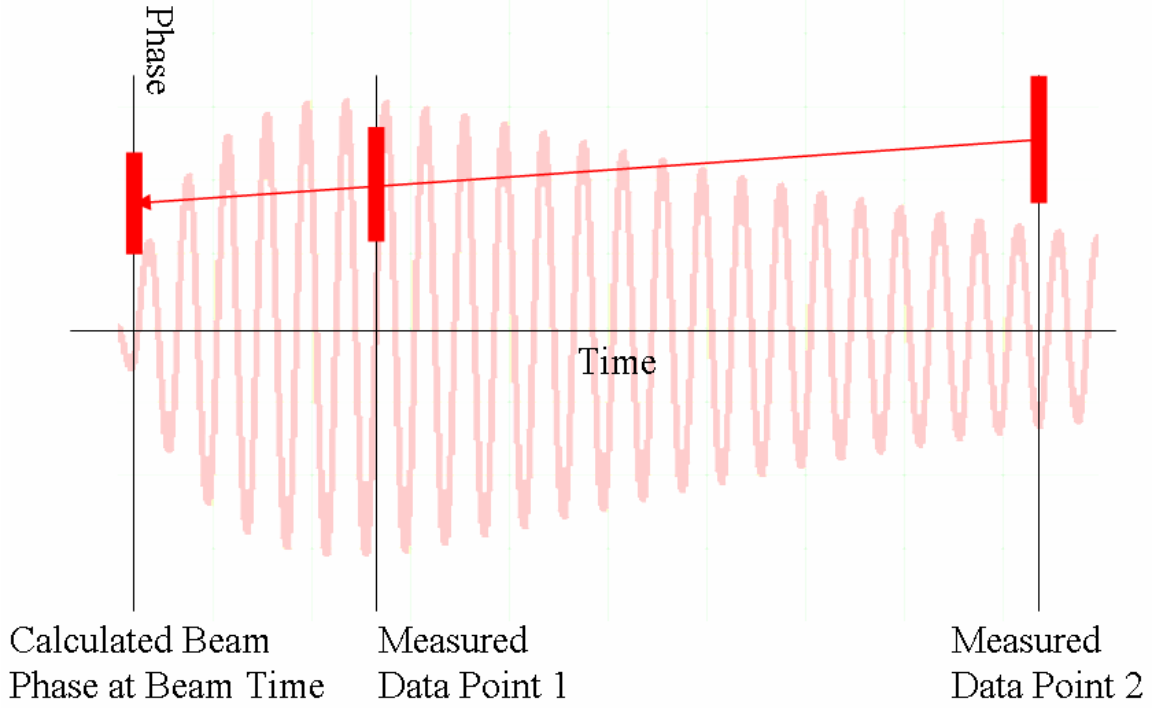


Figure 11, there are two regions of interest in the FIFOs, i.e. two samples, each with its own size and offset into the data. These samples are read in and corrected and the average I and average Q for each sample sent to the VME IOC for processing. The average phase is calculated for each point. From the two points and the equation for a line the intercept at beam time is determined. This is the beam phase. The slope of the line is scaled to the cavity frequency.

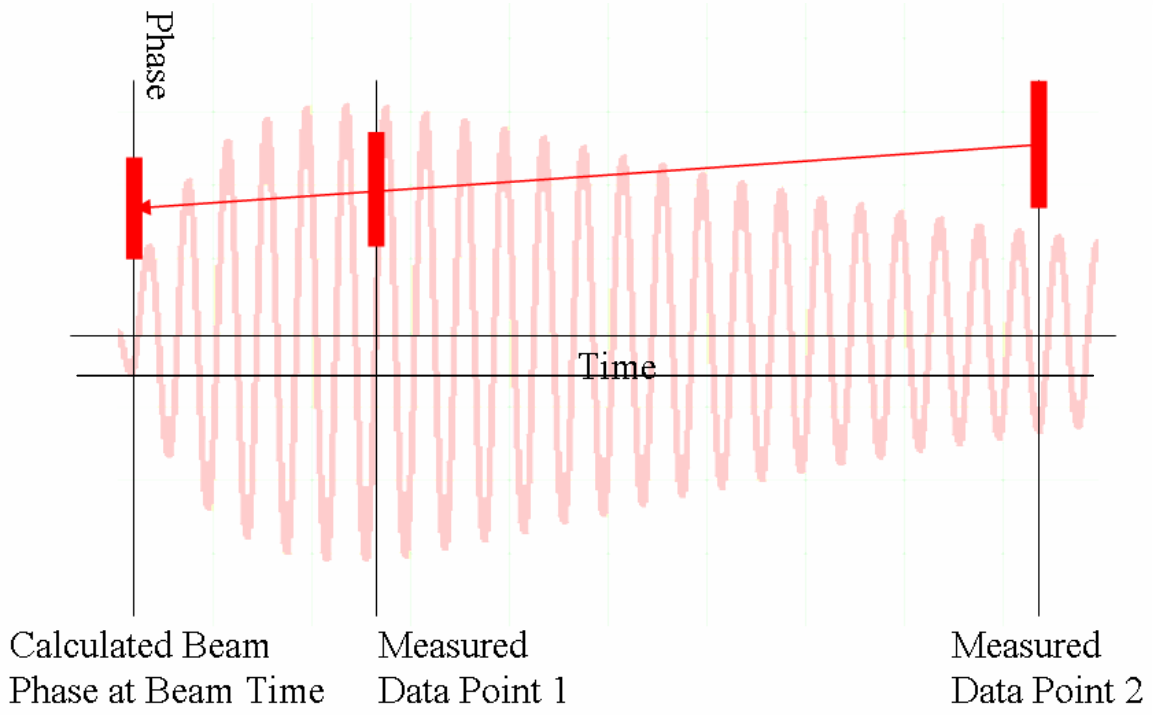


Figure 11 Calculation of freqency and phase from a line through 2 points

The PADs situated near the klystrons in the gallery can use a channel to send a single variable to the VME, i.e. no interlacing. This algorithm is called "WF" in Table 3. The raw data is corrected, but without interlacing, there is only one sum and average to determine. This channel is used to measure scalar signals, such as klystron beam voltage.

The operational mode of each PAD in the LLRF control system can change between CALIBRATING and RUNNING. When CALIBRATING, the PADs behave differently. An algorithm called "IQ CAL" is used during CALIBRATING. In "IQ CAL", no summing is done. The entire 64k sample dataset is sent to the VME where it can be used by high-level apps to determine the calibration of the IQ modulator. In this mode the PAC will put out a circle in IQ space. The PAD will read in this IQ circle and high levels apps can determine offsets, eccentricity, and tilt in the circle. Corrections will be sent back to the PAC calibration parameters.

2.4 Distribution of PAD algorithms

In Table 3 PAD Fast ADC Signals, the distribution of the algorithms is presented. These algorithms are described in 2.3. Note that there can be hybrid PADs, i.e. PADs running different algorithms in different channels.

Table 3 PAD Fast ADC Signals

PAD Fast ADC Signals				
	Digitizer			
PAD Name	***Chan 0***	***Chan 1***	***Chan 2***	***Chan 3***

RF Distribution			Sec 21		
	Signal Name	2856MHz Ref	2856MHz	119MHz	25.5MHz
	Sample Size	512	512	512	512
	Algorithm RUN	AVG + STD	AVG + STD	AVG + STD	AVG + STD
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
Laser	Signal Name	2856MHz Laser Osc	Laser Osc Pulsed	119MHz Laser Osc	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	AVG + STD	RF WF	AVG + STD	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes, but<120Hz	Yes	No	No
RFGun 1	Signal Name	Cell 1 A	Cell 1 B	Cell 2 A	Cell 2 B
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes	Yes	Yes	Yes
RFGun 2	Signal Name	For RF	REFL RF	Spare	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes	No	No	No
RF Gun Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
L0A/B	Signal Name	L0A in	L0A Out	L0B In	L0B Out
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast	Yes	Yes	Yes	Yes

	Feedback				
L0A Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
L0B Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
Tcav Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
Tcav	Signal Name	TCav In	TCav Out	Spare	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
BP1	Signal Name	Beam Phas 1A	Beam Phas 1B	Spare	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF - 2	RF WF - 2	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes	No	No	No
L1S Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw

	Fast Feedback	No	No	No	No
L1S	Signal Name	21-1B In	21-1B Out	21-1C Out	21-1D Out
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes	Yes	Yes	Yes
L1X Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Kly For
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
L1X / BP2	Signal Name	Beam Phas 2A	Beam Phas 2B	L1X In	L1X Out
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF - 2	RF WF - 2	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	Yes	No	Yes	Yes
L2Tcav Kly	Signal Name	PAC Out	Kly Drive	Kly Beam V	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	WF	WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No
L2Tcav	Signal Name	L2TCav In	L2TCav Out	Spare	Spare
	Sample Size	512	512	512	512
	Algorithm RUN	RF WF	RF WF	RF WF	RF WF
	Algorithm CAL	64K Raw	64K Raw	64K Raw	64K Raw
	Fast Feedback	No	No	No	No

2.5 Slow DAC inputs on the PAD

The queued serial port interface (QSPI) on the PAD's Acturus uCdimm 5282 processor[3] is used to send the 8 channels of the ADS1218 24-bit ADC[4] integer data (listed in Table 4) to the CPU. The channels are polled for updates; there is no hardware interrupt. These analog signals are used for diagnostics. They include RF structure temperatures, RF power levels and power supply voltages.

Table 4 PAD Slow ADC Signals

PAD Slow ADC Signals									
PAD Name		***Chan1***	***Chan2***	***Chan3***	***Chan4***	***Chan5***	***Chan6***	***Chan7***	***Chan8***
RF Distribution	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	RefA T	RefB T	RefC T	RefD T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
Laser	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	LaserA T	LaserB T	LaserC T	LaserD T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
RFGun 1	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Gun1 T	Gun2 T	Gun3 T	Gun4 T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
RFGun 2	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Gun5 T	Gun6 T	Gun7 T	Gun8T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
RF Gun Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare

[3] See http://www.slac.stanford.edu/grp/lcls/controls/global/standards/hardware/MCF5282UM.pdf chapter 22, page 471.
[4] See http://www.slac.stanford.edu/grp/lcls/controls/global/subsystems/llrf/ads1218.pdf

	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L0A/B	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	L0A 1 T	L0A 2 T	L0B 1 T	L0B 2 T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L0A Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L0B Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
Tcav Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
Tcav	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	TCav1 T	TCav2 T	TCav3 T	TCav4 T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
BP1	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	BP1A T	BP1B T	BP1C T	BP1D T
	Algorithm	Gain +	Gain + Offset	Gain +	Gain + Offset	Gain + Offset	Gain + Offset	Gain +	Gain +

		Offset		Offset				Offset	Offset
L1S Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L1S	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	21-1A T	21-1B T	21-1C T	21-1D T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L1X Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L1X / BP2	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	L1X1 T	L1X2 T	BP2A T	BP2B T
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L2Tcav Kly	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	Spare	Spare	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset
L2Tcav	Signal Name	LO Power	Local Plate T	ADC BRD T	Power Supply	L2TCav1 T	L2TCav2 T	Spare	Spare
	Algorithm	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset	Gain + Offset

2.6 PAD Software design

2.6.1 Goals

i. Minimize the amount of time spent in the driver's interrupt service routine.
ii. Minimize the time spent reading data.
iii. It is required to send each FIFO three read clocks (perform three read cycles) before valid data appears at the output of the FIFO.
iv. Take care of data type, FIFOs contain 16-bit integers and endianness across hardware.
v. Decouple the driver from the device support. Make all the device support run standalone driver routines, so that, EPICS does not have to be compiled in and so that every driver routine could be run at the command prompt to set and get values.

2.6.2 Approach

i. When a hardware interrupt is received, increment a counter and flag that new data is available to read, using an event semaphore. Use another task (thread) to read the data from the FIFOs and clear the flag.
ii. To reach the region of interest, read without storing the data. Store the data from the region of interest.
iii. Before reading a sample, add 3 to the specified offset so that the real data will be at the right place. The exception is sample 2 of the "RF WF2" algorithm described in 2.3
iv. Wrap data read/write actions with Till's basicIoOps utilities.

Instead of putting a hardware address to memory-mapped I/O in the INP or OUT field of the EPCIS record as described in section 2.1 "Hardware Addresses" in http://www.aps.anl.gov/epics/EpicsDocumentation/AppDevManuals/RecordRef/Recordref-5.html, the INP and OUT fields are used to specify the driver subroutine to be called during record processing. Here is an example: the PAD DTYP device support for longin record init routine parse the inp structure for the index, channel and sample. This is stored in the device private structure for this record instance. The read routine uses these fields to execute the correct driver subroutine with the correct parameters.

2.7 PAD Timestamping

Raw PAD data sent over the public controls LAN needs to be timestamped with the timestamp that contains the acquisition pulse id.

3 LLRF VME

3.1 Overview of VME software requirements

The software running on the VME system is responsible for:

- receiving the averaged (or raw, in the case of calibration) values from the PAD
- timestamp the PAD data with the timestamp which includes the embedded pulse id
- converting I and Q values to phase and amplitude
- monitoring the operational criteria to know
  - if there is beam
  - if each of the RF stations is in STANDBY or ACCELERATE mode
  - if the global, longitudinal, beam-based fast feedback is on
- maintain local feedback loops which control the phase and amplitude on each of the PADs' channels via a calculation:
  $R_n = A(V_{act} - V_{des}) + (1-A)R_{n-1}$
  $R_{n+1} = A(V_{act\ n+1} - V_{desn+1}) + (1-A)R_n$
  $0 < A <= 1$
- allowing each local feedback to be turned on and off independently from the others
- timestamp the corrections with the timestamp which includes the embedded pulse id
- adjust the phase and amplitude values by either the locally calculated correction or the global, longitudinal, beam-based fast feedback correction when applicable
- convert the corrected phase and amplitudes to I and Q
- timestamp the corrected I and Q values with the timestamp which include the embedded pulse id
- send the corrected I and Q values to the PAC
- store 32K values of I and Q values to a file for analysis via GUI button press
- keep a ring buffer of last 2000 I and Q values
- compute standard deviation on a variable number of I and Q values (HLA?)

3.2 VME PV calculations

3.2.1 RF_Distribution

Variables

- IACT is the averaged I value of the waveform sample
- QACT is the averaged Q value of the waveform sample
- AACT is the scaled RF power level of the measured signal.
- APC is the power scale factor which includes losses and coupler ratios.
- PACT is the offset measured phase
- POC is the phase offset to PACT

Equations

- ACT=√(IACT2+QACT2) x APCA
- PACT= Arctan(IACT/QACT) + POC

3.2.2 RF_WF

Variables

- IACT is the averaged I value of the waveform sample
- QACT is the averaged Q value of the waveform sample
- AACT is the scaled RF power level of the measured signal.
- APC is the power scale factor which includes losses and coupler ratios.
- VACT is the equivalent of the voltage in the beamline device as seen by the beam.
- AVC is the scale factor VACT to get the RF voltage as seen by the beam
- PACT is the offset measured phase
- POC is the phase offset to PACT

Equations

- AACT=√(IACT2+QACT2) x APC
- VACT=AACT2 x AVC
- PACT= Arctan(IACT/QACT) + POC

3.2.3 RF_WF-2

Variables

- I1 is the averaged I value of the waveform sample 1
- Q1 is the averaged Q value of the waveform sample 1
- I2 is the averaged I value of the waveform sample 2
- Q2 is the averaged Q value of the waveform sample 2
- PAV1 is the sample 1 phase
- PAV2 is the sample 2 phase
- PAV0 is the measured beam phase
- AAV1 is the scaled sample 1 amplitude.
- APC is the power scale factor.
- VACT is the equivalent of the bunch charge.
- FACT is the frequency calculated from the slope of the line
- AVC is the scale factor VACT to get the bunch charge

Equations

- AAV1=√(I12+Q12) x APC
- VACT=AACT2 x AVC

3.3 VME feedback calculations

3.3.1 RF Gun Tune Feedback Calculation

The calibration of the tune loop should first be done at a very low power level so the gun can be processed. After processing the gun should be run at the nominal operating power level and the tune loop recalibrated.

Inputs are:

1. Cell 1A phase
2. Cell 1A amplitude
3. Cell 1B phase
4. Cell 1B amplitude,
5. Cell 2A phase
6. Cell 2A amplitude
7. Cell 2B phase
8. Cell 2B amplitude
9. Forward RF phase
10. Forward RF amplitude

Note:

If the gun has not yet been processed, set the klystron to a forward power level that will not damage the unprocessed gun. If the gun has been processed, set the klystron forward power to the nominal value.

Steps are:

1. Average the phases (inputs 1, 3, 5, 7) using configurable weighting parameters that sum to 1. This is the cell phase used for tune and phase feedback.
2. Individual channels for the amplitude (inputs 2, 4, 6, 8, and 10) will have scale values (APCs) entered based on coupling ratios and attenuation in the system to determine fields in the cell.
3. Turn on the klystron and raise the forward power to operate the gun at the operational power level.
4. Get the cavity on resonance by changing the temperature and monitoring the ratio of cell RF amplitude to forward RF amplitude. The cell power is a weighted average of the 4 cell probe signals. This may be able to be done with a high level application such as the SCP correlation plot or MatLab. While changing water temperature measure the ratio of cell RF amplitude to forward RF amplitude. With the water temperature set to maximize this ratio, set phase calibration constants for forward RF phase and the 4 cell phases to equal 0.
5. Can use Matlab to fit a parabola to the Power Ratio vs. temperature curve.

6. Move the temperature to the peak value on the parabola. Set phase offsets (POCs) for inputs 1, 3, 5, 7, and 9 to have the respective phase read zero.
7. Now that the forward RF phase is calibrated to the cell phase , the adjusted temperature can be determined as:

   ΔTemp = (forward RF phase – cell phase) * constant

3.3.2 RF Gun Local Feedback Calculation

Inputs are:

1. Cell 1A phase
2. Cell 1A amplitude
3. Cell 1B phase
4. Cell 1B amplitude,
5. Cell 2A phase
6. Cell 2A amplitude
7. Cell 2B phase
8. Cell 2B amplitude
9. Forward RF phase
10. Forward RF amplitude

Steps are:

1. Average the phases (inputs 1, 3, 5, 7) using configurable weighting parameters that sum to 1.
2. Rotate the phase while looking at the beam energy out of the gun on a spectrometer. Set the phase to the point where the beam energy is maximum. Set the average phase correction to have an average phase reading of 0.
3. Average the amplitude (inputs 2, 4, 6, 8) using configurable weighting parameters that sum to 1.
4. Scale the average amplitude by a factor related to the beam energy out of the gun by reading the spectrometer. This should be done with the phase rotated so the energy gain is maximized.
5. Calculate the adjustments (corrections) for the phase and amplitude using PID or equivalent.
6. Convert to absolute correction (if relative is calculated)
7. Convert phase and amplitude to I and Q
8. Send to PAC

3.3.3 L0A Local Feedback Calculation

Inputs are:

1. L0A In phase
2. L0A In amplitude
3. L0A Out phase
4. L0A Out amplitude

Steps are:

1. Zero the input and output phase by rotating the phase through 360° to maximize beam energy around the dog leg and use constant measured as offset.
2. Calculate the scale factor for the amplitude by relating the input and output amplitudes to the beam energy obtained by reading the spectrometer.
3. Calculate average phase error as:
    i. (input phase + output phase)/2 – degrees running off crest
4. Calculate the average amplitude error as:
    i. (A0 x input amplitude + A1 x output amplitude)/2 – energy gain
5. Calculate the adjustments (corrections) for the phase and amplitude using PID or equivalent.
6. Convert to absolute correction (if relative is calculated)
7. Convert phase and amplitude to I and Q
8. Send to PAC

3.3.4 L0B Local Feedback Calculation

Inputs are:

1. L0B In phase
2. L0B In amplitude
3. L0B Out phase
4. L0B Out amplitude

Steps are same as L0-A with this exception: step 5 can be replaced by the application of a global fast feedback adjustment to L0B phase (only) provided: there is beam and global feedback is on in L0.

3.3.5 L0 TCav Local Feedback Calculation

Inputs are:

1. TCav In phase
2. TCav In amplitude
3. TCav Out phase
4. TCav Out amplitude
5. Spare1 phase

6. Spare1 amplitude
7. Spare2 phase
8. Spare2 amplitude

Steps are same as L0A except that there is no beam energy available. The transverse kick will be determined from the SCP using BPM data. This kick will be used to determine the RF amplitude in the structure. The zero kick crossing of the phase will be used to calibrate the phase.

3.3.6 Laser Timing Local Feedback Calculation

Inputs are:

1. I average from beam phase cavity 1 sample 1
2. Q average from beam phase cavity 1 from sample 1
3. X1, midpoint of beam phase cavity 1 sample 1 as absolute position in FIFO
4. I average from beam phase cavity 1 sample 2
5. Q average from beam phase cavity 1 sample 2
6. X2, midpoint of beam phase cavity 1 sample 2 as absolute position in FIFO

Steps:

1. Convert (I1,Q1) into Beam Phas 1A phase
2. Convert (I2, Q2) into Beam Phas 1B phase
3. Calculate the equation to the line, given points (X1, Beam Phas 1A phase) and (X2, Beam Phas 1B phase)
4. Calculate the Beam Phas 1 amplitude = $\sqrt{(I1^2 + Q1^2)}$ and Beam Phas 1 Frequency = (Beam Phas 1B -Beam Phas 1A)/(X2-X1) x Scale Factor.
5. As shown in Phasing Cavity_ESD_04_24_06.pdf, the phase of the beam equates to the y-intercept of the equation to the line for phase, the slope equates to the frequency of the cavity and the amplitude equates to the bunch charge.
6. Calculate the adjustments (corrections) for the phase and amplitude using PID or equivalent.
7. Convert to I and Q
8. Send to Laser SPAC. This PAC is not pulsed. There is no trigger. The FPGA must be configured so that the updated waveform gets sent as soon as it's updated.

3.3.7 L1S Local Feedback Calculation

Inputs are:

1. 21-1B RF input phase
2. 21-1B RF input amplitude
3. 21-1B RF output phase

4. 21-1B RF output amplitude
5. 21-1C RF output phase
6. 21-1C RF output amplitude
7. 21-1D RF output phase
8. 21-1D RF output amplitude

Steps:

0. Enter scale factors for amplitudes (inputs 2, 4, 6, and 8)
1. Average the phases (inputs 1, 3, 5, 7) using configurable weighting parameters that sum to 1.
2. Average the amplitude (inputs 2, 4, 6, 8) using configurable weighting parameters that sum to 1.
3. Scale the voltage by a factor related to the maximum beam energy gain calculated from BPM readings in DL1 and BC1 chicane.
4. Determine calibration constants for inputs 1, 3, 5 and 7. By rotating the phase and looking at the energy on a spectrometer, you choose the constant that makes the phase = 0 when the energy is maximum.
5. Calculate the adjustments (corrections) for the phase and amplitude using PID or equivalent or by the application of a global fast feedback adjustment to L1S phase and amplitude provided: there is beam and global feedback is on in L1.
6. Convert to absolute correction (if relative is calculated)
7. Convert phase and amplitude to I and Q
8. Send to L1S PAC

3.3.8 L1X Local Feedback Calculation

Inputs are:

1. L1X In phase
2. L1X In amplitude
3. L1X Out phase
4. L1X Out amplitude

Steps are the same as L0A and L0B.

3.3.9 Phase Cavity 2 Local Feedback Calculation

Inputs are:

1. I average from sample 1
2. Q average from sample 1
3. X1, midpoint of sample 1 as absolute position in FIFO
4. I average from sample 2

5. Q average from sample 2
6. X2, midpoint of sample 2 as absolute position in FIFO

Steps:

1. Convert (I1,Q1) into Beam Phas 2A phase
2. Convert (I2, Q2) into Beam Phas 2B phase
3. Calculate the equation to the line, given points (X1, Beam Phas 2A phase) and (X2, Beam Phas 2B phase)

Steps 4 to the end are same as the steps for Phase Cavity 1

3.3.10 L2 TCav Local Feedback Calculation

Inputs are:

1. L2TCav In phase
2. L2TCav In amplitude
3. L2TCav Out phase
4. L2TCav Out amplitude

Steps are same as L0 TCav Local Feedback Calculation.

3.3.11 L2

There are no PADs here to read. Adjustments to L2 phase (only) can be made by global fast feedback if there is beam and global feedback is on in L2. When global fast feedback is not on, a setpoint (configurable) will be maintained by the LLRF system. The existing RF system for the linac will hold the phase and amplitude stable enough so that corrections can be done by moving the phase of 2 klystrons. Using two klystrons the phase of each klystron can be independently rotated in such a way so that the vector sum can correct phase and amplitude variations for L2.

3.3.12 L3

There are no PADs here to read. Adjustments to L3 phase (only) can be made by global fast feedback if there is beam and global feedback is on in L3. When global fast feedback is not on, a setpoint (configurable) will be maintained by the LLRF system. There is no RF amplitude adjustment in L3. The energy of the beam is adjusted by moving the phase of the RF in sectors 29 and 30 in opposite directions so that, vectorally, the amplitude is changed without changing phase. The global feed back here is used to correct beam energy at the end of the linac.

3.4 VME Software design

3.4.1 Goals

The goal is to implement the algorithms listed in 3.3 using existed soft[5] EPICS records.

[5] Soft EPICS records handle data in memory; there is no hardware device involved.

3.4.2 Approach

Each instance of each algorithm requires its own record set. The approach is to implement the instance name as the stem of the record name and then the record set as a set of leaves off the stem. For display purposes, variables which are changing at the operational frequency of the machine are not shown. Rather, a slowly updated (eg 1 Hz) copy is maintained and drawn in the display.

Table 5 Process variables on LRLF VME system

Process variables on LLRF VME system

Note 1: All PVs prepended by $(PRIM):$(LOCA):$(UNIT):
Note 2: NAME = NAME STEM + NAME LEAF
Note 3: SLOW LEAF is the slow 1 Hz update copy of the NAME LEAF PV used in displays

Part 1: Record Set Definitions

NAME STEM	NAME LEAF	SLOW LEAF	DESCRIPTION	REC TYPE	INPUT FROM	OUTPT TO	SCAN METHOD
RF Reference, AVG + STD, algorithm record set needed in VME for one PAD channel							
$(STEM)	IACT	S_I	I average	ai	PAD	AACT,PACT	CP link
	QACT	S_Q	Q average	ai	PAD	AACT,PACT	CP link
	AACT	S_AA	measured ampl	calcout	I,QACT	diags	IACT flnk
	PACT	S_PA	measured phase	calcout	I,QACT	diags	IACT flnk
	ISS	S_IS	I variance	ai	PAD	ISG	CP link
	QSS	S_IQ	Q variance	ai	PAD	QSG	CP link
	ISG	S_IG	I sigma	calcout	ISS	diags	ISS flnk
	QSG	S_QG	Q sigma	calcout	ISQ	diags	ISQ flnk
	APC		ampl power correction	ao	GUI	AACT	caput
	POC		phase offset correction	ao	GUI	PACT	caput
RF Reference, AVG + STD, algorithm record set needed in VME for one PAD							
There is no combining of the RF REF PAD channel data, I.e, averaging and correcting needed.							
The RF Ref PAC adjusts the timing of the laset and is set by the laser timing feedback beam phasing cavity 1.							
RF WF algorithm record set needed in VME for one PAD channel							
$(STEM)	IACT	S_I	I average	ai	PAD	AACT,PACT	CP link
	QACT	S_Q	Q average	ai	PAD	AACT,PACT	CP link
	AACT	S_AA	scaled RF power of meas ampl	calcout	I,QACT	AAVG	IACT flnk
	PACT	S_PA	offset measured phase	calcout	I,QACT	PAVG	IACT flnk
	VACT	S_VA	beam voltage gain	calcout	AACT	?	AACT flnk
	AWT		weight factor ampl	ao	GUI	AAVG	caput
	PWT		weight factor phase	ao	GUI	PAVG	caput
	APC		ampl power correction	ao	GUI	AACT	caput
	POC		phas offset correction	ao	GUI	PACT	caput

	AVC		scale factor for VACT	ao	GUI	VACT	caput
RF Reference, AVG + STD, algorithm record set needed in VME for one PAD							
AAVG		S_AV	ampl average from all chans	calcout	4 AACT,AWT	FB	AACT flnk
PAVG		S_PV	phas average from all chans	calcout	4 PACT,PWT	FB	PACT flnk
ACOR		S_AC	ampl adjust	ao	FB	ADES	AAVG flnk or global FB
PCOR		S_PC	phase adjust	ao	FB	PDES	PAVG flnk or global FB
ADES		S_AD	ampl setpoint	ao	AAVG,ACOR	IDES,QDES	ACOR flnk
PDES		S_PD	phase setpoint	ao	PAVG,PCOR	IDES,QDES	PCOR flnk
IDES		S_ID	I setpoint	ao	ADES,PDES	PAC	
QDES		S_QD	Q setpoint	ao	ADES,PDES	PAC	
IQ CAL algorithm record set needed in VME for one PAD channel							
	DATA			wf	PAD	HLA	CP link
WFalgorithm record set needed in VME for one PAD channel							
	SACT	S_S	sample average	ai	PAD	diags	CP link
RF WF - 2 algorithm record set needed in VME for one PAD channel							
	I1	S_I1	sample 1 average I	ai	PAD	PAV1,AAV1	CP link
	Q1	S_Q1	sample 1 average Q	ai	PAD	PAV1,AAV1	CP link
	I2	S_I2	sample 2 average I	ai	PAD	PAV2	CP link
	Q2	S_Q2	sample 2 average Q	ai	PAD	PAV2	CP link
	X1	S_X1	sample 1 midpoint	ai	PAD	PAV1	CP link
	X2	S_X2	sample 2 midpoint	ai	PAD	PAV2	CP link
	AWT		weight factor ampl	ao	GUI	AAVG	caput
	PWT		weight factor phase	ao	GUI	PAVG	caput
	APC		ampl power correction	ao	GUI	AACT	caput
	AVC		scale factor for VACT	ao	GUI	PACT	caput
	FACT		slope of line	ao	PAV0,PAV1,AAV1	VACT	PAV0 flnk
	PAV1	S_A1	sample 1 phase	ao	I1,Q1	PAVG	X1 flnk
	PAV2	S_A2	sample 2 phase	ao	I2,Q2	PAVG	X2 flnk
	PAV0	S_P0	y intercept	ao	X1,PAV1,X2,PAV2		PAV2 flnk
	VACT	S_VA	bunch charge	ao	AAV1	diags	
	AAV1	S_AA	scaled sample 1 ampl	ao	I1,Q1	AAVG	FACT flnk
RF WF-2 algorithm record set needed in VME for the two channel beam phase cavity PAD							
AAVG		S_AV	ampl average for 2 chans	ao	AAV1		
PAVG		S_PV	phas average for 2 chans	ao	PAV1,PAV2		
ACOR		S_AC	ampl adjust	ao	GUI		
PCOR		S_PC	phase adjust	ao	GUI		

ADES		S_AD	ampl setpoint	ao	AAVG,ACOR		
PDES		S_PD	phase setpoint	ao	PAVG,PCOR		
IDES		S_ID	I setpoint	ao	ADES,PDES		
QDES		S_QD	Q setpoint	ao	ADES,PDES		

Part 2: Record List by LLRF subsystems

PRIM:	LOCA:	UNIT:	NAME OR NAME STEM FOR RECORD SET	RECORD SET (RUNNING)	RECORD SET (CALIBRATING)	COMMENTS
LLRF Subsystem: RF Reference Distribution						
LLRF_KLYS	IN20	RH	REF_0_	AVG + STD	IQ CAL	
LLRF_KLYS	IN20	RH	REF_1_	AVG + STD	IQ CAL	
LLRF_KLYS	IN20	RH	REF_2_	AVG + STD	IQ CAL	
LLRF_KLYS	IN20	RH	REF_3_	AVG + STD	IQ CAL	
LLRF_KLYS	IN20	RH	REF_FB			RF Distribution feedback status
LLRF_KLYS	IN20	RH	REF_PAD_ST			RF Distribution PAD operational state
~~LLRF_KLYS~~	~~IN20~~	~~RH~~	~~REF_PAC_ST~~	-	-	~~RF Distribution PAC operational state~~ May not be needed
LLRF Subsystem: RF Laser						
LLRF_KLYS	IN20	RH	LSR_0_	AVG + STD	IQ CAL	PAD channels 2 and 3 are unread spares
LLRF_KLYS	IN20	RH	LSR_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	LSR_FB			Laser local feedback status
LLRF_KLYS	IN20	RH	LSR_PAD_ST			Laser PAD operational state
LLRF_KLYS	IN20	RH	LSR_PAC_ST			Laser PAC operational state
LLRF Subsystem: RF Gun						
LLRF_KLYS	IN20	RH	GN1_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN1_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN1_2_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN1_3_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN2_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN2_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN2_2_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	GN2_3_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL601	GN3_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL601	GN3_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL601	GN3_2_	WF	IQ CAL	
LLRF_KLYS	IN20	BL601	GN3_3_	WF	IQ CAL	
LLRF_KLYS	IN20	BL601	GUN_FB			Klystron 20-6 local feedback status

LLRF_KLYS	IN20	RH	GN1_PAD_ST			RF Gun 1 PAD operational state
LLRF_KLYS	IN20	RH	GN2_PAD_ST			RF Gun 2 PAD operational state
LLRF_KLYS	IN20	BL601	GN3_PAD_ST			RF Gun Kly PAD operational state
LLRF_KLYS	IN20	BL601	GUN_PAC_ST			RF Gun Kly PAC operational state
LLRF_KLYS	IN20	BL601	KLY_STATE			From PNET data, for current pulse, is kly in ACCEL or STDBY?

LLRF Subsystem: L0-A

LLRF_KLYS	IN20	RH	LOA_0_	RF WF	IQ CAL	sharing PAD with L0B
LLRF_KLYS	IN20	RH	LOA_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL701	LOA_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL701	LOA_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL701	LOA_2_	WF	IQ CAL	
LLRF_KLYS	IN20	BL701	LOA_3_	WF	IQ CAL	
LLRF_KLYS	IN20	BL701	L0A_FB			Klystron 20-7 local feedback status
LLRF_KLYS	IN20	RH	L0_STATE			L0-A/L0-B PAD operational state
LLRF_KLYS	IN20	BL701	L0A_PAD_ST			L0-A Kly PAD operational state
LLRF_KLYS	IN20	BL701	L0A_PAC_ST			L0-A Kly PAC operational state
LLRF_KLYS	IN20	BL701	KLY_STATE			From EVG event number, for current pulse, is kly in ACCEL or STDBY

LLRF Subsystem: L0-B

LLRF_KLYS	IN20	RH	LOB_2_	RF WF	IQ CAL	sharing PAD with L0A
LLRF_KLYS	IN20	RH	LOB_3_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL801	LOB_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL801	LOB_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL801	LOB_2_	WF	IQ CAL	
LLRF_KLYS	IN20	BL801	LOB_3_	WF	IQ CAL	
LLRF_KLYS	IN20	BL801	LOB_FB			Klystron 20-8 local feedback status
LLRF_KLYS	IN20	BL801	LOB_PAD_ST			L0-B Kly PAD operational state
LLRF_KLYS	IN20	BL801	L0B_PAC_ST			L0-B Kly PAC operational state
LLRF_KLYS	IN20	BL801	KLY_STATE			From PNET data, for current pulse, is kly in ACCEL or STDBY?

LLRF Subsystem: L0 Tcav

LLRF_KLYS	IN20	RH	TCV_0_	RF WF	IQ CAL	

LLRF_KLYS	IN20	RH	TCV_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	TCV_2_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	TCV_3_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL501	TCV_0_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL501	TCV_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	BL501	TCV_2_	WF	IQ CAL	
LLRF_KLYS	IN20	BL501	TCV_3_	WF	IQ CAL	
LLRF_KLYS	IN20	BL501	TCV_FB			Klystron 20-5 local feedback status
LLRF_KLYS	IN20	RH	TCV_PAD_ST			TCav PAD operational state
LLRF_KLYS	IN20	BL501	TCV_PAD_ST			TCav PAD operational state
LLRF_KLYS	IN20	BL501	TCV_PAC_ST			TCav Kly PAC operational state
LLRF_KLYS	IN20	BL501	KLY_STATE			From PNET data, for current pulse, is kly in ACCEL or STDBY?

LLRF Subsystem: Beam Phasing Cavity 1

LLRF_KLYS	IN20	RH	PH1_0_	RF WF - 2	IQ CAL	
LLRF_KLYS	IN20	RH	PH1_1_	RF WF - 2	IQ CAL	
LLRF_KLYS	IN20	RH	PH1_2_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	PH1_3_	RF WF	IQ CAL	
~~LLRF_KLYS~~	~~IN20~~	~~RH~~	~~PH1_FB~~			LSR_FB replaces the need for this
LLRF_KLYS	IN20	RH	PH1_PAD_ST			Beam Phas Cav 1 PAD operational state
LLRF_KLYS	IN20	RH	PH1_PAC_ST			Beam Phas Cav 1 PAC operational state

LLRF Subsystem: L1-S

LLRF_KLYS	IN20	RH	L1S_0_	RF WF	IQ CAL	LOCA is IN20 because PAD is in RH
LLRF_KLYS	IN20	RH	L1S_1_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	L1S_2_	RF WF	IQ CAL	
LLRF_KLYS	IN20	RH	L1S_3_	RF WF	IQ CAL	
LLRF_KLYS	LI21	BL101	L1S_0_	RF WF	IQ CAL	
LLRF_KLYS	LI21	BL101	L1S_1_	RF WF	IQ CAL	
LLRF_KLYS	LI21	BL101	L1S_2_	WF	IQ CAL	
LLRF_KLYS	LI21	BL101	L1S_3_	WF	IQ CAL	
LLRF_KLYS	IN20	RH	L1S_FB			
LLRF_KLYS	IN20	RH	L1S_PAD_ST			L1S PAD operational state
LLRF_KLYS	IN20	BL101	L1S_PAD_ST			L1S Kly PAD operational state
LLRF_KLYS	IN20	BL101	L1S_PAC_ST			L1S PAC operational state

LLRF_KLYS	L121	BL101	KLY_STATE			From PNET data, for current pulse, is kly in ACCEL or STDBY?

LLRF Subsystem: L1-X

LLRF_KLYS	IN20	RH	L1X_2_	RF WF	IQ CAL	LOCA is IN20 because PAD is in RH
LLRF_KLYS	IN20	RH	L1X_3_	RF WF	IQ CAL	sharing PAD with PH2
LLRF_KLYS	LI21	BL201	L1X_0_	RF WF	IQ CAL	
LLRF_KLYS	LI21	BL201	L1X_1_	RF WF	IQ CAL	
LLRF_KLYS	LI21	BL201	L1X_2_	WF	IQ CAL	
LLRF_KLYS	LI21	BL201	L1X_3_	WF	IQ CAL	
LLRF_KLYS	IN20	RH	L1X_FB			
LLRF_KLYS	IN20	RH	L1X_PAD_ST			L1X PAD operational state
LLRF_KLYS	IN20	BL201	L1X_PAD_ST			L1X Kly PAD operational state
LLRF_KLYS	IN20	BL201	L1X_PAC_ST			L1X PAC operational state

LLRF Subsystem: Beam Phasing Cavity 2

LLRF_KLYS	IN20	RH	PH2_0_	RF WF - 2	IQ CAL	sharing PAD with L1X
LLRF_KLYS	IN20	RH	PH2_1_	RF WF - 2	IQ CAL	
LLRF_KLYS	IN20	RH	PH2_FB			
~~LLRF_KLYS~~	~~IN20~~	~~RH~~	~~PH2_PAD_ST~~			use L1X_PAD_ST since sharing

LLRF Subsystem: L2 Tcav

LLRF_KLYS	LI24	BL801	TC1_0_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC1_1_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC1_2_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC3_0_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC2_0_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC2_1_	RF WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC2_2_	WF	IQ CAL	
LLRF_KLYS	LI24	BL801	TC2_0_	WF	IQ CAL	
LLRF_KLYS	IN20	RH	TC2_FB			

Additional PVs
global feedback on/off

LLRF_KLYS	IN20	RH	G_L0_FB_CTL			LOCA may change
LLRF_KLYS	LI21	RH	G_L1_FB_CTL			
LLRF_KLYS	LI24	RH	G_L2_FB_CTL			
LLRF_KLYS	LI30	RH	G_L3_FB_CTL			

beam y/n

LLRF_KLYS	IN20	RH	L0_BEAM			Get this from PH1 amplitude
LLRF_KLYS	LI21	RH	L1_BEAM			Get this from PH2 amplitude
~~LLRF_KLYS~~	~~LI24~~	~~RH~~	~~L2_BEAM~~			There is no way to read this yet
~~LLRF_KLYS~~	~~LI30~~	~~RH~~	~~L3_BEAM~~			There is no way to read this yet

3.5 VME data timestamping

The PNET data records (PP, YY, etc) arriving in the EVR at 360 Hz contain the pulse id in the lower 17 bits of the nanosecond field of the EPICS record timestamp field. The averages sent to the VME will be stamped with this timestamp when they arrive. Checks must be in place to use the correct timestamp, since the PNET records will be pipelined and sent 3 in advance to the EVR.

4 LLRF Phase and Amplitude Controller (PAC)

4.1 PAC Hardware Design

The PAC is design to adjust the phase and amplitude of an RF signal using 2 analog outputs to run an IQ mixer. A block diagram is shown in Figure 12 and a picture of the prototype chassis in Figure 13. The main components in the PAC chassis are the control board and the RF module.

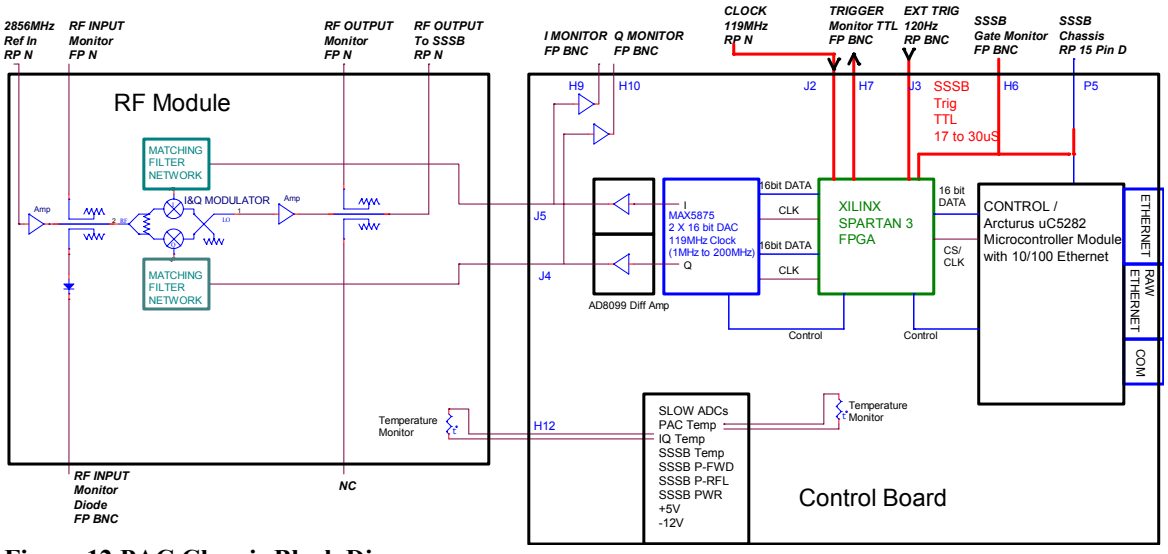


Figure 12 PAC Chassis Block Diagram

Figure 13 Prototype PAC Chassis

4.1.1 Control Board

The control board uses a MAX5875 two channel 16 bit, 200MSPS, DAC to clock out waveforms which are stored in a Xilinx Spartan 3 FPGA. The coldfire processor is memory mapped to two 2k 16bit sample waveforms in the FPGA. On a trigger the two waveforms are simultaneously clocked out the dual DAC. Voltage waveforms of up to ±1.25Volts are sent out to the IQ modulator. The FPGA has an internal trigger mode to continuously write out a waveform. The unit is calibrated by writing a cosine to one waveform and a sine to the other. In this mode the unit becomes a single side band modulator.

There are 8 analog input to PAC board which use the 14 bit, 8 single ended channels, MAX1149 ADC. The ADC is connected through the serial port to the FPGA. The FPGA places the data from the ADC in eight 16 bit registers which are memory mapped to the Arcturus uCDIMM. Three of the eight input channels are used to measure temperature of the control board, the RF Module, and where applicable the SSSB. The two 12VDC power supplies in the SSSB are monitored along with the bulk 5 Volt supply for the control board and the 15V bulk supply for the RF Module. The last ADC channel is used to monitor RF Power level.

4.1.2 Control board tests

In order to measure distortion, the PAC was set up to run a SSB modulator. The FPGA was programmed to output a 2048 point sine and cosine wave at a level of 2.5Vp-p. The PAC was clocked with a 119MHz 13dBm input low noise oscillator. The output frequency was about 58kHz, 119MHz/2048. The sine and cosine outputs were connected to the I and Q inputs of an IQ modulator. The LO input of the IQ modulator was driven with +17dBm of 476MHz from a low noise oscillator. The output, RF port, of the modulator was connected to an Agilent E4407B spectrum analyzer.

The Figure 14 shows the lower side band frequency shifted 476MHz. The measurement below has distortion both from the PAC and measurement system. The distortion harmonics are all below 60dB from the carrier and will meet LCLS specifications for the RF system.

The RBW of the spectrum analyzer for the below plot is 100Hz. The noise floor level in the plot is -125dBm/Hz, about -122dBc/Hz, and is likely that of the analyzer. Another setup will need to be done to measure the added noise of the modulator. The input RF used in this test has a noise floor of better than -150dBc/Hz.

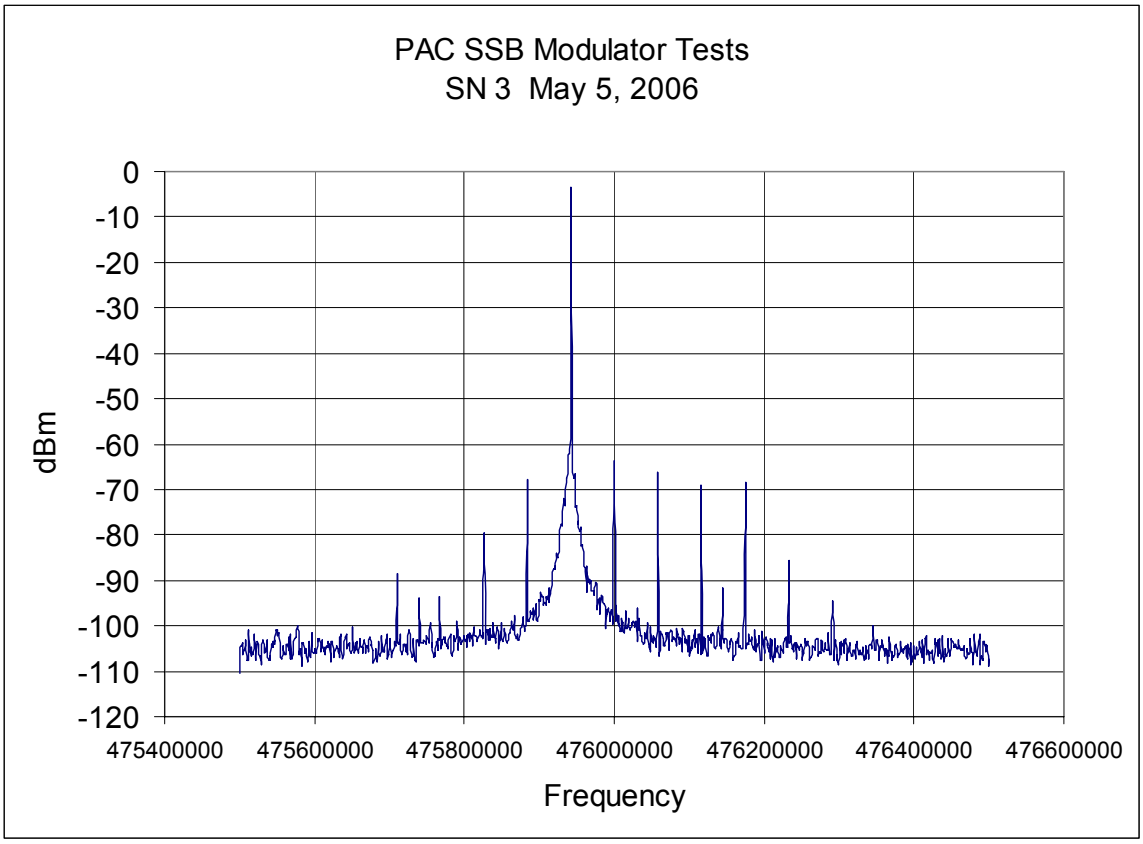


Figure 14 PAC as SSB Modulator

4.1.3 RF Module

There will be a total of 17 PACs used in LCLS. The number of PACs and frequency control are given below:

102MHz	1
476MHz	4
2830.5MHz	1
2856MHz	10
11.424GHz	1

It was decided to make an RF module for the 11 PACs at 2856MHz and 2830.5MHz. The other frequency PACs RF Module will be made with discrete components. The RF Module for 2856MHz is mounted in the rear of the prototype chassis shown in Figure 13.

4.2 Overview of PAC software requirements

The PAC software requirements are given in http://www.slac.stanford.edu/grp/lcls/controls/global/subsystems/llrf/LCLS RF PAC Control Spec.pdf. The PAC software receives the corrected I and Q values from the VME system as soon as it is calculated (i.e. there is no trigger). A new waveform is calculated and stored in the FPGA. The FPGA sends out the waveform on the next timing trigger. In addition to this, when the PAC is in CALIBRATING mode, the FPGA is loaded with a

calibration waveform and then the offset and gain of I and Q can be adjusted until you get a circle.

4.3 PAC algorithms

The algorithm running in the PAC depends on the operational mode of the PAC. The mode can be CALIBRATING or RUNNING. At startup, the I and Q calibration waveform and the I and Q operational waveforms are loaded into memory from files stored on the server.

When CALIBRATING, the PAC uses the I and Q calibration waveforms along with the operator entered values for I and Q gain and offset to calculate the new I and Q waveforms for the FPGA:

I waveform = I cal waveform * I gain + I offset
Q waveform = Q cal waveform * Q gain + Q offset

When RUNNING, the PAC uses the I and Q operational waveforms, the latest I and Q gain and offset values (from the last calibration) and the operator entered values for I and Q adjustments to calculate the new I and Q waveforms for the FPGA:

I waveform = I operational waveform * I gain * I adjust + I offset
Q waveform = Q operational waveform * Q gain * Q adjust + Q offset

In both operational modes, the next timing trigger sends FPGA contents out to IQ modulator.

4.4 Slow ADC inputs on the PAC

The slow ADC on board the PAC is used to monitor eight 16-bit analog signals. They are described in PAC datasheet.

4.5 PAC Software design

4.5.1 Goals

Minimize time spent copying waveform data.

4.5.2 Approach

Avoid waveform copies by computing the new waveform directly in the memory-mapped I/O space, free the BPTR field of the waveform record and point it at the address of the FPGA.

Use a state machine to keep track of which waveform calculation to do.

State machine for LLRF PAC

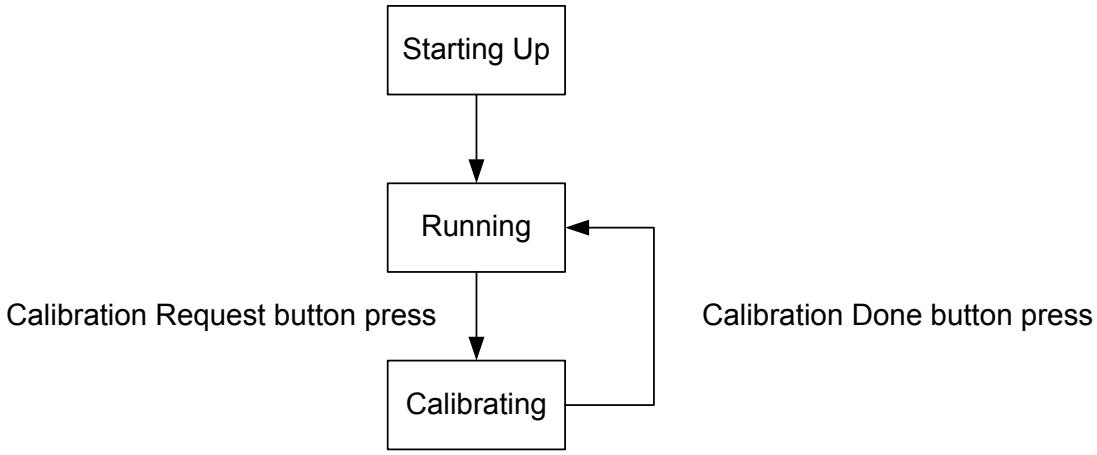


Figure 15 State machine for LLRF PAC

5 LLRF System Interfaces

5.1 Event System and Timing Trigger Interface

5.1.1 Trigger timing for the PAD and PAC

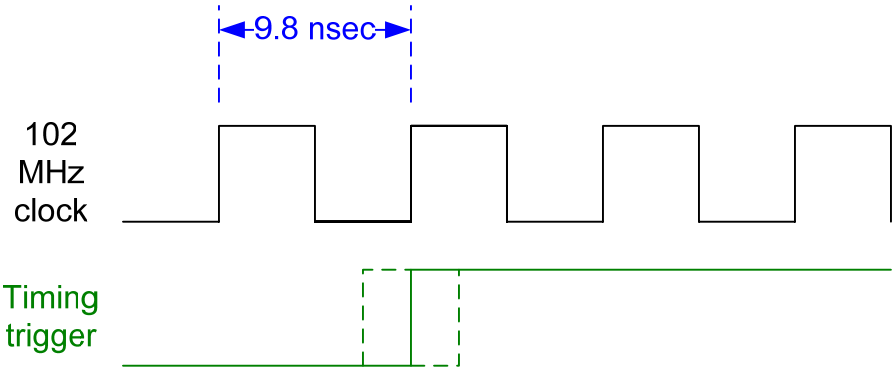


Figure 16 Timing trigger granularity

As described in 1.4, timing triggers are needed by the PADs and PACs. A list is given in Table 6The PAD uses a 102MHz clock to clock in data starting with a trigger. The PAC uses a 102MHz clock to clock out data starting with a trigger. For both the PAD and the PAC, if the trigger is too close to the clock edge, it may or may not trigger on the specific clock edge shown in Figure 16. If it does not trigger of the clock edge it is close to, it will trigger on the next clock edge. This will cause jitter in the RF if it occurred in the PAC and measured jitter plus a 90degree phase jump, not in the RF, if it occurs in the PAD. To eliminate this, the triggers should be timed in. To optimally set the trigger timing, the trigger would need to be moved in divisions much smaller than the 9.8nSec clock cycle.

To time in the PAD trigger, the trigger will need to be moved until the RF phase jumps 90degrees one way and then moved the opposite direction until the RF phase jump 90 degrees the opposite direction. The trigger should then be set in the center.

To time in the PAC trigger, the trigger should be moved one direction until the output waveform jumps by 9.8nS. The trigger is then moved the opposite direction until the waveform jumps the other direction. The trigger should be centered between these two points.

The width of the timing triggers was selected to be 100 ns, so that it is wide enough to ensure that the PAD or PAC gets triggered and short enough so that the input coupling transformer does not saturate.

Table 6 LLRF Timing Triggers

LLRF Timing Triggers				
General Location	***Destination Device***	***Type***	***Date needed***	***Requirements***
near klystron 20-5 in the gallery				
	L0 Tcav Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L0 Tcav Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 20-6 in the gallery				100 nsec pulse width, 2.1 nsec granularity
	RF Gun Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Gun Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 20-7 in the gallery				100 nsec pulse width, 2.1 nsec granularity
	L0A Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L0A Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 20-8 in the gallery				100 nsec pulse width, 2.1 nsec granularity
	L0B Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity

	L0B Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 21-1 in the gallery				100 nsec pulse width, 2.1 nsec granularity
	L1S Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L1S Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 21-2 in the gallery				100 nsec pulse width, 2.1 nsec granularity
	L1X Kly PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L1X Kly PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
in the RF Hut				100 nsec pulse width, 2.1 nsec granularity
	RF Distribution PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Distribution SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Distribution SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Distribution SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Distribution SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Distribution SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	Laser SPAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	Laser PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity

	RF Gun 1 PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	RF Gun 2 PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L0A PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	PH01 PAC	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	PH01 PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L1S PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	PH02 PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	L1X PAD	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	oscillosope 1	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	oscillosope 2	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
	Phase-locked loop	TTL	11/01/06	adjustable (100 nsec-5ms) pulse width. 120 Hz, fixed TRBR
	BCS	TTL	11/01/06	120 Hz, fixed TRBR
	BCS	TTL	11/01/06	120 Hz, fixed TRBR
	BCS	TTL	11/01/06	100 nsec pulse width, 2.1 nsec granularity
near klystron 24-1 in the gallery				
	L2 24-1 Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
near klystron 24-2 in the gallery				
	L2 24-2 Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
near klystron 24-3 in the gallery				

	L2 24-3 Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
near klystron 24-8 in the gallery				
	L2 TCav Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
	L2 Tcav Kly PAD			
	L2 TCav PAD			
near sector 29 subbooster				
	L3 29 Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
near sector 30 subbooster				
	L3 30 Kly PAC	TTL	07/01/07	100 nsec pulse width, 2.1 nsec granularity
Explanations:				
PAD = Phase and Amplitude Detector				
PAC = Phase and Amplitude Controller				

5.1.2 Events

LCLS Timing system events related to LLRF consist of ACCELERATE and STANDBY events, one per klystron. A list is given in Table 7. The LLRF ACCELERATE events arrive such that the triggers can occur at least 20 μs before the beam. The LLRF STANDBY events arrive after the ACCELERATE event at one of 5 pre-selected, fixed times set by the BCS system. These STANDBY times are as follows:

- 26.8uμS (not used)
- 35.4μS
- 44.0μS
- 52.6μS
- 61.2μS
- 69.8μS
- 78.4μS (not used)

The gun will be set at a different STANDBY time from L0 and L1 to prevent dark current acceleration.

Table 7 LLRF Timing Events from LCLS Timing System Event Generator

LLRF Timing Events from LCLS Timing System Event Generator

Event Name	***Time sent after 360 Hz fiducial (μs)***

Accelerate 20-5	840.0000
Accelerate 20-6	840.0084
Accelerate 20-7	840.0168
Accelerate 20-8	840.0252
Accelerate 21-1	840.0336
Accelerate 21-2	840.0420
Accelerate 24-1	840.0504
Accelerate 24-2	840.0588
Accelerate 24-3	840.0672
Accelerate 24-8	840.0756
Standby 20-5	Accelerate 20-5 time + BCS delay
Standby 20-6	Accelerate 20-6 time + BCS delay
Standby 20-7	Accelerate 20-7 time + BCS delay
Standby 20-8	Accelerate 20-8 time + BCS delay
Standby 21-1	Accelerate 21-1 time + BCS delay
Standby 21-2	Accelerate 21-2 time + BCS delay
Standby 24-1	Accelerate 24-1 time + BCS delay
Standby 24-2	Accelerate 24-2 time + BCS delay
Standby 24-3	Accelerate 24-3 time + BCS delay
Standby 24-8	Accelerate 24-8 time + BCS delay

5.2 Longitudinal Beam-based Fast Feedback Interface

Longitudinal, beam-based fast feedback will have the capacity to set corrections to:

- L0-B phase
- L1-S phase
- L1-S amplitude
- L2 phase and amplitude
- L3 amplitude

given that there is beam and that global feedback for the appropriate section is ON. The corrections are set by writing to setpoint PVs which are then converted to I and Q values and sent out to the PACs. Steps showing how the global corrections are incorporated into the system are described in section 3.2. See step 5 of 3.3.7, for example.

Longitudinal, beam-based fast feedback has the capability to read any of the process variables listed in Table 5 Process variables on LRLF VME system.

5.3 Vacuum

The Vacuum system consists of ion pumps, vacuum gauges, vacuum valves and a PLC system. The vacuum PLC has interlock input to the existing MKSU. When faulted, the MKSU removes the modulator trigger. It is likely that the Non-Ionizing Radiation Committee requires this system to be in place and operational before start up. This system is outside the scope of this document, and review. In the event of a vacuum fault, the RF system will detect no RF and the feedback will ignore this data.

5.4 BCS

When a fault occurs, the existing BCS system inhibits the Sub-Booster from driving the klystrons during beam time. However, the existing BCS is unable to inhibit a Solid State Sub-Booster (SSSB) from driving an individual klystron. The new BCS system will provide triggers to the SSSB to maintain the BCS function. During a BCS fault the accelerate trigger will go away and a standby trigger will appear at the preset standby time. This system is outside the scope of this document, and review.

5.5 Water

Water systems to high power RF components have flow switches which are connected to interlocks in the associated MKSU. Low water flow to these devices will shut off the corresponding klystron through the existing MKSU interlock.

The water temperature effects phase and power in the RF devices. Local feedback loops are expected to regulate RF phase and amplitude during temperature changes. All the LLRF Chassis use water to stabilize phase and amplitude. There are temperature sensors in the PADs and PACs to monitor water temperature. Other chassis do not have temperature sensors. For chassis where the loss of cooling water may result in a failure, Klixons will be used to remove power. There is currently no flow switch planned in the LLRF water system.

5.6 SCP interface

Correlation plots are needed of LLRF phase or amplitude vs. beam position, etc. By enabling the LLRF VME system as an SLC-aware IOC, it will be able to participate in beam synchronous data acquisition commands from the SCP.

6 High level applications

6.1 Generic high level applications needed by LLRF

6.1.1 Correlation plots

6.1.2 Calibration of power levels using beam energy

Calibration of high power rf couplers in systems can have errors as high as 1dB. It is nice to have the RF power levels calibrated to levels of 0.1dB. The beam energy gain or kick through an RF structure can be measured much more accurately than RF power levels. It is desired to have a way to measure the beam energy gain and or strength of kick to calibrate high power RF readings.

6.2 High level applications needed by RF Reference Distribution system

The goal of the reference distribution system, Figure 17, is to supply phase stable signals to the PADs and PACs. The PADs and PACs in the reference system are used to monitor the phase stability of the system and maintain phase relationships.
There is no continous feedback planned in the RF reference system. All RF components are located on temperature stabilized water plates and where critical heliax cables are located in temperature controlled environments.

There are two places where dividers are used to generate RF signals. One is in the 2830.5MHz LO Generator, where 2856MHz is divided to generate 25.5MHz. The 25.5MHz is used to generate the 2830.5MHz LO and the 102MHz clock. The other place a division occurs is with the drive laser, which locks to 476MHz and pulses at 119MHz. The PADs will be used to monitor the phases at in slow loops and supply alarm signals if the phases go out of tolerance.

If the 25.5MHz generator looses synchronization, it will show up in the Sector 21 phase monitor. The RF control PAC for the 2856MHz signal, which feeds the 2830.5MHz generator, can be rotated an integral number of 2856MHz cycles to regain synchronization.

If there is a loss of synchronization with the laser, the difference in PAD readings from the laser 119MHz and linac 119Mhz will change by 476MHz cycles. A change in the synchronization of the 25.5MHz used to generate the 102MHz clock will show up in both reading the same, although the clock with respect to the trigger may change the difference reading. **It is important to check that the 25.5MHz phase has not changed before correcting the laser phase.** The laser phase is corrected by rotating the laser reference PAC by an integer number of 476MHz cycles.

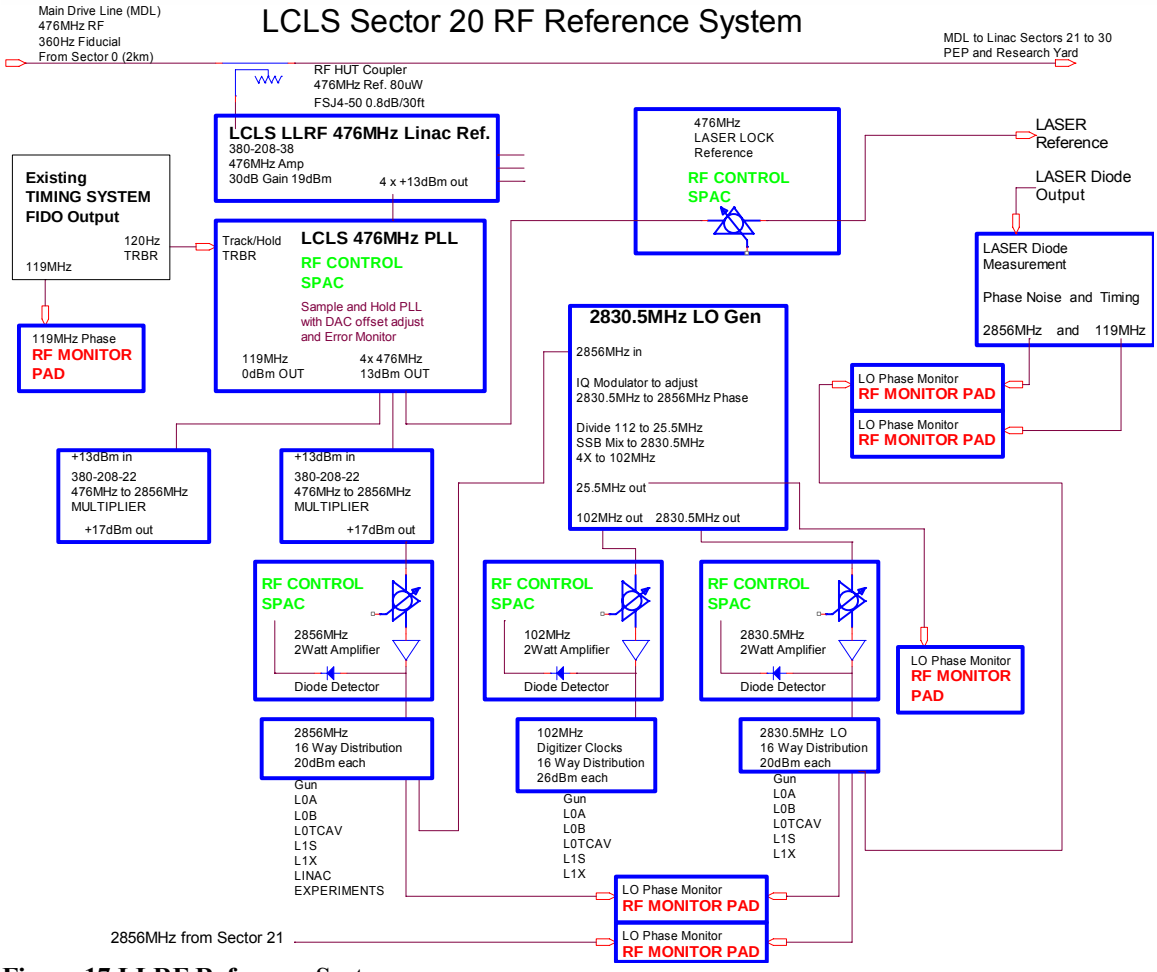


Figure 17 LLRF Reference System

A high level application will be required to rotate the phase of the reference system PACs by one full RF cycle, 360 degrees.

A second high level application will be required to display an FFT of the 64k sample points of the reference system PADs.

6.3 High level applications needed for PAC calibration

The PAC has a calibration mode where single cycle of sine and cosine waveforms are loaded into the 2048 sample I and Q waveform memory. The memory can be continuously read out as a circular buffer to create a circle in IQ space. When connected to the RF IQ Modulator it becomes a Single Side Band (SSB) modulator.

Calibration of the IQ modulator involves centering of this circle by use of I and Q offsets and suppression of the opposite side band by use of I and Q gains. The phase relationship between I and Q is calibrated in the lab and fixed by changing cable lengths to suppress

the opposite side band. Further setting of the I and Q offsets can be done by setting the input waveforms to zero and suppressing any feedthrough of the fundamental frequency.

This process will initially be done by use of a spectrum analyzer looking at the PAC output. A high level application can automate this process by reading 64k samples from the PAD in calibration mode and fitting the data to a circle to determine offsets. The eccentricity of the circle can be measured and gain of I or Q adjusted. An FFT of the PAD signal can be taken and the offsets adjusted to minimize the fundamental feedthrough. The gain can then be adjusted to minimize the opposite side band.
A final adjustment on offsets can be made by setting the PAC waveforms to zero and adjusting the I and Q offsets to minimize the fundamental power level. The fit residuals of data to a circle can be used to determine the level of nonlinearities in the PAC. Levels above a "to be determined" threshold will alert the operator to a bad calibration.

6.4 High level applications needed for PAD testing

6.4.1 Lab tests

Cross talk, SNR, Noise floor

The PAD will be set up with a 102MHz clock. A 25.5MHz signal, -1dBFS, locked to the clock, will be used to connect to channels 0 to 3, one at a time and four readings of 64k samples from each channel taken. Non-signal inputs will be terminated with 50ohm loads. FFTs will be done on each of the 16, 64k sample, sets. The FFT will not require windowing since the signal is a subharmonic of the clock. Any DC offset will be measured and then removed before the FFT.

In each of the four data sets, the following will be analyzed by doing an FFT on each of the 4 channels:

- Cross talk from the signal channel to the other 3 channels will be taken from the sum of the 2 25.5MHz signal lines on each of the 3 non-signal channels and compared the 25.5MHz signal level on the channel with the signal.
- Noise floor on all three channels will be recorded by subtracting out the 25.5MHz point and the 51MHz point integrating over 51MHz, to get Noise level -3dB, and dividing by 51MHz, to get SSB noise floor.
- Signal level will be taken as the sum of the two 25.5MHz lines in the FFT.
- Second harmonic content will be taken as the 51MHz line.

Items recorded for each channel will be Signal level, Channel to channel cross talk, Noise Floor, and noise level.
In the time domain the I, Q, -I, and -Q values will have averages and standard deviations taken and recorded.

Linearity

The linearity will be measured by a sine wave histogram test. All four channels of the board can be done at the same time. The data set size will need to be between 2M and 64M points depending on the level to which we want to measure the nonlinearities.

An asynchronous, wrt the 102MHz clock, low noise sine wave between 1MHz and 25.5MHz, at about full scale, will be split 4 ways and used to drive each channel. A detailed plan for this will be worked out. The effect of creating a histogram from multiple data sets needs to be evaluated.

7 Data throughput

Assuming the operational mode RUNNING and 4 channels of PAD data running the RF WF algorithm, the amount of data to be transferred to the VME is:
(two 16-bit integers + packet overhead) * 4 channels * 30 Hz = 480 bytes/sec + overhead

Assuming the operational mode RUNNING, the amount of data to be transferred between the VME and each PAC is:

(two 16-bit integers + packet overhead) * 30 Hz = 120 bytes/sec + overhead.

From Figure 1 and Figure 2, there are 15 PADs and 6 PACs and 1 (laser) SPAC used in fast feedback. The total throughput is: 480 * 15+ 120 * _____ = _____ bytes/sec. This number is high because some PADs don't use all 4 channels and some send a smaller dataset.

8 Commissioning Test Plan

8.1 Pre-beam, Pre-high-power, LLRF Commissioning

Test RF Cables - Measure attenuation
- Manpower - Kly Eng, AMRF
- PreReq - RF Cables Installed.

Low Level tests and calibration PACs and PADs
- Manpower - SWE, Kly Eng, AMRF, Stanek
- CW lab PAC calibration
  - PreReq - PADs and PACs Chassis Complete
    - Operational Temp determined
  - Set offsets, gain, phase
- Installation of PACs and PADs
  - PreReq - PADS and PACs tested
  - LLRF Racks installed
  - Water System installed
  - Trigger system in place
  - AC Rack power available
- Installation of Solid State Sub-Boosters (SSSB)
- Installation of RF VME Crate
- PreReq - Installation of network switches
- Get devices booting from afsnfs2
- test VME connectivity to PAD by sending I and Q avgs.
- Connection of PADs, PACs, and VME IOCs to network
- Initial Set-up of PAC triggers
  - Align 119MHz trig to 102MHZ clocks for PACs and PADs
- PAD Calibrations

Enter channel calibration factors (APCs)
PAC Calibration
Calibration with spectrum analyzer
Calibration with PAD channel
Phase Noise Measurements
Manpower - SWE, Kly Eng, Laser Group
Prereqs - RF Distribution system installed
102MHz Clock
2830.5MHz LO
2856MHz RF
Laser Lock to RF

8.2 High Power RF - no beam

Timing System setup
Manpower - SWE, Kly Eng, AMRF, Stanek
Line up PAC and PAD triggers to existing modulator triggers
Adjust PAC waveforms for 6 Klystron stations
Adjust PAD window length and offset to fit waveform
Commission local Feedback loops
Manpower - SWE, Kly Eng, AMRF, Ops
See Commissioning plans for local loops - no beam
Gun Tune
Gun Phase
Gun Amplitude
L0A Phase
L0A Amplitude
L0B Phase
L0B Amplitude
Tcav Phase
Tcav Amplitude
L1S Phase
L1S Amplitude
L1X Phase
L1X Amplitude
Test Standby Timing and BCS functions

8.3 High power RF - with Beam

Timing System setup
Manpower - SWE, Kly Eng, AMRF, Stanek
Adjust PAC and PAD triggers to align waveforms to beam time
Note: 119MHz PAD/PAC triggers must move in increments of 14 ticks
to keep all phases aligned (~117.65nS)
PAD window must move in increments of four 102MHz cycles
to keep phase reading the same. (~39.2nS) increments of
9.8nS will cause 90 degree phase shifts in readings
Commission local Feedback loops
Manpower - SWE, Kly Eng, AMRF, Ops

See Commissioning plans for local loops - with beam
Gun Phase - Phase to beam (Rotate phase to get max beam energy)
Gun Amplitude - Check Cal (RF power to maximum energy gain)
L0A Phase - Phase to beam
L0A Amplitude - Check Cal
L0B Phase - Phase to beam
L0B Amplitude - Check Cal
Tcav Phase - Phase to Beam
Tcav Amplitude - Check Cal
L1S Phase - Phase to Beam
L1S Amplitude - Check Cal
L1X Phase - Phase to Beam
L1X Amplitude - Check Cal

8.4 Frequently asked questions (or ones that should be):

When timing changes - does phase change also?
For PAD, phase readings can jump 90degrees, Actual phase does not change.
For PAC, the waveform will shift in time
How do we insure phase relationships between IF Clock and RF remain constant?
Check timing alignment procedures 102MHz Clock vs 2830.5MHz LO vs 119MHz to tell if phase has changed.

9 Post-commissioning plans

Second ethernet port of PAD and PAC will be used to improve the speed of the data transfer (PAD average I and Qs to VME phase and amplitudes to PAC corrected I and Qs) at 120 Hz. In June, 2006, we measured data transfer time (PAD -> VME -> PAC) to be 3.5 ms for two 16-bit integers.

Appendix A PAD Measurements

PAD TESTs

May 8, 2006

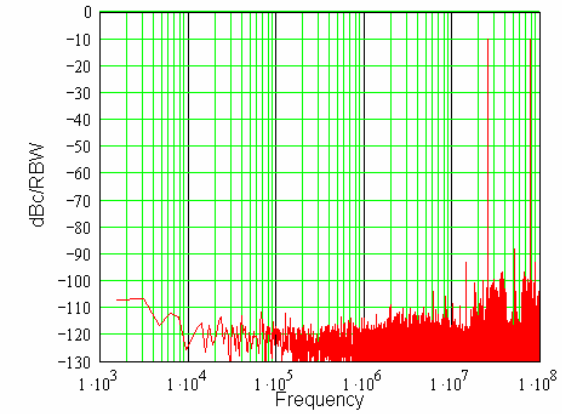
A low noise 25.5MHz signal was generated by dividing down 2856MHz. The 25.5MHz was split and half quadrupled to 102MHz. The 102MHz was used for the clock input and the 25.5MHz was used as a signal input to the 4 channel ADC board. The power levels for the 102MHz was +20dBm and +3.6dBm for the 25.5MHz. The signal level is about -6dBFS (Full Scale) of the ADC. Four 65k points of data sets were taken with the signal moved from channel to channel. For each data set the FFT for each channel is shown below. Channel to channel cross talk and signal to noise ratios (SNR) are measured for each data set.

Summary

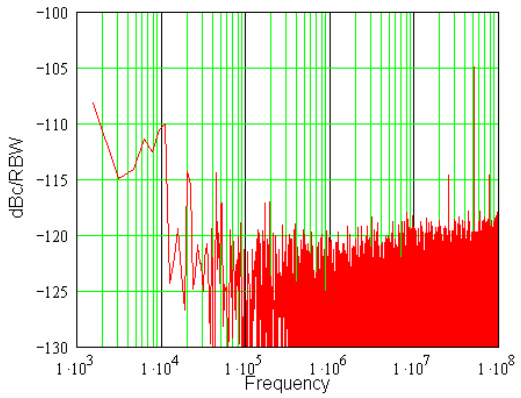
The SNR is better than 63dB on all four channels as measured. If scaled to the ADC full scale this would be 69dBFS. It looks like the signal may have noise levels limiting the measurement, since it looks like the noise floor is raised in the signal channel from -79dB to about -70dB. If this is the case the board may be able to achieve 79dBFS SNRs. There is also the possibly that the board layout and/or power supply connections contributes to this raised noise floor. Further study will be done although the board will work as is for the RF system.

Channel to Channel cross talk is in all cases better than -100dB at 25.5MHz.

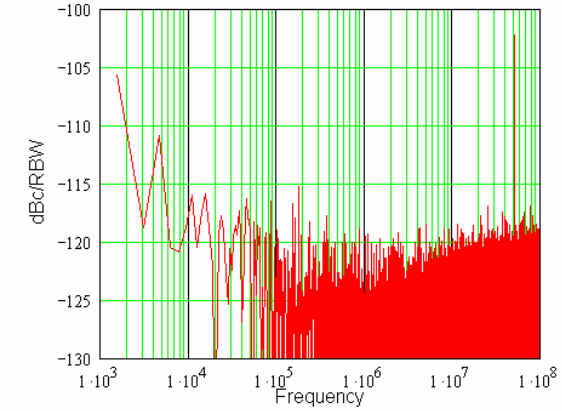
Data set 1 : 3.6dBm into Channel 0



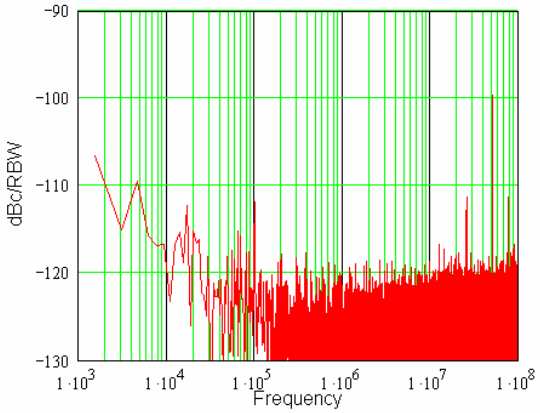
RBW=1556Hz : Channel 0 : Channel 0 signal = +3.6dBm
File: dayle315755836.dat



RBW=1556Hz : Channel 1 : Channel 0 signal = +3.6dBm
File: dayle315755836.dat



RBW=1556Hz : Channel 2 : Channel 0 signal = +3.6dBm
File: dayle315755836.dat

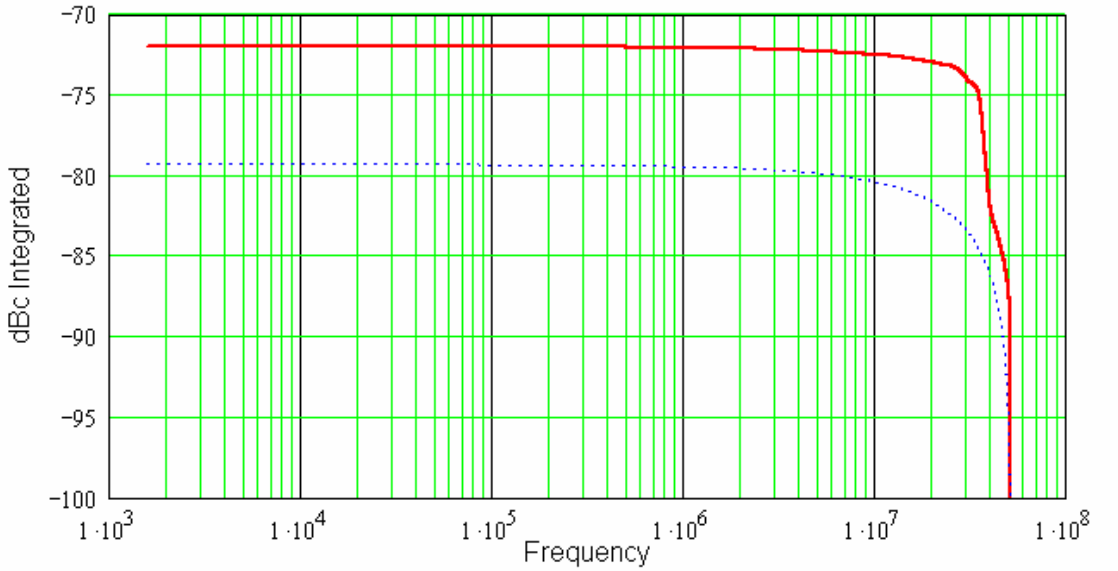


RBW=1556Hz : Channel 3 : Channel 0 signal = +3.6dBm
File: dayle315755836.dat

Channel 0 data: Signal = -7.1dB Noise Level = -72.1dB
Channel 1 data: Signal = -112dB Noise Level = -79.3dB
Channel 2 data: Signal = -114dB Noise Level = -79.3dB
Channel 3 data: Signal = -111dB Noise Level = -79.2dB

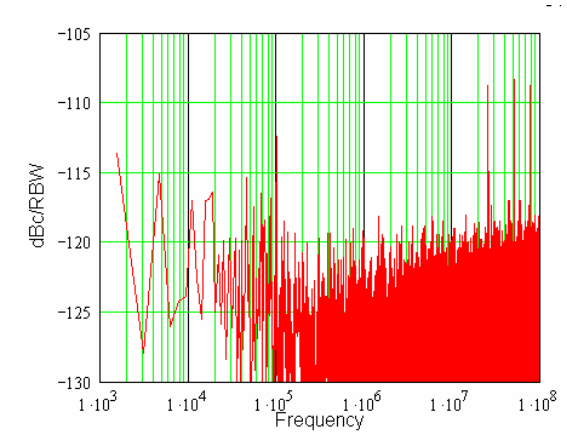
Integrated Noise Levels

The below plot shows the integrated noise levels of both the signal, channel 0, with the signal removed, red, and the adjacent channel, channel 1 in the same data set.

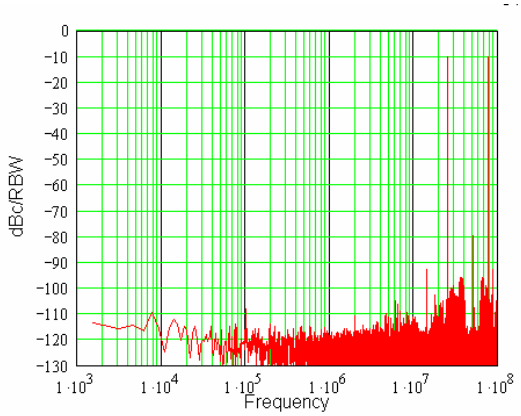


The plot shows an overall increase in noise of channel 0, which could be due to the signal having a higher noise level. The sharp increase between 35MHz and 40MHz can also be seen as an increase in the noise floor at these frequencies in the spectral plot for channel 0.

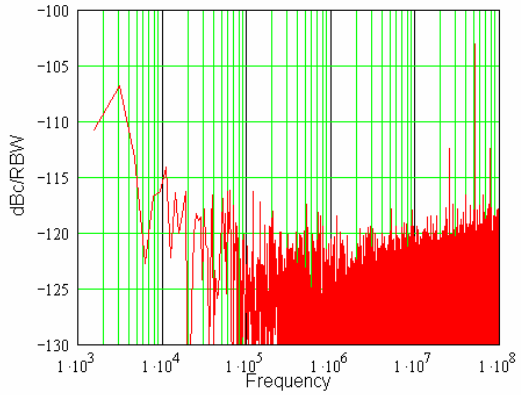
Data set 2 : 3.6dBm into Channel 1



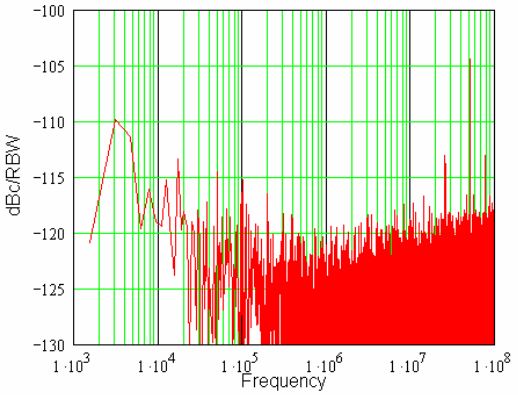
RBW=1556Hz : Channel 0 : Channel 1 signal = +3.6dBm
File: dayle315776048.dat



RBW=1556Hz : Channel 1 : Channel 1 signal = +3.6dBm
File: dayle315776048.dat



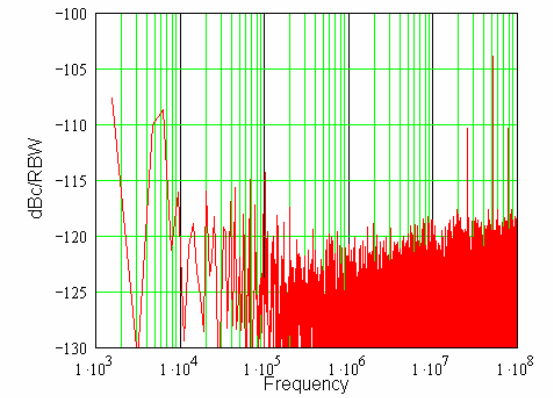
RBW=1556Hz : Channel 2 : Channel 1 signal = +3.6dBm
File: dayle315776048.dat



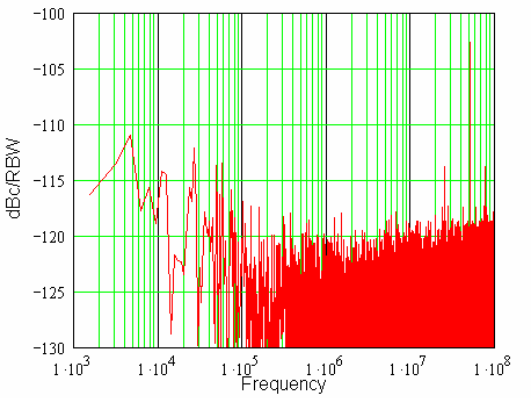
RBW=1556Hz : Channel 3 : Channel 1 signal = +3.6dBm
File: dayle315776048.dat

Channel 0 data: Signal = -106dB Noise Level = -79.3dB
Channel 1 data: Signal = -7.2dB Noise Level = -70.6dB
Channel 2 data: Signal = -109dB Noise Level = -79.3dB
Channel 3 data: Signal = -114dB Noise Level = -79.2dB

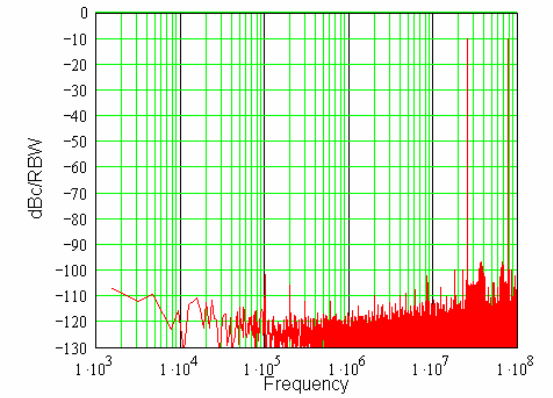
Data set 3 : 3.6dBm into Channel 2



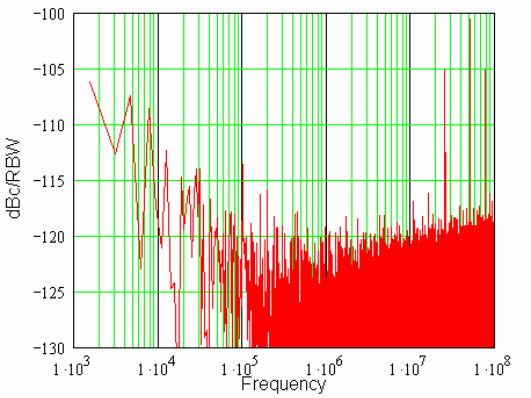
RBW=1556Hz : Channel 0 : Channel 2 signal = +3.6dBm
File: dayle315776147.dat



RBW=1556Hz : Channel 1 : Channel 2 signal = +3.6dBm
File: dayle315776147.dat



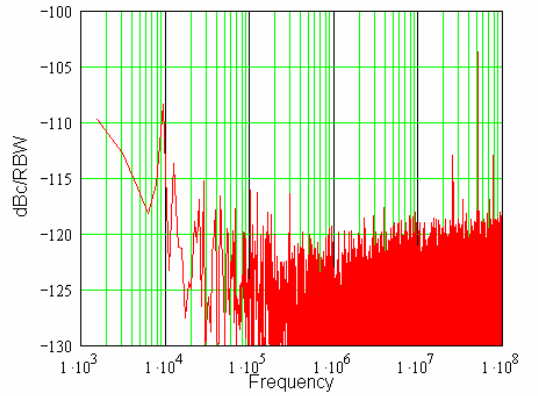
RBW=1556Hz : Channel 2 : Channel 2 signal = +3.6dBm
File: dayle315776147.dat



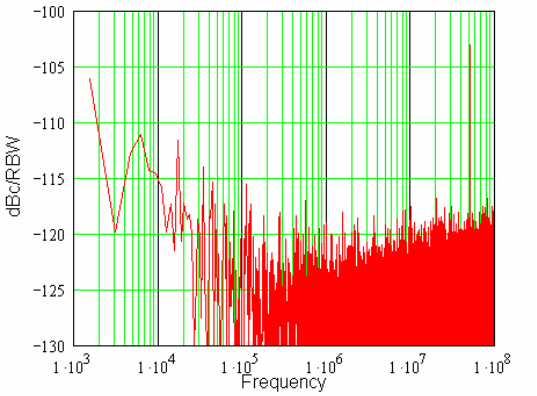
RBW=1556Hz : Channel 3 : Channel 2 signal = +3.6dBm
File: dayle315776147.dat

Channel 0 data: Signal = -107dB Noise Level = -79.2dB
Channel 1 data: Signal = -111dB Noise Level = -79.3dB
Channel 2 data: Signal = -7.1dB Noise Level = -70.4dB
Channel 3 data: Signal = -102dB Noise Level = -79.1dB

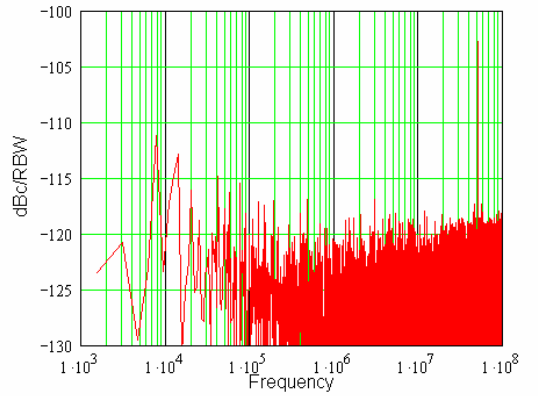
Data set 4 : 3.6dBm into Channel 3



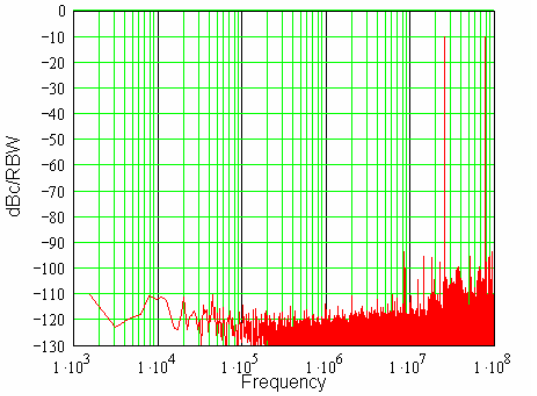
RBW=1556Hz : Channel 0 : Channel 3 signal = +3.6dBm
File: dayle315776216.dat



RBW=1556Hz : Channel 1 : Channel 3 signal = +3.6dBm
File: dayle315776216.dat



RBW=1556Hz : Channel 2 : Channel 3 signal = +3.6dBm
File: dayle315776216.dat



RBW=1556Hz : Channel 3 : Channel 3 signal = +3.6dBm
File: dayle315776216.dat

Channel 0 data: Signal = -110dB Noise Level = -79.3dB
Channel 1 data: Signal = -121dB Noise Level = -79.4dB
Channel 2 data: Signal = -121dB Noise Level = -79.3dB
Channel 3 data: Signal = -7.1dB Noise Level = -70.5dB