Research and Development of a Pipeline Readout System for the Belle Silicon Vertex Detector

Yu Nakahama
Department of Physics, University of Tokyo

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Abstract

The goal of the Belle experiment, after the discovery of CP violation in B meson system, is to search for the new physics beyond the Standard Model through much larger number of B meson decays. In particular, the precise measurements of time-dependent CP asymmetries in rare B decays are of great interest since they are sensitive to contribution from the new physics.

The Silicon Vertex Detector (SVD), which detects the B meson decay vertices and provides the information of their positions, has been a key device in the experiment. The high efficiency of the vertex finding and the superb position resolution of the decay vertices are essential to all time-dependent CP analyses.

As the luminosity of KEKB accelerator further increases (with more beam currents and with new cavities), we expect the beam-induced background would also increase. In the worst-case scenario, the number of the hits in the SVD could become $\sim$30 times more than the present value and SVD would no longer work.

To cope with the harsh background and not to compromise the superb performance, we have developed a fast pipelined readout system for the Belle SVD, using the new readout VLSI, APV25, developed for the CMS experiment at LHC. We have designed APV25 readout scheme (the waveform sampling and reconstruction) for SVD system. We have also developed a new occupancy and data reduction method using the reconstructed event timing information.

We have performed the beam test and the simulation to verify the performance of this readout scheme. We find that the occupancy of the SVD will be reduced by a factor of 12 due to a fast analog signal (a pulse peaking time of 50 ns) and by an additional factor of 3 with the newly-developed event timing reconstruction method. We also ensure that the reduced data transfer rate satisfies the bandwidth of the backend data acquisition (DAQ) system.

Based on this study, we conclude that this new readout system will withstand at least 30 times larger background than the current system does, which satisfies the requirements of the now-planned SuperKEKB with a luminosity of $5 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

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Chapter 1

Introduction

The Standard Model (SM) contains three generations of quarks and leptons, and their interactions are mediated by gauge bosons according to the $SU(3)_C \times SU(2)_L \times U(1)_Y$ gauge field theory. Over the past thirty years, the SM has been confirmed by many precise experimental measurements.

There are, nevertheless, some reasons why the SM is not the complete theory that can explain all the questions in the particle physics: first of all, it includes too many parameters, secondly, the hierarchy of quark and lepton masses and the flavor mixing matrices suggest that some hidden mechanism occurring at a higher energy scale governs their pattern. Many theories beyond the SM are suggested [1, 2] and are waiting for the new experimental discoveries. The most direct way to discover a new physics phenomenon beyond the SM is to construct an energy-frontier collider and accumulate beam collision data at TeV energy scale in which new heavy particles may be directly produced. (For this purpose, Large Hadron Collider (LHC) is under construction and International Linear Collider (ILC) is also planned.)

Another way to discover a new physics phenomenon is to perform precise measurements on the physics processes that have small amplitude that is unambiguously predicted by the SM. The Flavor Changing Neutral Current (FCNC) processes in the B meson decays, such as the hadronic $b \to s(d)q\overline{q}$ decays, the radiative $b \to s\gamma$ decay and the semileptonic $b \to s\ell^+\ell^-$ decay, are suitable to this end [3]. All of these processes are suppressed in the SM by the GIM mechanism, and the effects of the new physics may be relatively enhanced. The higher luminosity B factory makes it accessible and the comprehensive studies of B meson decays in a clean e^+e^- environment provide the ideal solution for this purpose.

The Belle experiment [4] started in 1999 and has since studied the nature of CP violation through B meson decays with a large statistics [5] that no other experiments have ever achieved. The KEKB accelerator has achieved a peak luminosity of $1.6 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and the Belle detector has accumulated an integrated luminosity of 500 fb^{-1} by the end of December in 2005.

To probe the new physics beyond the SM, we need multiple precise measurements on the CP asymmetries for the rare B decay modes that have small branching ratios. The sufficient statistics for such measurements corresponds to a large integrated luminosity of $O(\mathrm{ab}^{-1})$ or more. To accumulate such a large data sample, the KEKB increaes the luminosity by storing higher beam currents and employing new cavities, which could cause excessive beam-induced background.

The Silicon Vertex Detector (SVD) is the crucial device in measurements of the time-dependent CP asymmetries. It measures the distance between two B decays, from which the time difference between the two decays is inferred. The resolution of the measured vertices

must be good enough to measure the $B^0\overline{B^0}$ mixing oscillation.

According to the luminosity increase of the KEKB as planned, the occupancy of the SVD innermost layers will go up to 30 % in 2008 due to the beam-induced background. If we keep using the current SVD, the SVD would not achieve its performance enough. To shorten the process time per event and to avoid the dead time due to the current *track* and *hold* readout, a faster readout system with pipeline memory is necessary.

We have developed a fast pipelined readout system using the new readout chip (APV25), which is designed for the CMS Silicon Tracker at LHC. We plan to adopt this readout to the upgraded SVD (SVD2.5), which will be installed in 2007.

Although APV25 has many good features that are suitable for use at the SVD, we have to modify the readout scheme due to the beam structure of KEKB. We improved an APV25 operation mode (Multi peak mode) so as to suit for the SVD by changing the trigger control parameters of APV25. We sample a part of the waveform of the shaper output and reconstruct it by an external processing. We have evaluated this APV25 readout scheme (Waveform sampling and its reconstruction) using the APV25 test system in the beam test at KEK 12GeV-PS. We have studied the waveform reconstruction methods.

At now-planned SuperKEKB with a luminosity of $5\times10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$, we require an occupancy reduction factor of 30. The trigger rate is expected to be 20 times higher than the current one and the data transfer rate will exceed the backend DAQ bandwidth. We have developed a new sophisticated occupancy and data reduction method using the reconstructed event timing. Using the beam test data and the simulation, we have studied how we apply the scheme throughout the entire readout system at the various background levels. We have also showed the tolerable background level of the SVD entire system.

In this thesis, we show the APV25 readout scheme for the SVD, and the performance evaluation of it. Furthermore, we describe the new occupancy reduction method using event timing information and discuss the performance of this readout system. We describe the brief introduction of the Belle experiment in Chapter 2, the SVD Upgrade in Chapter 3, the performance evaluation of the APV25 readout scheme for SVD in Chapter 4, the new occupancy reduction method using event timing information in Chapter 5, the performance of the entire readout system at the various background levels and the discussion of the SVD system with APV25 readout in Chapter 6 and the conclusion in Chapter 7.

Chapter 2

Belle experiment

The Belle experiment is designed to study the physics on CP asymmetries of B meson system and now it searches for New Physics effects through large number of B meson decays. The experiment is performed at the High Energy Accelerator Research Organization (KEK) in Japan, and utilizes the energy-asymmetric e^+e^- KEKB collider to produce B mesons. The decay products of B mesons are collected by the Belle Detector. To further search for New Physics effects precisely through the rare B decays, the upgrades of the accelerator and the detector are proposed as SuperKEKB project. The SuperKEKB aims 30 times higher luminosity than the current KEKB.

In this chapter, we introduce the physics motivation of the Belle experiment, then we describe the experimental apparatus, the KEKB accelerator and the Belle Detector. We also show the overview of the upgraded Belle Detector for SuperKEKB.

2.1 Physics Motivation

We briefly describe two major physics motivations. The details are described in elsewhere [6].

- CP asymmetries in a FCNC loop diagram: $b \to sq\overline{q}$, $b \to dq\overline{q}$.
  The measurement of the time-dependent CP-asymmetries on the pure $b \to sq\overline{q}$ and $b \to dq\overline{q}$ processes and the comparisons of that on the $b \to c\overline{c}s$ process like $B \to J/\psi K^0_S$ decay, is one of the powerful tools to probe the new physics beyond the SM. The $B \to \phi K^0_S$ decay, which is purely dominated by the $b \to ss\overline{s}$ transition described by the FCNC loop diagram, which is shown in Figure 2.1, is especially a theoretically-clear and sensitive probe of new CP-violating phase from physics beyond the SM. There is no simple phenomenology which can explain these anomalous values without introducing physics beyond the SM. It is possible to have the New Physics effects in the loop by replacing the t quark or W boson with some other unknown particle. In the Belle, a series of studies has been launched to understand this anomalous behavior of $B \to \phi K^0_S$ decay experimentally [7]. Figure 2.2 shows the expected total errors on ΔS and ΔA as a function of integrated luminosity. With $O(\mathrm{ab}^{-1})$ sample data, the total errors are expected to be $O(10^{-1})$. Figure 2.3 shows a comparison between time-independent CP asymmetries in $B^0 \to J/\psi K^0_S$, which is dominated by the $b \to c\overline{c}s$ tree process, and $B^0 \to \phi K^0_S$, which is governed by the $b \to s\overline{s}s$ FCNC loop process. It demonstrates how well a possible new CP phase can be measured. Measurements with larger sample data are required to conclusively establish the existence of a new CP-violating phase beyond the SM.

  If we have much larger sample data, CP asymmetries in $b \to dq\overline{q}$, which is rarer decay and more sensitive to the New Physics effects than any other mode [8], will become within

our reach. For example, the $B \to K^0_S K^0_S$ decay, which is purely dominated by the $b \to ds\overline{s}$ and is observed in the summer of 2005, is the most promising with $O(\mathrm{ab}^{-1})$ sample data.

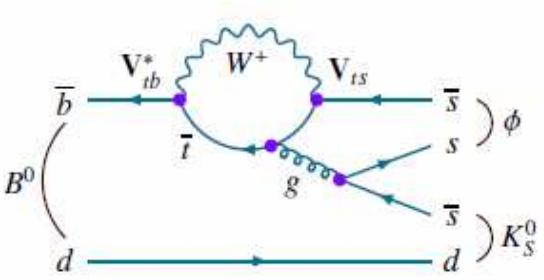

Figure 2.1: Feynman diagram in the $B^0 \to \phi K^0_S$ decay. If only SM particles appear in this diagram, the CP violating asymmetry in this decay is $\sin 2\phi_1$.

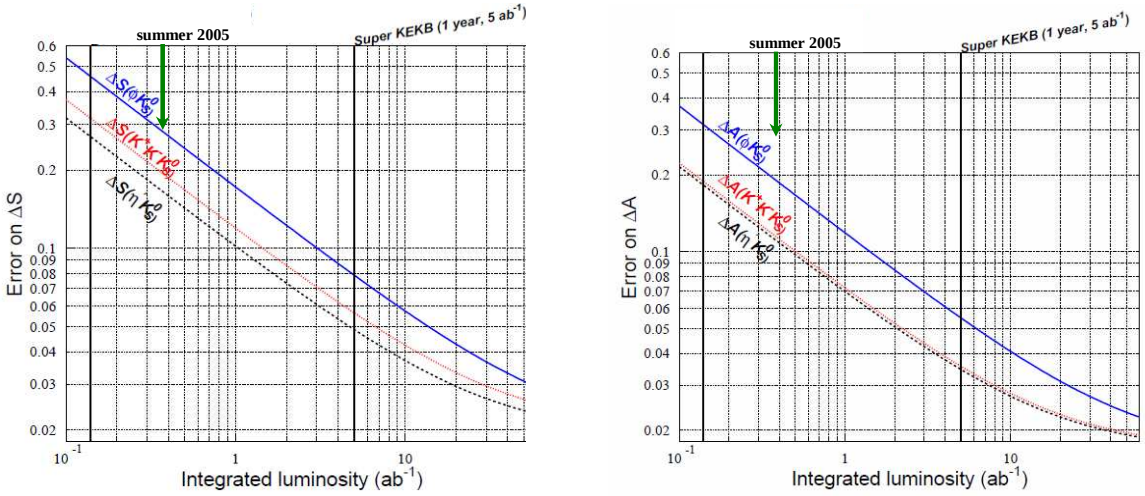

Figure 2.2: Expected total errors on ΔS (Left) and ΔA (Right) as a function of integrated luminosity.

- Correlations between the CP asymmetry parameters in the FCNC decays.
  Since the KEKB is an e^+e^- collider, the environment is clean enough to measure decay modes including π^0, γ and ν in the final state. The Belle, therefore, can measure the various CP asymmetries not only of the hadronic decays but also of the radiative decays. Theoretical studies indicate that the effects of New CP phase differ mode by mode. We *can* constrain the parameter and study which theory is appropriate by checking the correlations between different modes. Correlations among the FCNC processes constrain further the possible scenarios.

  We show one of the examples. Figure 2.4 shows the correlations between time-dependent CP asymmetries in $B^0 \to K^{*0}\gamma$ decay (radiative FCNC transition) and $B^0 \to \phi K^0_S$ decays (hadronic FCNC transition) in two representative new physics models with different SUSY breaking scenarios; the SU(5) SUSY GUT with right-handed neutrinos and the minimal supergravity model. As you can see, these two can clearly be distinguished. This

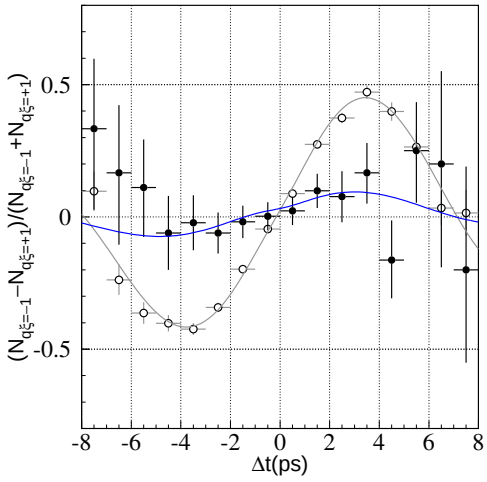

Figure 2.3: Time-dependent CP asymmetries in $B^0 \to \phi K^0_S$ and $B^0 \to J/\psi K^0_S$ decays expected with the one-year operation at the SuperKEKB (5ab^{-1}.) The world averages in August 2003 for modes governed by the $b \to s$ transition are used as the input values of $\mathcal{S}_{\phi K^0_S}$=+0.24 and $\mathcal{A}_{\phi K^0_S}$=+0.07.

demonstrates that High Luminosity B factory is sensitive to a quantum phase even at the GUT scale. If these two models have similar mass spectra, it will be very difficult to distinguish one from the other at LHC. If SUSY particles are discovered at LHC, the origin of SUSY breaking will be one of the primary themes in particle physics. High Luminosity B factory plays a leading role in such studies.

2.2 KEKB accelerator and SuperKEKB accelerator

The KEKB accelerator has two rings in a tunnel which is used for TRISTAN. The total length of the main rings is about 3 km. The KEKB factory is designed to produce as many $B\overline{B}$ pairs as possible and to aim for higher luminosity. Beam energies are chosen to be 8.0GeV for the electron and 3.5GeV for the positron, so that the center of mass energy becomes equal to the Υ(4S) resonance energy [1] and the center of mass system is boosted by $\beta\gamma \simeq 0.425$ that corresponds to the flight length of the B meson decays of approximately 200μm [2]. Figure 2.5 shows configuration of the KEKB accelerator.

Now the KEKB factory routinely produces ~1.0fb^{-1} per day and the integrated luminosity exceeds 500fb^{-1} data [3]. The peak luminosity is 1.627×10^{34}cm^{-2}s^{-1}. KEKB people will plan to install crab cavities, which effectively creates a head-on collision, for both rings in the early 2006. Peak luminosity will be more than doubled. The integrated luminosity will reach 1 ab^{-1} or more in 2008.

[1] For this reaction, the Υ(4S)$\to B\overline{B}$ cross section is 1.05nb. At the same energy, the $e^+e^- \to q\overline{q}$ (q=u, d, s, or$c$) continuum process has a cross section of 3.7nb.

[2] The typical flight length of a B meson in the Υ(4S) center of mass frame is only 2μm which is not sufficient for a time-dependent CP analysis.

[3] The integrated Luminosity of the KEKB for the Belle is 525.8fb^{-1}, while that of the PEPII for the BaBar [9] in U.S.A. is 324.8fb^{-1} in 12/31/2005.

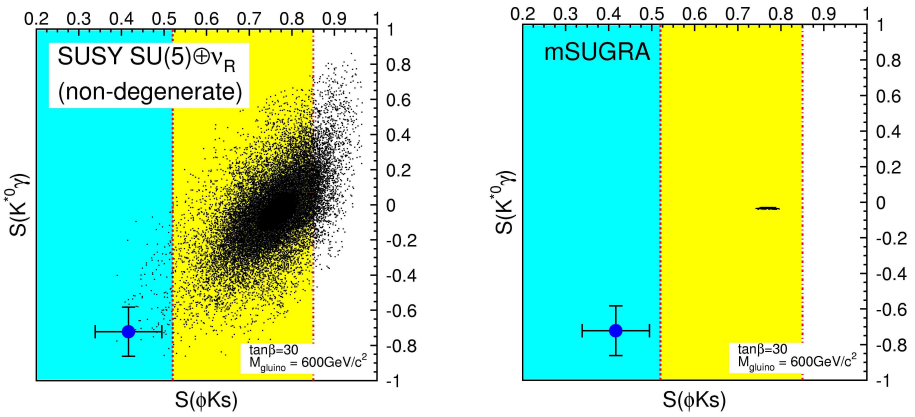

Figure 2.4: Correlation between time-dependent asymmetries of $B \to \phi K^0_S$ and $B \to K^*\gamma$. $S_{K^*\gamma}$ and $S_{\phi K^0_S}$ for various parameters in (left) SUSY SU(5) with right-handed neutrinos (the non-degenerate case), and (right) mSURGA. Circles with error bars indicate an expected result from a certain parameter set in the SU(5) SUSY GUT, where the error bars are obtained at 5ab^{-1}. A present experimental bound at 2σ (3σ) level is also shown by the dashed (dot-dashed) vertical line.

Table 2.1: The machine parameters of the KEKB and the SuperKEKB.

Parameters	KEKB	SuperKEKB
Peak Luminosity [$\times 10^{35}$cm$^{-2}s^{-1}$]	0.15	5
$B\overline{B}$/year	1×10^8	5×10^9
Beam current: I [A]	1.8 / 1.34	9.4 / 4.1
beam-beam parameter: ξ	0.057	0.19
Vertical β at IP [mm]	6.5 / 6.2	3.0 / 3.0
Vacuum [10^{-7} Pa]	5	$\sim$1.5
Crossing angle [mrad]	$\pm$11	0 (crab crossing)

To further extend reach for the new physics search, SuperKEKB is planned. The design luminosity of the SuperKEKB is 5×10^{35} cm^{-2}s^{-1}. The SuperKEKB will be constructed by re-using most of the components of the KEKB, in particular the ring magnets and klystrons used to supply RF power to the cavities. But, there are many components that need to be modified or newly developed; RF system, vacuum system, feedback system and so on. The machine parameters of the KEKB and the SuperKEKB are listed in Table 2.1 [4]. Figure 2.6 shows the plan of the KEKB accelerator upgrade.

2.3 Belle Detector

2.3.1 The current Belle Detector

The Belle detector is a 4π spectrometer designed for the study of CP violation in the B meson system and is required to measure decay vertices precisely. The Belle detector consists of 7 sub detectors, from an inner part, a silicon vertex detector (SVD), a 50-layer central drift chamber

[4] Luminosity: $L \propto \frac{I\xi}{\beta}$

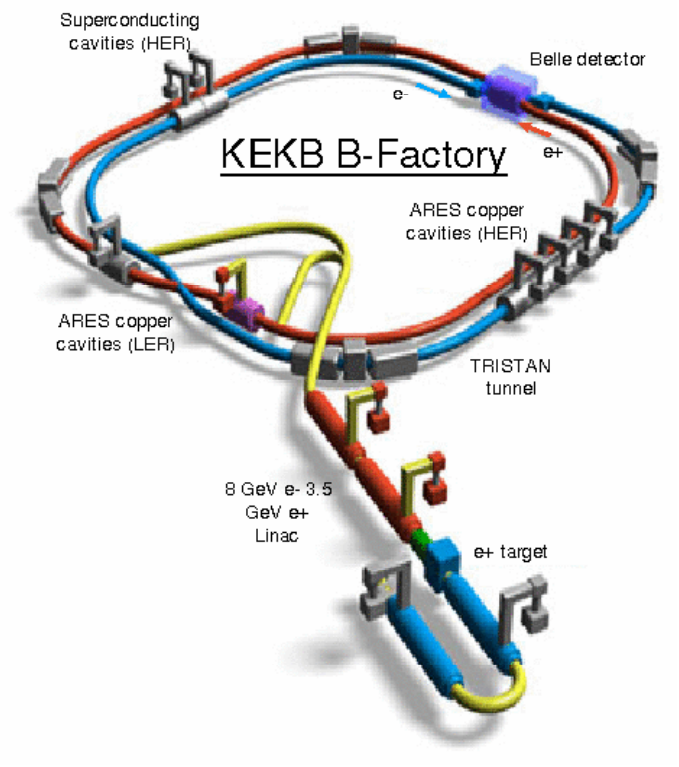

Figure 2.5: KEKB accelerator system.

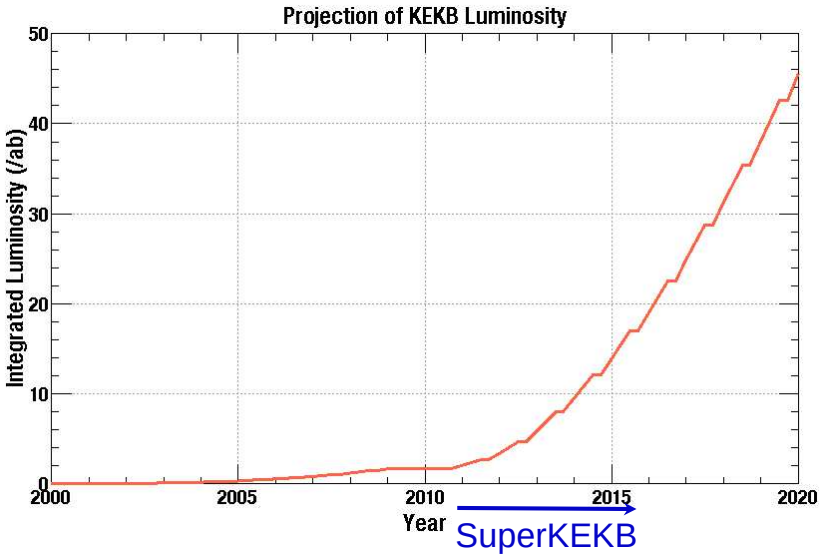

Figure 2.6: KEKB accelerator upgrade plan. The integrated luminosity as a function of year.

(CDC), an array of aerogel threshold Cerenkov counters (ACC), time of flight scintillation counters (TOF), an electromagnetic calorimeter composed of CsI(TI) crystals (ECL), a K_L^0 and muon detector (KLM), and a pair of extreme-forward calorimeters (EFC). Figure 2.7 shows the schematic view of the Belle detector. We briefly summarize the purposes of the sub detectors and their SVD-related topics.

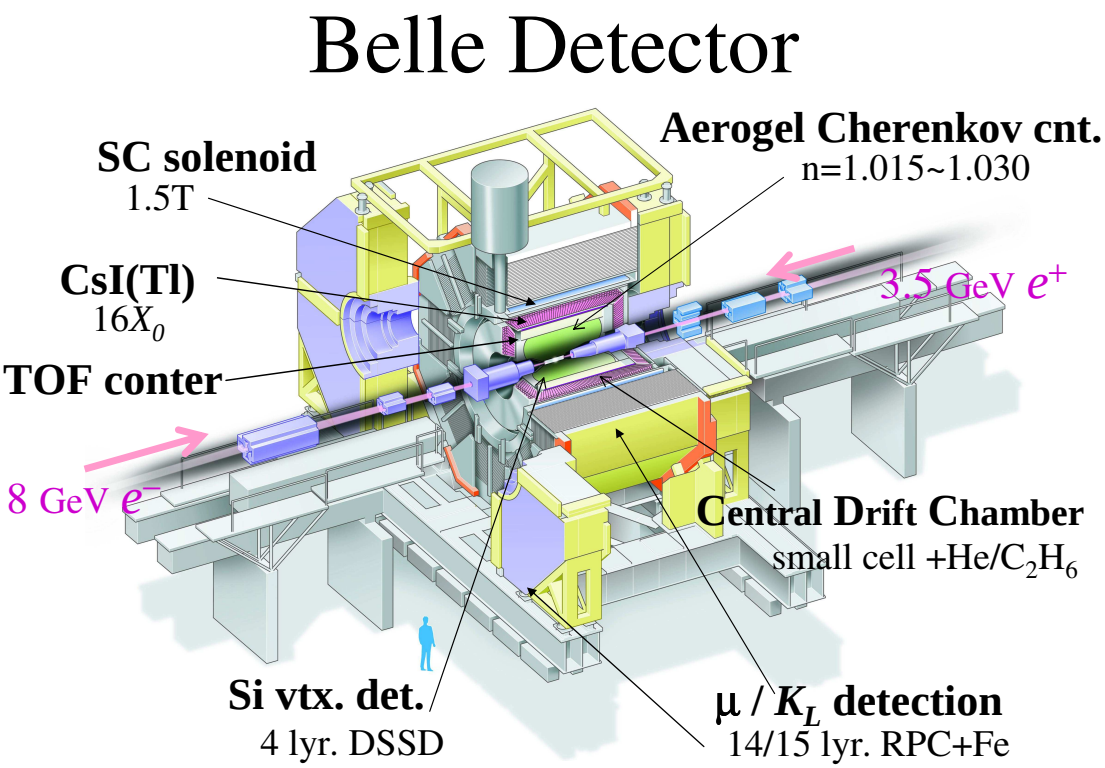

Figure 2.7: Schematic view of the Belle Detector.

- SVD

  SVD is a device that finds the vertex of charged particle tracks with precise resolution. Measurements of *CP* asymmetry parameters require the resolution of a vertex detector to be better than the average flight distance of a B meson, which is about 200 μm at the KEKB accelerator. The resolution of SVD is sufficiently good to measure this separation.

- CDC

  The main role of CDC is the detection of charged particle tracks and the reconstructions of their momenta. The momentum resolution is quite good, P_t resolution is $\sim 0.19 P_t \oplus 0.30/\beta\%$. By measuring dE/dX, CDC also gives particle identification information.

- ACC

  The main purpose of ACC is to separate kaons from pions for the momentum region in 1.2<p<3.5 GeV/c. The aerogel of the ACC is made of SiO_2 whose refractive index is n $\simeq$1.1015. By using the momentum information measured by CDC, a particle can be identified based on the information whether it emits a light or not.

- TOF

  TOF, which is made of a plastic scintillation counter, is also used for the particle identification. It has capability to identify the charged particles, whose momentum is less than 1.2 GeV/c. TOF has other sets of scintillation counters, which are used to generate the trigger signal. A pre-trigger to hold SVD signal is generated by TOF trigger.

- ECL

  The main purpose of ECL is to detect photons and is to identify of electrons from B meson decays with high efficiency and good energy resolution. ECL is made of CSI(Tl). ECL is also used for the measurement of the luminosity using Bhabha scattering. ECL covers a wide energy range from 20 MeV to 8 GeV.

- KLM

  KLM detects K_L^0s and identifies muons by measuring their positions. KLM consists of an alternating sandwich of 4.7 cm thick iron plates and resistive plate counter (RPCs) located outside the superconducting solenoid.

- EFC

  EFC measures the energy of photons and electrons at the extreme forward/backward direction outside the ECL acceptance. EFC covers $6.4^\circ < \theta < 11.5^\circ$ in the forward direction and $163.3^\circ < \theta < 171.2^\circ$ in the backward direction. EFC is made of BGO crystals in order to tolerate high radiation of photons from the synchrotron radiation and the spent particles (about 5MRad per year).

- Trigger

  The Belle trigger system mainly consists of the Level-1 hardware trigger and the Level-3 software trigger. Level-1 consists of the 6 sub detector trigger systems and the central trigger system called the Global Decision Logic (GDL). The trigger system provides the trigger signal with a fixed time of 2.2 μs after the collision. The trigger efficiency for the hadronic events is more than 99%, which meets requirements from physics analysis. The average trigger rate is about 400Hz at the luminosity of $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The current SVD system needs pre-hold trigger (so-called Level-0 trigger), which comes after 800ns from the collision. The average Level-0 trigger rate is around 2kHz and hold efficiency is $\sim$95%.

- DAQ

  The Belle Data Acquisition (DAQ) system deals with the data flow from the analog signals by the individual sub-detectors to their digitized data to save in mass storage for offline analysis. The Belle DAQ system consists of three parts: a frontend readout part, an event building part and a mass storage part. For the frontend readout part, each sub detector uses the commonly-developed FASTBUS TDC system, expect for SVD. The data from SVD are digitized by FADC and processed by a PC-based readout system and sent to the event building farm directly via the network.

2.3.2 The upgraded Belle Detector for SuperKEKB

Figure 2.8 shows the conceptual design of a detector for SuperKEKB. The major upgraded Belle detector for SuperKEKB consists of vertex detector, central tracker, particle identification detector, calorimeter, and K_L and muon detector. To maintain and to evaluate the

current performance in the higher beam-induced background environment, each sub-detector is upgraded gradually. We introduce the detail of the upgraded SVD in Section 3.2. The detail of the other sub-detectors can be found elsewhere [6].

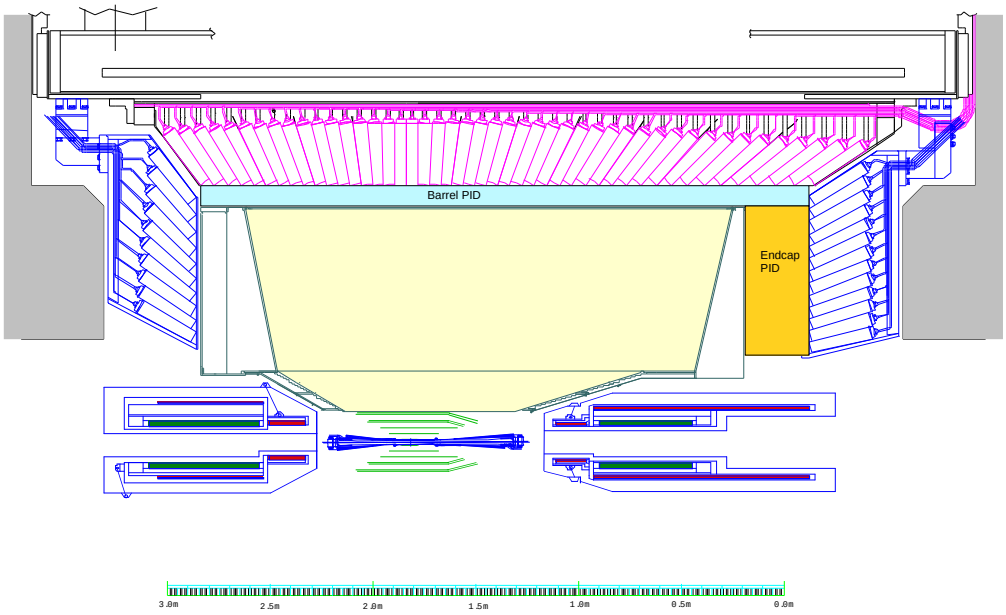

Figure 2.8: Conceptual design of a detector for SuperKEKB.

Chapter 3

SVD Upgrade

To accomplish the high performance in the coming high luminosity environment, we need to upgrade SVD. This is because, for example, the beam-induced background to the innermost layers of SVD are expected to be triple in 2008, and the performance deterioration, such as occupancy increase, is expected. The upgrade of the SVD is planned to proceed in the two steps: The first upgrade, called SVD2.5, is planned in 2007 to catch up with the gradually increasing luminosity. The second upgrade, called SVD3, is planned for the SuperKEKB.

In Section 3.1, we describe the overview of the current SVD (SVD2.) In Section 3.2, we show the overview of the upgraded SVD (SVD2.5 and SVD3.)

3.1 The current Silicon Vertex Detector (SVD2)

In this section, we describe the SVD and its performance in the current Belle experiment. We also discuss the expected deterioration of the SVD performance due to the larger beam-induced background.

3.1.1 Overview of SVD2

The SVD system has been upgraded several times since the commissioning of the Belle experiment. This is not only by the demand for replacing the damaged detectors and beampipe but also by the aim at improving the performance and the radiation tolerance. In summer of 2003, we completed a major SVD upgrade from SVD1 to SVD2 [10]. The improvements of SVD2 includes employment of the radiation-hard readout chip [1] and geometrical improvements [2].

The SVD2 consists of 4 layers of Double Sided Silicon Detectors (DSSDs.) The signal of the silicon sensor is read out by the 128ch VA1TA chip with a peaking time of 800ns, which is adjusted to be short and also to obtain good S/N. Figure 3.1 shows the schematic view of SVD2 and its characteristics are listed in Table 3.1.

The typical trigger rate is ∼400Hz and the average occupancy of the SVD is around 3 %. Under these conditions, the performance of SVD2 is good enough as summarized in Table 3.2 [3] [4].

[1] The VA1TA chip with 0.35μm for SVD2 functions up to 20 MRad, while the VA1 chip with 0.8μm for SVD1 does up to 1MRad (The maximum radiation dose accumulated in Layer-1 is 500kRad/year.).

[2] SVD extends outer for better low-p_t tracking and catch of the vertex information of more decays, and closer to the interaction point for better impact parameter resolution.

[3] p is the track momentum and θ is its incident angle with respect to the detector module.

[4] SVD hit information also help CDC tracking. The matching efficiency is defined as the probability that tracks reconstructed in the drift chamber can be extrapolated to the hits in the SVD.

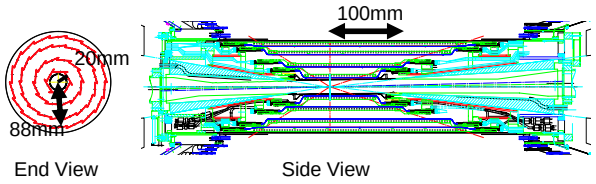

Figure 3.1: Schematic view of SVD2.

Table 3.1: Characteristics of SVD2.

Beampipe radius [mm]	15
Number of layers	4
Number of DSSD ladders in layers 1/2/3/4	6/12/18/18
Number of DSSDs in a ladder in layers 1/2/3/4	2/3/5/6
Radii of layers [mm] in layers 1/2/3/4	20.0/43.3/70.0/88.0
Angular coverage (acceptance)	$17°<\theta<150°$ (0.92)
Active area [mm^2] per sensor	76.8×25.6 (73.8×33.3 for Layer-4)
Total number of channels	110592
Strip pitch [μm] for p (z)	75 (73 for Layer-4)
Readout pitch [μm]	150 (146 for Layer-4)
Strip pitch [μm] for n ($r\phi$)	50 (65 for Layer-4)
Readout pitch [μm]	50 (65 for Layer-4)
DSSD thickness [μm]	300
Total material at θ=90° [X_0]	2.6
Readout chip	VA1TA
Readaout scheme	Track and Hold
Intrinsic DAQ dead time/event [μs]	25.6

Table 3.2: Performance of SVD2.

Parameter	
S/N	>16
Occupancy [%] in layers 1/2/3/4	10/3.5/2.0/1.5
Hit detection efficiency [%]	90
Impact parameter resolution [μm] for dz	$26.3\oplus 32.9/\ (p\beta(\sin\theta)^{\frac{5}{2}})$
Impact parameter resolution [μm] for $d\rho$	$17.4\oplus 34.3/\ (p\beta(\sin\theta)^{\frac{3}{2}})$

3.1.2 The expected deterioration of the SVD2 performance

In this subsection, we discuss the coming background condition and the expected deterioration of the SVD2 performance.

- **Expected background conditions**

  Near Future at KEKB

  The peak luminosity is expected to be more than doubled by the installation of new cavities and by the increase of the beam currents. As the luminosity increases, the beam-induced background [5] level is expected to rise and the detector occupancy is also expected to be increased as well. In the SVD, the background to the innermost layers is estimated to become three times worse in 2008.

  Future at SuperKEKB

  The luminosity level and also the background level will rise dramatically by a factor of ten or more than now. SVD are estimated to recive 20∼30 times larger beam-induced background. Figure 3.2 shows the expected event displays of the Belle experiment in the current case and in the 20 times larger background case. The SVD is in the center part like the 4 concentric circles. As you can see, the number of hits increases dramatically in the SuperKEKB case and we find it difficult to reconstruct the physics-originated tracks.

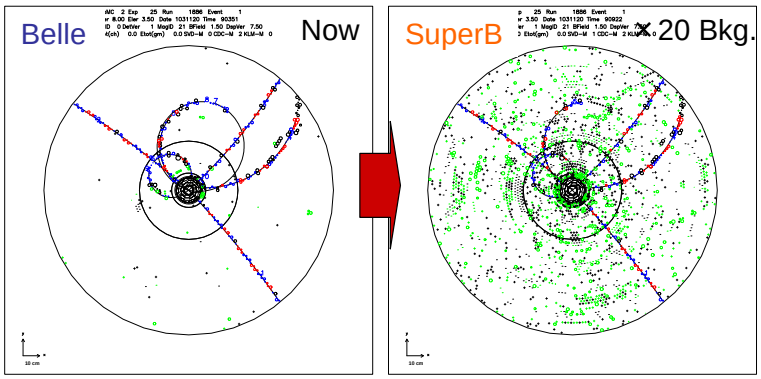

Figure 3.2: Belle event displays at the current background level and at 20 times higher one, respectively.

- **Occupancy**

  We define *Occupancy* as the number of hit channels and their neighbor channels over the number of all channels. At the current background level, the average occupancy of Layer-1 (Layer-2) is 10% (3.5%) at L_{peak}=10^{34}cm^{-2}s^{-1}. Since almost all the SVD hits are due to the beam-induced background, the occupancy increases proportional to the background level with the same sensitive area per channel in both time direction and the space direction. With the current readout system, at the triple background level, the occupancy would increase up to 30 %, and at the harsh background level as of SuperKEKB, the occupancy would almost 100% and the SVD would no longer work.

[5] SVD is affected by mainly two kinds of beam-induced background: showers from scattered beam particles by the residual gas or intra-beam scattering (Particle background) and synchrotron radiation.

Here, we discuss the degradation of the basic parameters of the SVD performance in the triple background.

- **Hit detection**
  The hit detection efficiency is defined whether hits are found in P and N sides near the extrapolated track from CDC. Figure 3.3 shows the hit detection efficiency of Layer-1 as a function of occupancy. The degradation at the triple background level is expected to be about 20%.

- **Impact parameter resolution**
  Figure 3.4 shows the impact parameter resolutions in $r\phi$ using μ pair events as a function of the Layer-1 occupancy. The degradation with the triple background level is expected to be about 15 %.

- **Vertex resolution**
  Using lower momentum $J/\psi K^0_S$ events, the expected decay length difference of B_{CP}, B_{tag} with the triple background level in Layer-1 is 104μm, which is 17% degradation from the current value of 86μm, as shown in Figure 3.5.

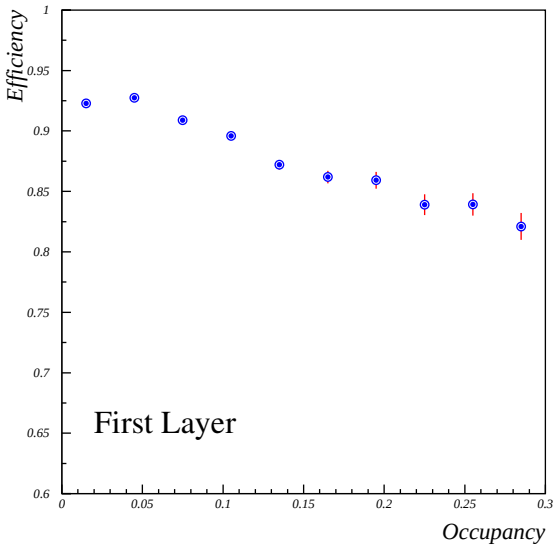

Figure 3.3: Hit detection efficiency as a function of occupancy of Layer-1.

The deterioration at the high beam-induced background level comes from the following reasons. First, the background-originated clusters are wrongly associated in tracking. Second, the background-originated hits are overlapped with the signal making wider and distorted cluster shape (Pileup events.) Occupancy should be kept below 10 %, which comes from the requirements on the charged track reconstruction analyses on the physics. The clustering and tracking software improvements [6] may help get out of the situation, but to suppress the background hits themselves and reduce occupancy, a hardware upgrade is essential.

[6] Correlations between detected charge from both sides of the DSSD can help reduce the number of hits with wrong associate clusters. Correlation between cluster size and track incident angle could also help reduce the number of background-induced hits.

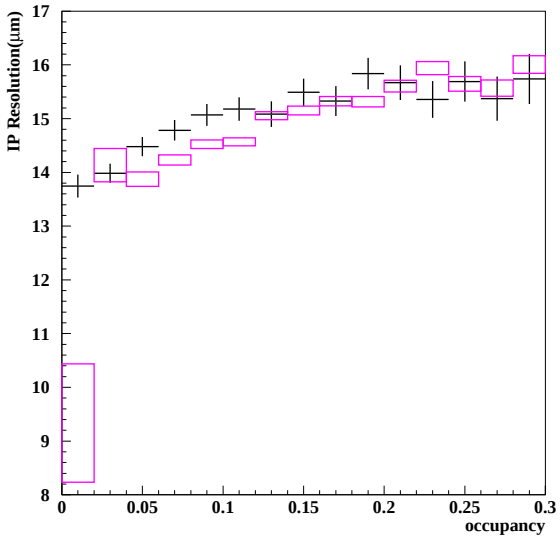

Figure 3.4: Impact parameter resolution in $r\phi$ as a function of the Layer-1 occupancy using di-muon events. Crosses (boxes) indicate the collision (MC) data.

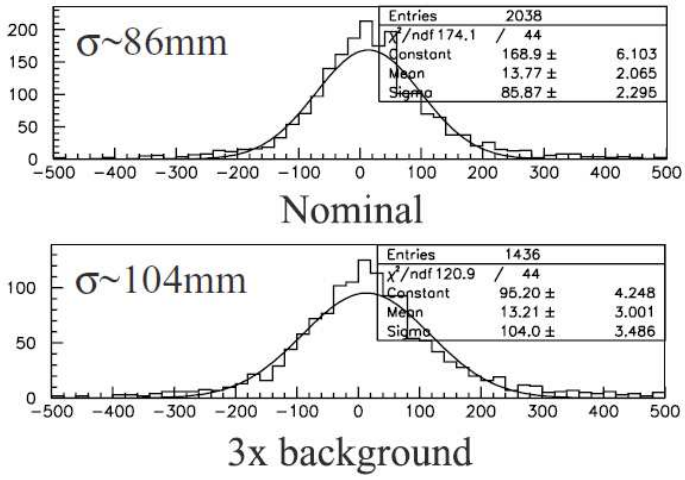

Figure 3.5: Expected impact of the triple background level in Layer-1 on the measured decay length difference of B_{CP} and B_{tag} vertices for the decay channel $B \to J/\psi K_S$.

Table 3.3: Target of the SVDs.

	SVD2	SVD2.5	SVD3
Physics	Observation of CP violation	Search for a new CP phase	Observation of a new CP phase
Normalized background level	1	3	20∼30
Trigger rate [Hz]	400	2k	10k∼20k

3.2 The upgraded SVD (SVD2.5 and SVD3)

The SVD upgrade is planned to proceed in the two steps: The first upgrade for KEKB, SVD2.5, and the second upgrade for SuperKEKB, SVD3. The strategy of SVD2.5 and SVD3 are given in Subsection 3.2.1. We also give a brief introduction of SVD2.5 in in Subsection 3.2.2. The introduction of SVD3 can be found in [11].

3.2.1 Strategy toward the high luminosity B factory

At the higher luminosity environment, the large beam-induced background and the higher trigger rate are expected as listed in Table 3.3. To suppress the beam-induced background event, the time constant in the electronics should be shorter. To cope with the high trigger rate, the deadtime-less readout system is required instead of the current track-and-hold readout. Furthermore, the expected annual radiation dose of innermost layers could reach 3MRad.

To meet all these requirements above, we adopt a faster readout system using a new readout chip (APV25) with analog pipeline memory, which is developed for the CMS silicon tracker at LHC. There are several reasons. First, the design of the chip is already finalized and mass production is on-going. The pipeline length is long enough to wait for the Level-1 trigger; it is more than 3 μs for a clock frequency of 40MHz. The continuous shaping scheme is also preferable at SuperKEKB where the bunch crossing occurs every 2ns. It has sufficient radiation hardness up to 30 MRad. We modified the readout scheme to suit for the KEKB Beam structure. We discuss the performance of the readout scheme in Chapter 4.

As the luminosity of the KEKB gradually increases, we will install the new SVD (SVD2.5) in the summer of 2007. In SVD2.5, APV25 readout is adopted to the innermost two layers.

In SVD3, we employ the readout system to all layers. At ∼12 times higher background level with a 10% occupancy, only using the APV25 is not sufficient. Hence, we develop a noble occupancy reduction scheme using event timing. We discuss it in detail in Chapter 5.

3.2.2 Overview of SVD2.5

In this subsection, we describe the overview of the SVD2.5: the silicon sensor and the readout system. The geometrical characteristics of SVD2.5 are the same as those of the SVD2. The APV25 readout system of the Layer-1 and 2 is completely new and the other systems are modified for optimization with APV25. The characteristics of the SVD2.5 are listed in Table 3.4.

Table 3.4: Characteristics of SVD2.5

	Layer-1 and 2	Layer-3 and 4
Sensor Direction	$r\phi$ for p-side (z for n-side)	z for p-side ($r\phi$ for n-side)
Strip Pitch [μm]	25.5 for p-side (76 for n-side)	75 for p-side (50 for n-side)
Readout Pitch [μm]	51.0 for p-side (152 for n-side)	150 for p-side (50 for n-side)
Capacitance [pF]	9.4 for p-side (4.7 for n-side)	3.8 for p-side (22.5 for n-side)
Readout chip	APV25	VA1TA

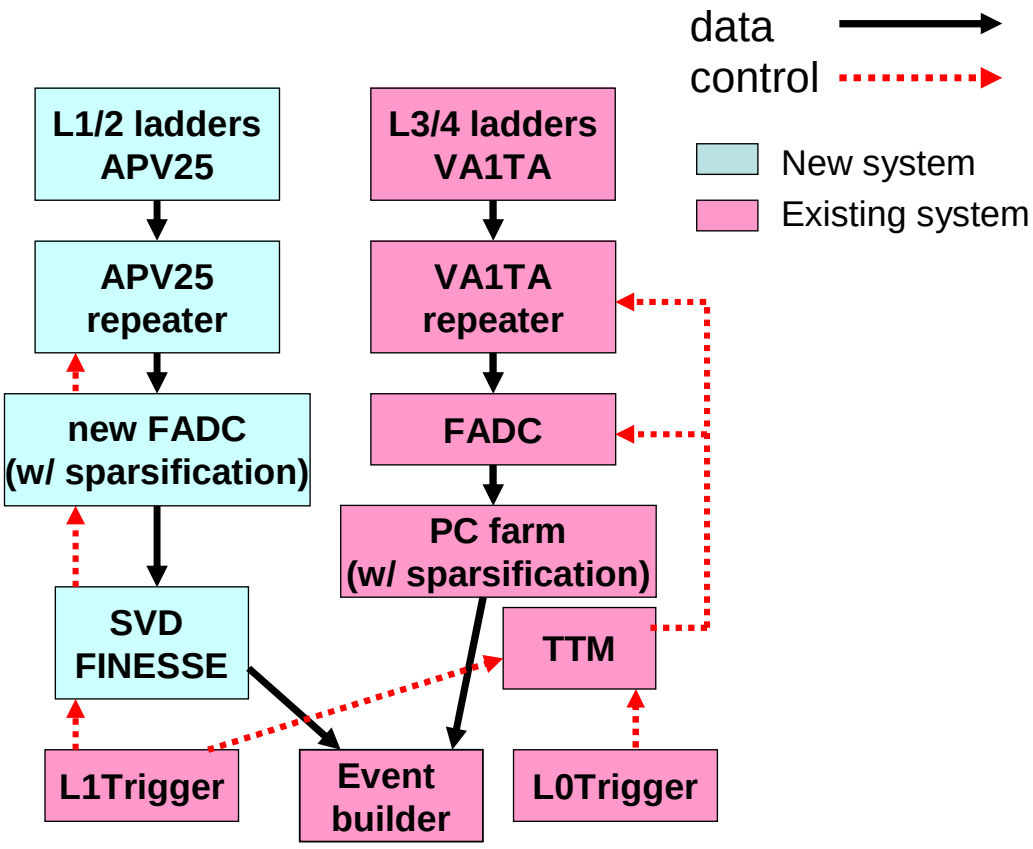

Figure 3.6: Overall design of the SVD2.5 readout system. The pink parts are the current system and the blue ones are the additional new system. The black lines and the red lines correspond to the signal paths and the control paths, respectively.

The double-sided silicon sensor

In employing APV25 as a readout chip, a sensor option is important because the noise at the shorter shaping is affected by the detector capacitance [7] [8]. The noise performance of APV25 is assumed to be the equivalent noise charge (ENC)=270+38C_{det}/pF with 50ns shaping time, while ENC of VA1TA is 250+12C_{det}/pF with 800ns peaking time. Total S/N with the DSSDs will be better for the longer peaking time. To ensure good S/N (> 15), we modify the sensor structures to reduce the capacitance [9]. Table 3.4 lists the specifications of the DSSDs for SVD2.5. The main modification is the flip of the sensor directions (PN flip) to reduce the detector capacitance of both sides.

The readout system

SVD2.5 readout system consists of two systems: APV25 readout system for Layer-1 and 2 and VA1TA readout system for Layer-3 and 4. Figure 3.6 shows the overall design of the SVD2.5 readout system from the output of the frontend chips to the Event Builder. To make the best use of both systems, the data streams are completely separated due to their different frontend chip properties. VA1TA readout system is the same as that of SVD2. APV25 readout system is completely new. After briefly describing the properties of VA1TA chip and VA1TA readout system, we show the detail description of APV25 chip and APV25 readout system.

- **VA1TA readout system**
  - **VA1TA chip**
    VA1TA is divided into 2 sections. One is the VA1 section for the analog readout, and the other is TA section for SVD trigger capability, but we don't use the latter. We explain the VA1 section.
    1. Preamp and CR-RC Shaper
       The signal is successively amplified by an integrating preamplifier and shaped by a CR-RC shaper with a peaking time of 800ns.
    2. Track and Hold
       When the hold trigger (Level-0) comes, the shaper output is held by the capacitors. When the readout trigger (Level-1) comes, the output voltage is read out sequentially.
    3. Multiplexing
       The 128 analog channels are multiplexed onto a single output.
  - **Overview of VA1TA readout system**
    The signals are transmitted to a repeater system installed in the boxes at the endplate about 2m away from the interaction point outside the main detector volume.

[7] The shot noise due to the leak current can be ignored.

[8] The noise component of a chip is mainly determined by two components. One is a detector capacitance dependence part ($\mathrm{Noise_{det}}$) and the other is a leak current dependence part ($\mathrm{Noise_{leak}}$). Assuming a peaking time as T_p, the detector capacitance as C_{det} and the leak current as I_{leak}, $\mathrm{Noise_{det}}$ and $\mathrm{Noise_{leak}}$ is represented as follows:

$$\mathrm{Noise_{det}} \propto \frac{C_{det}}{\sqrt{I_{T_p}}} \text{ and } \mathrm{Noise_{leak}} \propto \sqrt{I_{leak} T_p}. \tag{3.1}$$

[9] If we employed the same sensor as of SVD2, the S/N with 2 DSSDs of the Layer-2 would be 10 for $r\phi$ side, which don't meed our requirement.

The amplified signals are transmitted over 10 m-long CAT5 cables to a flash analog-to-digital converter (FADC) system in the electronics hut near the Belle Detector. The FADC system digitizes the data and provides information that is subsequently used by the trigger system. The digitized data is read out via custom PCI link boards to PCs where the data sparsification and the partial event building is performed and the data are further transmitted to the Event Builder of the Belle DAQ system.

- **APV25 readout system**
  - **APV25 chip**
    The APV25 circuit consists of mainly three parts: Preamplifier and shaper, Pipeline memories, and Multiplexing. Figure 3.7 and Figure 3.8 show the die layout and the architecture of APV25 chip. Here is the description of APV25 circuit. The more detailed description can be found elsewhere [13, 14].
    1. Preamplifier and Shaper
       The integrated preamplifier circuit is composed of a single-ended folded cascade amplifier with a feedback capacitor of 150fF and an input transistor of pFET type with a size of W/L = 2000/0.36μm. Due to this large effective width of input transistor, the intrinsic noise of APV25 is very low, corresponding to an equivalent noise charge (ENC) of $270e$+$38e$pF^{-1}. The shaping filter with a time constant of T_p = 50ns is coupled to the preamplifier output. The shaping curve is an ideal CR-RC shaper.
    2. Pipeline memory
       The shaper output is sampled at clock intervals and stored in the analog pipeline memory, which consists of a ring buffer of 192 cells with cycling write and read pointer. 160 cells are kept for trigger latency and 32 cells for event buffering. Their depths determined the latency time between signal and trigger arrival. With a clock frequency of 40MHz, the maximum time allowed for the trigger decision latency is 4 μs, which is long enough for average Belle Level-1 trigger arrival time of 2.2μs. To protect information from being overwritten, a FIFO with a depth of 32 locations stores the pipeline addresses of the cells that are awaiting for readout. This procedure avoids dead time while keeping a serial readout scheme. The charge of samples in the pipeline cells are converted to a voltage and consequently stored onto the capacitors.
    3. Multiplexing
       The sampled output is sent to a single output line though a 1:128 multiplexer with system clock (40MHz) or half system clock (20MHz.) The output buffer amplifies the multiplexer output current and splits into differential channels. Both output lines have an analog gain of 1mA/MIP, resulting in a differential signal of 2mA/MIP. The differential logic level corresponds to ±8mA.

       APV25 chip includes an internal calibration circuit. The operational principal is to apply a voltage step pulse ΔV to a series capacitance C that is connected to the preamplifier input. The injected charge Q is determined by $Q = C\Delta V$. The injected charge can be adjusted from 0 to 25.5fC by changing the amplitude of the voltage step. Moreover, the timing of the pulse can be adjusted in steps of 1/8 of the system clock (3.125 ns at 40MHz.) One can check the shaping curve of the shaper output and the pulse height linearity, and can obtain the

electronics gain.

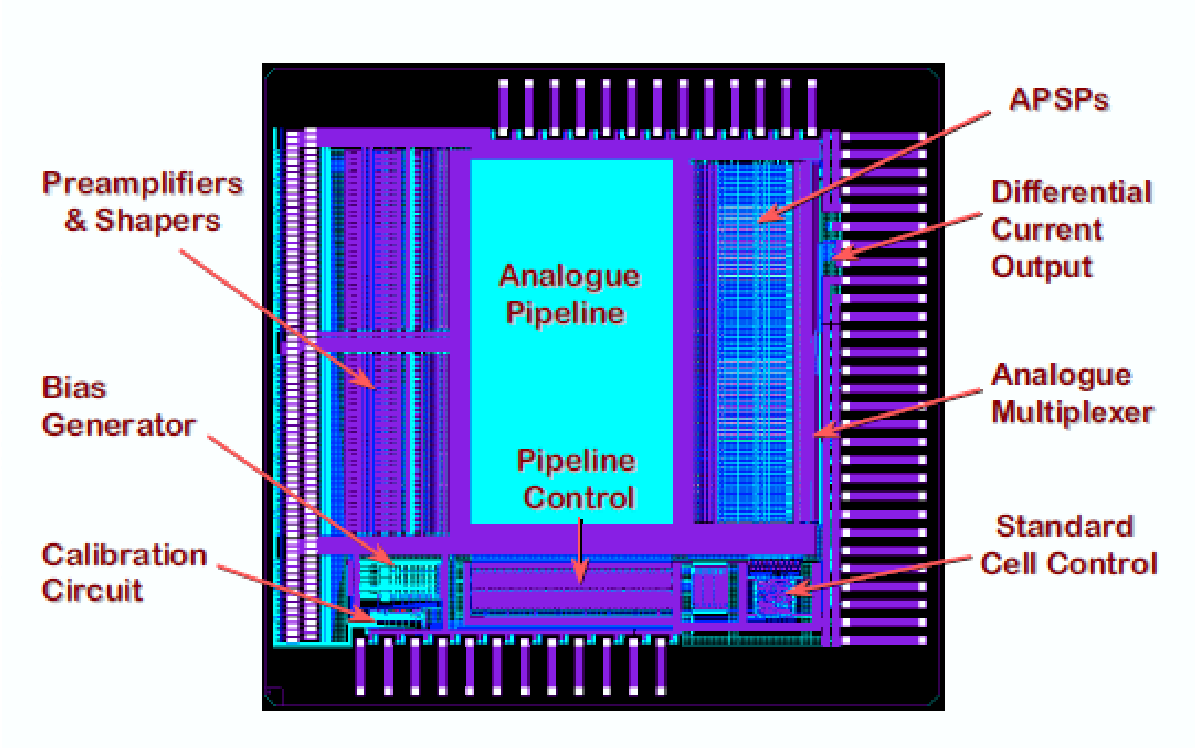

Figure 3.7: The die layout of APV25 frontend chip (8.055×7.1 mm^2.) The 128 input pads are visible on the left edges, the central parts are covered by the pipeline, and the control and output pads are to the right.

– **Overview of APV25 readout system**
We briefly describe the APV25 readout system. The analog data from the repeater is digitized on FADC. Data sparsification, and hit finding, is done by FPGA on FADC. The SVD FINESSE modules on COPPER system collects and packs data and also distributes timing control to the repeater and FADC. The data which pass through the data sparsification on FADC is finally sent to the Event Builder of the Belle DAQ system.

To summarize, the main differences concerning the readout systems are the difference of the signal processing speed and the trigger. The time scale of the processing is different by a factor of 10. VA1TA doesn't have pipeline memories and need hold trigger (Level-0 Trigger), while APV25 has long pipeline memories to buffer the analog data until the Level-1 Trigger comes. Table 3.5 and Table 3.6 summarize the comparisons of the two readout chips and their readout systems, respectively.

Table 3.5: Comparison of VA1TA and APV25 readout chips.

Readout chip	VA1TA	APV25
CMOS process [μm]	AMS 0.35	IBM 0.25
Radiation tolerance [MRad]	>20	>30
Principal	continuous shaping, analog	continuous shaping, analog
Peaking time T_p [ns]	800 (300∼1000)	50 (30∼130)
Multiplexing speed [MHz]	5	40
Pipeline memory [depths]	no	192
Trigger latency [depths]	no (need hold trigger)	160 (4.0 [μs] at 40MHz clock)
Intrinsic DAQ deadtime/event [μs]	25.6	0
Readout time [μs]	25.6	3.5
Power [mW/ch]	1.2	2.4

Table 3.6: Comparison of VA1TA and APV25 readout systems.

Readout chip	VA1TA	APV25
Layers	3, 4	1, 2
Trigger	Level-0 (hold), Level-1 (readout)	Level-1
Timing control (distribution)	TTM	SVD FINESSE
Data collection	PC Farm	SVD FINESSE
Data sparsification	PC Farm	FADC

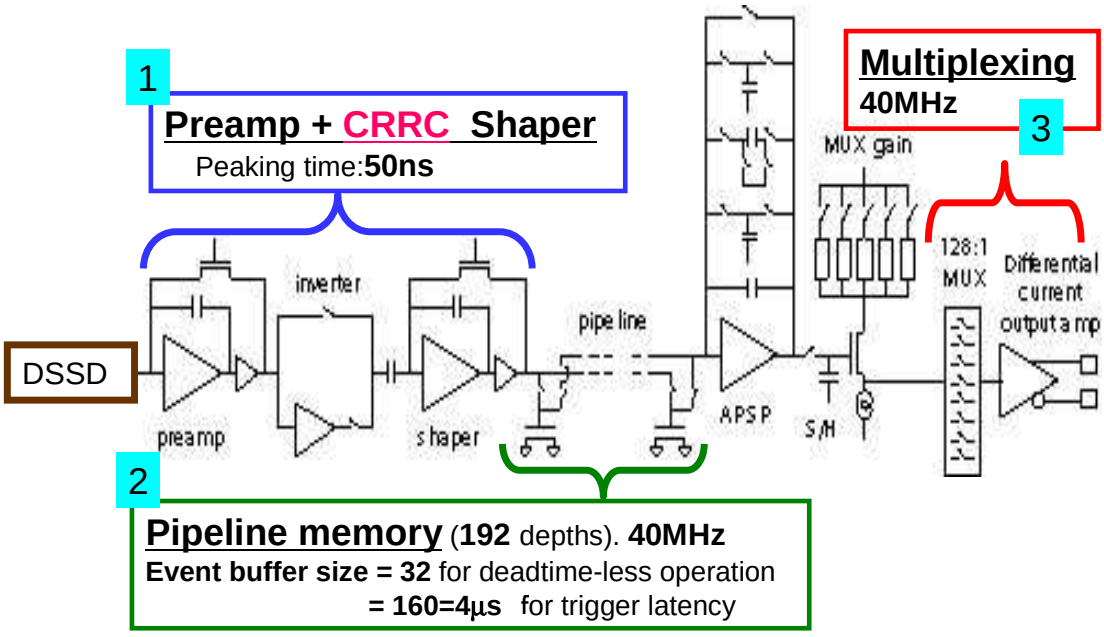

Figure 3.8: Architecture of APV25.

Chapter 4

Performance of APV25 readout scheme for SVD

In this chapter, we describe the APV25 readout scheme for SVD and its performance evaluation using the APV25 test system in the beam test at KEK 12GeV-PS.

4.1 Overview of APV25 readout scheme for SVD

In this section, we show the original operation modes of APV25 and their limitation for the SVD in Subsection 4.1.1. We describe the improved operation mode for SVD and the new readout scheme for SVD using it in Subsection 4.1.2.

4.1.1 APV25 operation mode

Analog Pipeline Voltage mode chip (APV25) has been developed for CMS Silicon Tracker [12] at LHC.

The properties of APV25 are as follows:

- Fast DAQ with a shaping time of 50ns and with a system clock of 40MHz.
- Long pipelined readout with analog memory as a delay buffer to wait for Level-1 trigger and as event buffers for burst trigger.

APV25 is operated originally in two modes:

- Peak mode.
- Deconvolution mode.

Figure 4.1 shows the APV25 shaper output measured by the internal calibration. In the peak mode, one sampling point within the pipeline cells is sent to the APV25 output buffer without passing on-chip internal processing (APSP.) In the deconvolution mode, the weighted mean of the three consecutive sampling points by APSP is sent to the output buffer. The extracted output appears only at an interval of 25ns. The signal output that does not occur at the corresponding clock timing is removed.

At CMS, a beam crossing occurs at every 25 ns. With a 40MHz clock and with a peaking time of 50ns, the components of the readout system, such as the peak position of the shaper output waveform, the sampling points and the pipeline, always operate synchronously to the beam collisions. However, KEKB, RF clock is 508MHz and it requires APV25 to be operated

Table 4.1: Comparison of the APV25 operation modes.

Operation mode	Peak	Deconvolution	Multi peak
# of input sampling points	1	3	3, 6, ..., 30
# of output sampling points	1	1	3, 6, ..., 30
processing	-	internal (on-chip)	external

practically under DC beams. In such operations, the clock timing of the data sampling may has some jitter relative to the trigger timing. Due to this jitter, the amplitude of the sampling point is different from the peak amplitude, resulting in lower and inaccurate gain. We, thus, cannot use the peak mode nor the deconvolution mode as they are.

4.1.2 APV25 readout scheme for SVD (Multi peak mode and Waveform reconstruction)

The APV25 has an I2C interface to access the internal registers, which control analog bias voltages and currents to tune the analog amplifiers, the operational modes, and the calibration settings.

We consider the possible solutions to overcome this issue as listed below:

- To use longer shaping time (50ns $\rightarrow$ 100ns.)
- To sample a part of the waveform of the shaper output (Waveform sampling) and reconstruct it by an external processing (Waveform reconstruction.)

The former option results the high occupancy and just reduces this effect. We take the latter option, which we realize not by modifying the electronics but by changing the controlling parameters of APV25. We call this waveform sampling mode *multi peak mode*.

The multi peak mode is realized by changing the programmable trigger pattern that the APV25 sequencer generates [1]. With this feature, we sample the waveform of the shaper output. Possible numbers of the samples to acquire are 3, 6, 9, ..., and 30. Figure 4.2 shows an example of the raw APV25 output in the multi peak mode. Followed by a header, consisting of the pipeline address and the error bit, the analog data of all channels are transmitted in the multiplexed order. The overall output is 140$\times$3X (X=1, 2, ..., 10) bit wide in multi-peak mode, while it's 140 bit wide in the peak mode and in the deconvolution mode. In this example, 6 samples are acquired in the sequence. Two triggers at an interval of 75ns are sent to the APV25, The APV25 returns three consecutive samples after each trigger and results the 6 sequential samples in total. Table 4.1 summarizes the properties of the operation modes. The difference of the CMS Silicon tracker and the SVD is also summarized in Table 4.2.

Through the beam test at KEK 12GeV-PS, we have established this APV25 readout scheme consisting of the multi peak mode and the waveform reconstruction methods. The reconstructed waveform information gives us not only the precise peak amplitude but also the start timing, which we call *event timing*. By comparing the reconstructed event timing and the trigger timing, we can effectively get rid of off-timing beam-induced background events. The details are described in Chapter 5.

[1] In the peak mode, the trigger pattern orders to sample 1 point. In the deconvolution mode, it orders to sample the consecutive 3 points.

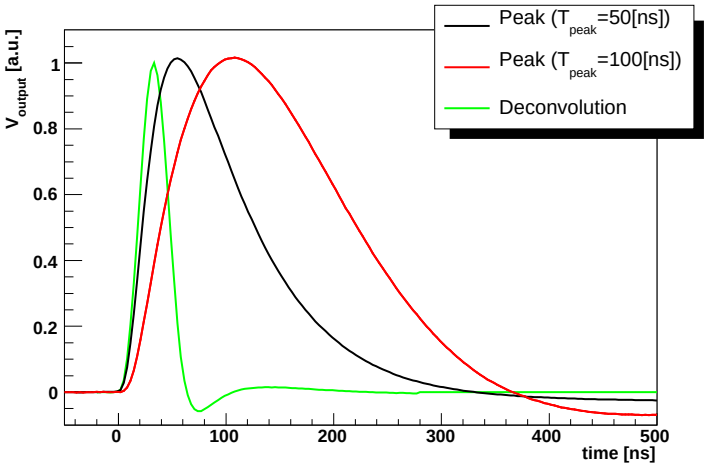

Figure 4.1: APV25 shaper output. The black (red) line corresponds to the shaper output in the peak mode with a peaking time of 50ns (100ns.) The green line indicates the shaper output in the deconvolution mode.

Table 4.2: Comparison of the environment around the CMS Silicon Tracker and the Belle SVD.

	CMS Silicon Tracker	Belle SVD
Beam structure (RF clock)	proton beam (40MHz)	e^+e^- beam (508MHz)
Trigger (Signal) and Sampling Clock timing	synchronous at 40MHz	jitter ($\pm$12.5ns, at worst)
Trigger rate [kHz]	$\sim$100	0.5$\sim$20
Operation mode	deconvolution	multi peak

To summarize, the new readout scheme not only removes the issue of low and inaccurate peak amplitude due to the timing jitter between the trigger and the clock but also suppresses the background-originated events.

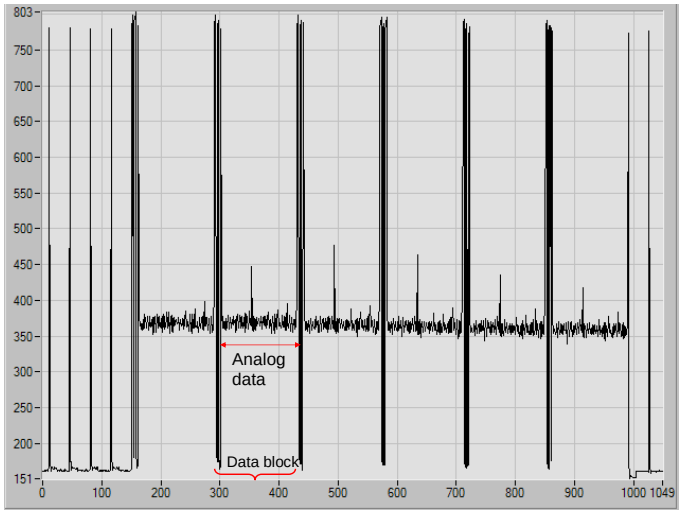

Figure 4.2: Screenshot of the raw APV25 output with the consecutive samples obtained with the multi peak mode. In each data block, the analog data follows in the multiplexed order after the header (the large spikes.)

4.2 APV25 test system

We introduce the APV25 test system in this section. Figure 4.3 shows the picture of the APV test system and its signal paths. The system can be divided into three sub-components: the silicon sensor, the frontend readout, and the backend readout. The followings are the brief description.

- Silicon sensor: Striplet sensor
  The sensors are DSSDs with short strips, called *Striplet* Detector. The details of the Striplet Detector are described in Appendix C. The strips with UV coordinates are placed at an angle of 45 degrees with respect to the DSSD outer shape with XY coordinates. For the P-side, the strip pitch and the readout pitch are 25.5μm and 51μm, respectively, since we read only one strip per each two strips. For the N-side, both the strip pitch and the readout pitch are 51μm. The applied bias voltage is 80V. We don't employ a striplet sensor for SVD2.5, although the sensor is the most promising sensor candidate for SVD3. As described in Subsection 3.2.2, we have developed the strip sensor with small noise due to its small capacitance, hence the results with this sensor can be applied to that for SVD2.5.

- Frontend readout: APV25, Hybrid, and Repeater
  We have 4 data/control paths between the APV25 and the repeater: Analog data (differential); Fast control (LVDS) such as trigger, clock and reset; Slow control (I2C) such as clock and data; and Power supply. Raw signal from the silicon sensor is received by the APV25 on a hybrid. The hybrid is connected to the repeater, which buffers the analog signals and supplies the power to the APVs. The repeater also relays control signals from the backend readout to the APV.

- Backend readout: APVDAQ and PC
  APVDAQ [15] is a 6U VME module with 1) a sequencer logic that delivers clock and trigger signals, 2) FADC memory/readout, and 3) I2C interface. APVDAQ sends clock and trigger signals to the repeater, communicates control signals with the repeater, and controls the crate bus with TTM signals, such as clock and event number. When the trigger comes (in beam test case, a trigger from the scintillator,) it generates the synchronized trigger with the clock by Flip-Flop in the sequencer. Then, it receives the analog signal via the repeater, and digitizes it with the FADC. APVDAQ itself is controlled by a software on PC through the VXI-PCI bus controller. The data acquisition (DAQ) software interactively controls the system and reads out the digitized data, which are recorded on a hard disk drive. Moreover, it provides a simple online analysis for monitoring purposes. APV25 software runs in the LabWindows/CVI environment by National Instruments on a PC under Windows NT.

This system is a realistic prototype of the new readout of SVD2.5 (See Subsection 3.2.2.) The hybrid and the repeater is almost the same as the final SVD2.5 version. APVDAQ corresponds to the combination of the FADC and SVD FINESSE. PC corresponds to the Event Builder and the data storage.

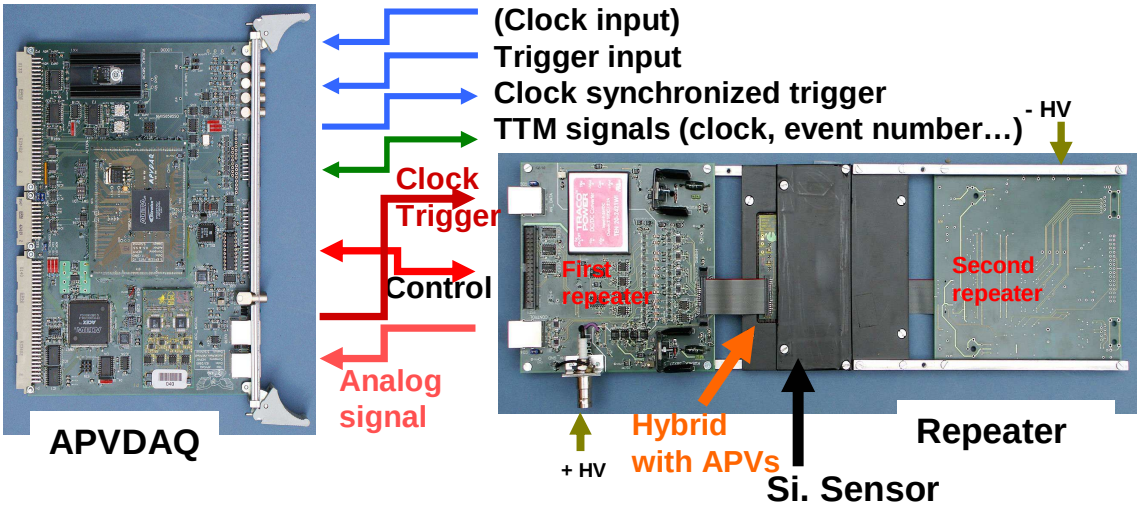

Figure 4.3: APV25 test system and its signal paths: Backend readout (Left) and Frontend readout (Right.)

4.3 Beam test

We carry out a beam test with the APV25 test system in the $\pi 2$ beamline at KEK 12GeV-PS. The purpose of this beam test is to establish the performance of the APV25 readout scheme by checking the following items:

- Cluster properties of the DSSDs for SVD with APV25 [2].
- Performance with the various APV25 operation parameters (Mode scan.)

[2]The sensor of the CMS Silicon Tracker is Single Sided.

- Performance of waveform reconstruction methods.
- Timing resolution of the reconstructed event timing.

We describe the hardware setup in Subsection 4.3.1, the data analysis to obtain the cluster information in Subsection 4.3.2, the results on the APV25 operation in Subsection 4.3.3, and the results on the waveform reconstruction in Subsection 4.3.4.

4.3.1 Hardware Setup

Figure 4.4 shows a schematic drawing of the hardware setup, which consists of the sensor (Figure 4.5,) the frontend readout (Figure 4.6,) and the backend readout (Figure 4.7.)

The additional hardware from the APV25 test system is the beam; the scintillator, and the PMTs; and the oscillator. The sensor and the scintillator is set perpendicularly to the beam. In the beam test, the trigger is produced from the scintillator signals detected by two photomultiplier tubes (PMTs.) The coincidence signals of the two PMTs with the adjustable delay are put into APVDAQ trigger input. As the reference for the study of the event timing reconstruction, we measure the time between the clock generated by APVDAQ and the trigger by TDC, which is optionally equipped on APVDAQ. For mode scan, the external clock of the oscillator is put into APVDAQ trigger input [3].

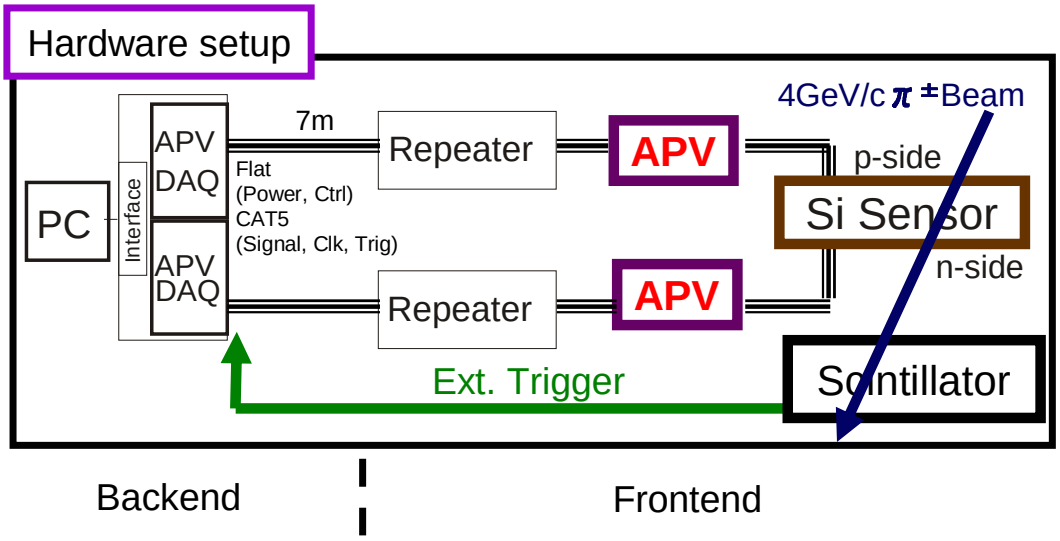

Figure 4.4: A schematic drawing of the hardware setup of the beam test.

4.3.2 Data analysis

We analyse raw data to extract the cluster information. The APV25 output frame (See Figure 4.2.) begins with a 11-bit header with digital values, consisting of 3 high bits and 8-bit pipeline address. The analog values of 128 channels and then an error bit follow. The analog values of the raw data are digitized by FADC on APVDAQ.

The measured ADC counts ($ADC_i(k)$) receive the contributions from several components, represented in Eq. 4.1. In the following description, the index i denotes the strip number, k

[3]The APV25 on-chip oscillator is 40MHz.

Figure 4.5: A picture of the striplet detector equipped with four APVs.

the event, *clk* the sampling clock frequency, and *address* the pipeline address.

$$ADC_i(k) = S_i^{particle}(k) + N_i^{noise}(k) + p_i + p_{i,clk,address} + CMS_{chip}(k). \tag{4.1}$$

It consists of the signal from a charged particle ($S_i^{particle}$), the random noise contribution for each channel ($N_i^{noise}(k)$), a DC voltage offset of each channel refereed to as Pedestal (p_i), and a random shift that is common in the all channels in one chip, so-called Common mode shift, $CMS(k)$. An additional pedestal contribution ($p_{i,clk,address}$) must be considered, which depends on the cable type, length, pipeline address and the clock frequency [4]. Since we cannot deconvolve $N_i^{noise}(k)$ from $S_i^{particle}(k)$, we extract $S_i'^{\,particle}$ ($=S_i^{particle}(k) + N_i^{noise}(k)$) from $ADC_i(k)$.

We show the analysis procedure. After the initialization, event loop follows.

Initialization

Initialization is done in two stages.

- **Calibration constant and Pedestal effect in a special run**
  In calibration run, we obtain the calibration constants (e/ADC) of each channel. By multiplying the calibration constant(e/ADC), one can change the unit from ADC counts to electrons.

  We also estimate the additional pedestal contribution ($p_{i,clk,address}$.) The correction values are obtained in a special run at high statistics.

- **Initialization of pedestal and noise in each run**
  With the first 600 events data taken by random triggers, we calculate the pedestal (p_i) for each channel. We also obtain the noise (n_i) for each channel to be used for hit finding and exclusion of noisy channels.

Event loop

Event loop, which is composed of the following four calculations, is repeated until the run ends.

1. **Data frame check**
   We remove the header and check the error bit.

[4] We guess this contribution is from the deterioration of the analog data by the preceding digital header part. This is because the deterioration is expected to depend on the cable properties and the contents of the digital header part determined by the pipeline address.

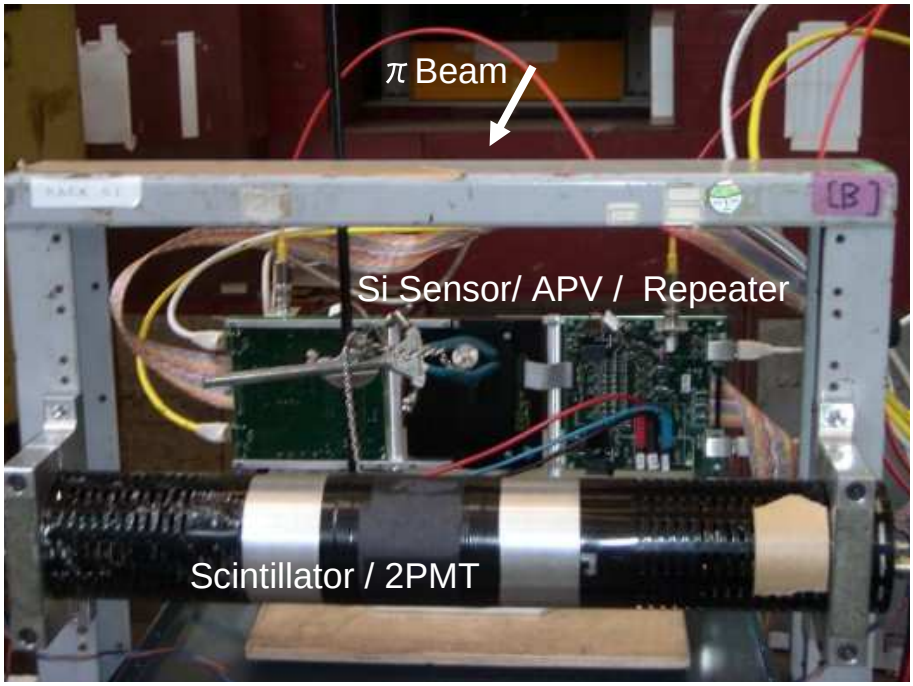

Figure 4.6: A picture of the frontend readout system.

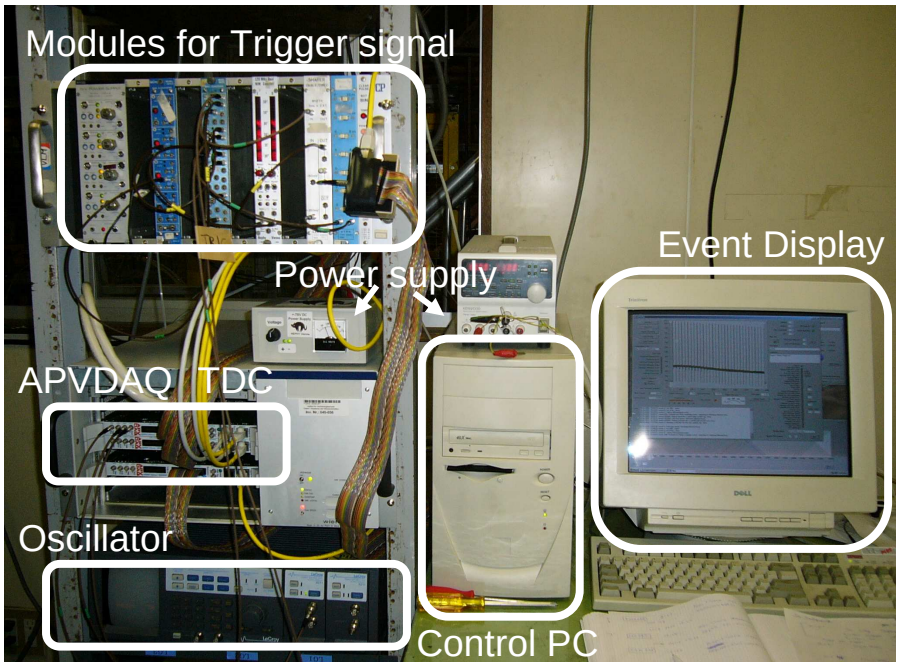

Figure 4.7: A picture of the backend readout system.

2. **Hit finding**
   We obtain the corrected signal data by subtracting the pedestal (p_i) and the additional pedestal ($p_{i,clk,address}$) from the raw data ($ADC_i(k)$.) Then, we calculate $CMS(k)$ for each chip by taking the average of the corrected signal data. After we update the signal data ($S_i'^{\,particle}$) by subtracting $CMS(k)$.

   We, then, search for hit candidates, which indicate $S_i'^{\,particle}$ is three times larger than n_i. CMS calculations are repeated twice with the hit candidates excluded. We finally obtain the signal data: $S_i'^{\,particle}$, find the hits and put the flags (Hit, Seed, or Noisy) to each strip data. Seed strip indicates $S_i'^{\,particle}$ is five times larger than n_i. Noisy strip indicates n_i is five times larger than the chip-averaged noise ($\bar{n}$.)

3. **Cluster finding in space direction**
   We search for the cluster candidate in space (space and time) direction in the peak (multi peak) mode. Here, we explain the peak mode case. We combine the subsequent hits, which indicates the cluster candidate, and calculate the cluster information, such as the cluster energy ($S_{cluster}$), the cluster noise ($N_{cluster}$) and S/N [5].

   We finally select the final clusters based on the following three conditions.

   - S/N is larger than C_s [6].
   - A cluster must include, at least, *one* seed strip.
   - A cluster energy is larger than 5000e.

4. **Waveform reconstruction in the multi peak mode**
   In the multi peak mode, we reconstruct the waveform and obtain the pulse height and the event timing (See Subsection 4.3.4.)

4.3.3 Results on the APV25 operation

After the data analysis, we obtain the cluster information. We operate it in the peak mode with 50ns shaping time and 40MHz clock.

First, we check the beam position by the hit position distribution. We obtain the hit position (X) by taking the center of gravity of ($S_i'^{\,particle}$) over one cluster as follows:

$$X = \frac{\sum_{i=Hit} x_i S_i'^{\,particle}}{\sum_{i=Hit} S_i'^{\,particle}}, \tag{4.2}$$

assuming that x_i denotes the strip position. Figure 4.8 shows the hit position distribution. The area on which both the sensor and the scintillator overlap is about 14mm in UV coordinates. The hit position distribution is Gaussian distribution with the width of 14mm and the center position of the center of the area. We confirm that the beam is well centered on the sensor.

[5] $S_{cluster}$, $N_{cluster}$ and S/N are defined as follows: $S_{cluster} = \sum_{i=Hit} S_i'^{\,particle}$, $N_{cluster} = \sqrt{\sum_{i=Hit}(N_i)^2}$, and S/N= $\frac{S_{cluster}}{N_{cluster}}$.

[6] We set the threshold for cluster (C_s) to be 5.

Cluster properties of SVD DSSD with APV25

We check the cluster properties of SVD DSSD with APV25, such as the cluster energy distribution, S/N distribution and the cluster width distribution [7] as shown in Figure 4.8. We fit the cluster energy distribution with the deconvolution of the Landau distribution and the Gaussian distribution. The result of the S/N distribution is far better than the requirement that S/N is larger than 10. Table 4.3 summarize the results. We confirm that the cluster properties of SVD DSSD sensor with APV25 fully meet our requirements.

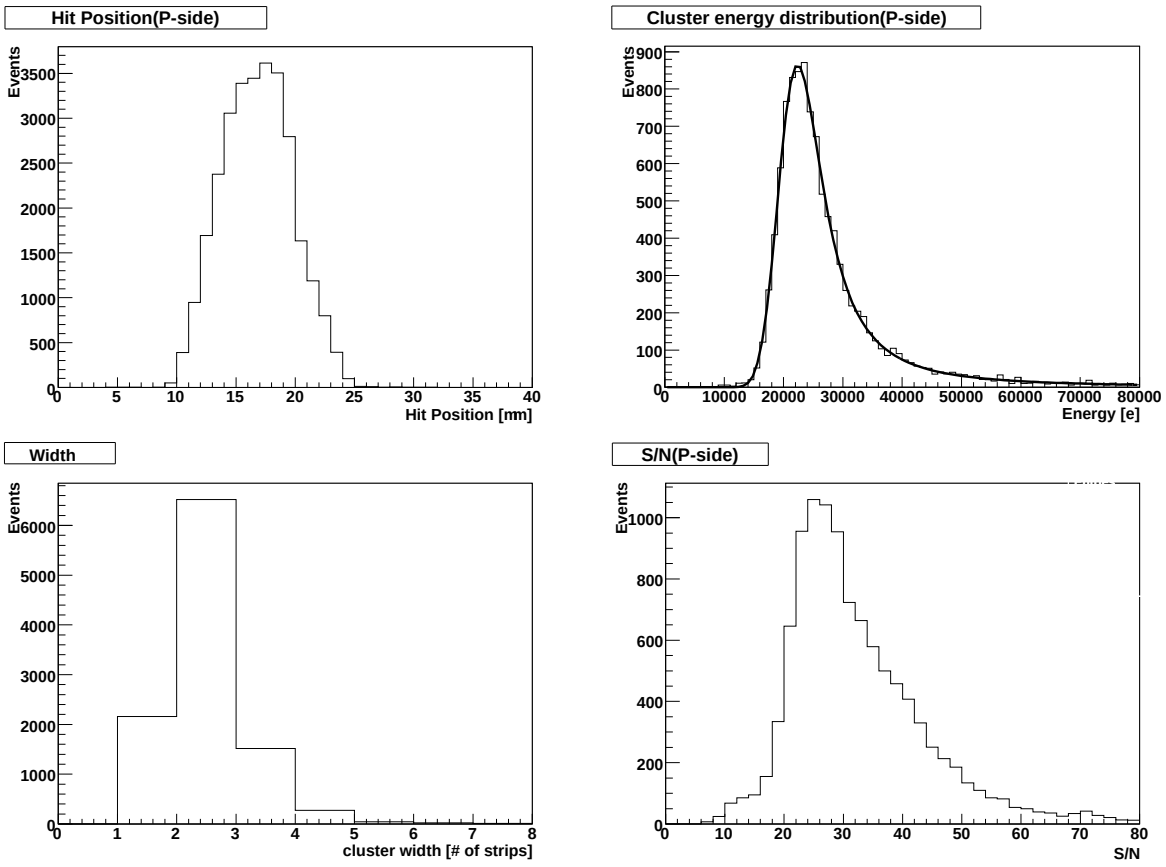

Figure 4.8: Cluster properties on P-side with the APV25. The distributions of the hit position (Top left), the cluster energy (Top right), the cluster width (Bottom left), and the S/N (Bottom right) are shown.

	P-side	N-side
Cluster energy [e]	21k	20k
S/N	26	28
Cluster width [# of strips]	2.1	1.6
Strip noise [e]	550	600

Table 4.3: Cluster properties of SVD DSSD with APV25 (The most probable values.)

[7] We define the cluster width as the number of strips in one cluster.

Performance with the various APV25 operation parameters (Mode scan)

To find the APV25 operation parameters that suit the SVD DSSD, we take data in the various conditions as listed below. Figure 4.9 (Figure 4.10) summarises the most probable values of the S/N (the cluster noise ($N_{cluster}$)) distribution in each condition.

- **Operation Mode**: Peak mode, Multi peak mode and Deconvolution Mode.
  We take data with multi peak mode, with keeping low noise. The deconvolution mode compromises the noise because the noise component increases due to the on-chip signal processing. Moreover, the multi peak mode is preferable in a view of the readout scheme (See Subsection 4.1.2.)

- **System clock**: 40MHz, 63MHz and 80MHz.
  We *can* operate at a clock of 63MHz and 80MHz using the external oscillator. But S/N is worse than that with 40MHz because the faster clock results in the worse performance. Moreover, all the components of APV25 are optimized to work at 40MHz and APV25, thus, operates stably at a clock of ∼40MHz. Since we plan to operate it with the SuperKEKB system clock of 42.33MHz, this result is preferable for us.

- **Peaking time**: 50ns and 100ns.
  The performance of amplifier is better for 50ns peaking time case because we change a peaking time by controlling the input current of the transistor of amplifier that is optimized for 50ns setting, although the total noise with the sensor is generally better for the longer peaking time (See Subsection 3.2.2.) Moreover, the shorter peaking time leads to the less background hits and the less occupancy. A peaking time of 50ns is the most suitable for SVD.

Considering both the performance and the readout scheme, we confirm that the multi peak mode with a peaking time of 50ns and a clock of 40MHz is the default setting of the APV25 operation for SVD.

4.3.4 Results on the waveform reconstruction

In this section, we describe the waveform reconstruction using the sampling points with the multi peak mode. The detailed discussion on the waveform reconstruction methods are shown in Section 5.2.

Overview of waveform reconstruction

We reconstruct the waveform with the discrete sampled values. We explain it with the example shown in Figure 4.11. We sample 6 consecutive points at an interval of 25ns: P[0], P[1], ..., and P[5]. The APV25 sharper output is almost the same as a CR-RC function, especially in the time region where we really want to see (around the peak.) The linearity of the waveform shape is guaranteed up to 7MIPs by a calibration run.

We fit the 6 amplitudes with the known function (W(ΔT)) and the obtained parameters are the peak amplitude (A) and the start timing relative to the clock timing ($\Delta T_{\rm start}$(fit)), respectively:

$$W(\Delta T) = A \cdot x \cdot e^{-(x-1)}, \tag{4.3}$$

assuming that ΔT indicates the timing relative to the clock and $x = \frac{\Delta T - \Delta T_{\rm start}}{T_p}$.

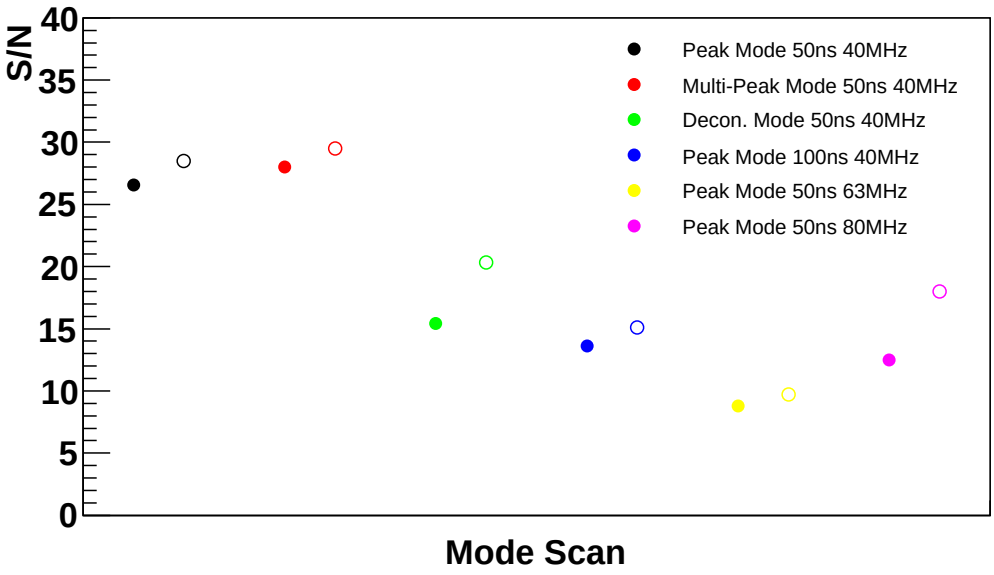

Figure 4.9: The most probable value of S/N distribution in various operation modes. The closed (open) circles correspond to P-side (N-side).

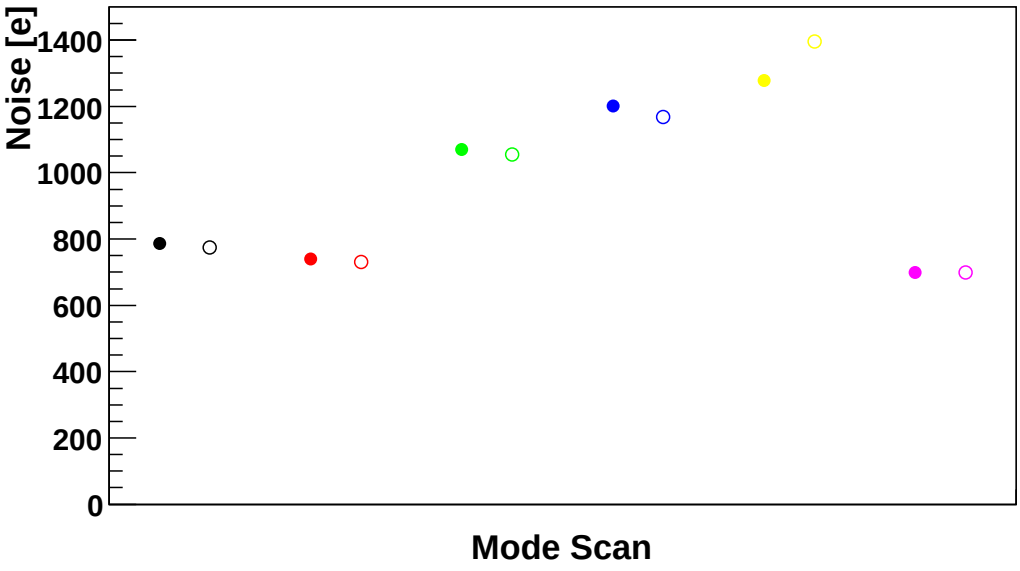

Figure 4.10: The most probable value of cluster noise distribution in various operation modes. The closed (open) circles correspond to P-side (N-side).

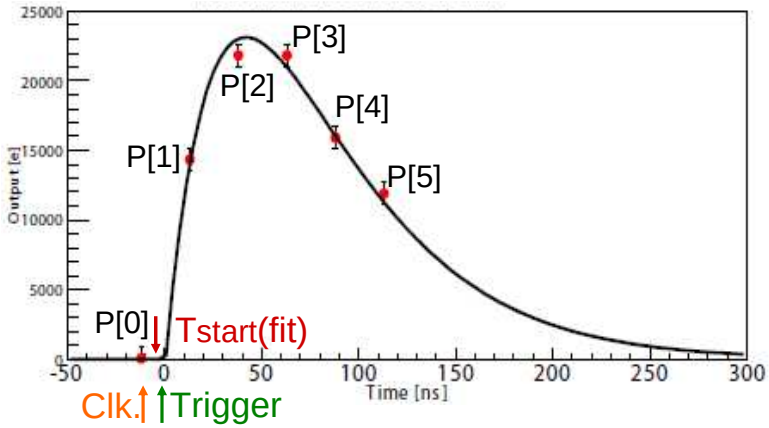

Figure 4.11: The sampling points with the multi peak mode and the reconstructed waveform using fitting as a function of time, assuming that the trigger timing ($T_{trigger}$) is 0. The orange (red) arrow points to the clock timing ($T_{Clk.}$) of the first sampling point (the reconstructed event timing (T_{start}(fit)).)

Reconstructed event timing resolution

In the beam test, we measure the timing difference ($\Delta T_{trigger}$) between the trigger and the clock. Since the shaper output starts at the trigger timing, $\Delta T_{trigger}$ has a correlation with ΔT_{start}(fit) as shown in Figure 4.12 (Left).

Now, we assume the trigger timing to be T(Trigger)=0. We define the event timing as T_{start}(=ΔT_{start}+T(Clk.).) The residual distribution of the reconstructed event timing and the trigger timing, which corresponds to the true event timing, is shown in Figure 4.12 (Right.) We fit it as a gauss function. The RMS of the distribution is 2.4[ns]. In this way, using the amplitudes of the sampling points, we reconstruct the event timing with a timing resolution of 2.4[ns].

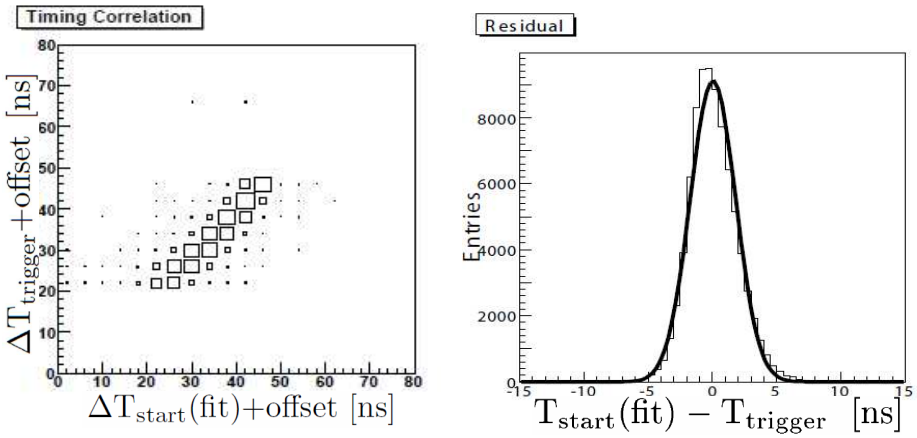

Figure 4.12: Correlation between and ΔT_{start}(fit) and $\Delta T_{trigger}$ (Left.) The residual distribution between the reconstructed event timing and the true timing (Right.)

The number of sampling points

We determine how many sampling points we need for the waveform reconstruction. In the multi peak mode, we obtain sampling points until the FIFO becomes full: 3, 6, up to 30. 1, 3, or 6-point samplings are realistic options because the time range above the threshold is ∼160ns. We compare the results with 1, 3, and 6 sampling summarized in Table 4.4. We obtain the best timing resolution with the 6 sampling points by the fitting. However, the more sampling points cause the larger data size and the longer readout time, which affect the backend DAQ system. In addition, the true timing resolution is limited by a jitter of the Belle Level-1 trigger (∼3[ns] [8].) Therefore, three-point sampling multi peak mode is the best in terms of both the reconstructed data quality and the backend DAQ.

Table 4.4: Performance with the various number of the sampling points.

# of sampling points	1	3	6
The obtained value/the peak	0.9 [9]	0.95	1
Timing resolution (RMS) [ns]	-	3.0	2.4
Readout time [μs] [10]	3.5	10.5	21.0
Normalized data size per event	1	3	6
Pipeline buffer [events]	32	10	5

4.4 Summary of the performance of APV25 readout scheme for SVD

Though the results of the beam test, we confirm that

- The cluster properties of SVD DSSD with APV25 readout are good enough.
- The three-point sampling multi peak mode with a peaking time of 50ns and a clock of 40MHz has a good property as the default setting of the APV25 operation.
- With this setting, we obtain the event timing with a timing resolution of 3.0ns.

[8] The trigger jitter of the beam test is less than 1[ns]

[9] The amplitude in one-point sampling is assumed that the point is sampled at the appropriate time, and could be 0.8 or worse dramatically if not.

[10] The readout time of VA1TA is 25.6μs.

Chapter 5

New occupancy reduction method using event timing reconstruction

With the readout scheme using the multi peak mode, we obtain the precise event timing. If the event timing information is available for the background reduction, we can further reduce the occupancy than using a shorter shaping time.

We describe the overview of the new occupancy reduction method using event timing reconstruction in Section 5.1, and timing reconstruction methods in Section 5.2. We also show the simulation study of the occupancy reduction power at the expected background level in Section 5.3 and the performance of the occupancy reduction method in Section 5.4.

5.1 Overview of the new occupancy reduction method

The occupancy reduction is done by eliminating beam-induced background hits while keeping all signal hits. There are two approaches to reduce the occupancy:

- Space wise (See Section 6.2.)
- Time wise (See Figure 5.1.)
  - using a fast shaping time (Subsection 5.1.1)
  - using event timing information: time cut (Subsection 5.1.2)

In the space wise approach, one reduces the sensitive area per channel with a fine segmentation of a sensor, which leads to the increase of the number of channels and requires the cost of the sensor developments.

In the time wise approach, one reduces the sensitive time with a fast readout chip. We choose the latter option because it doesn't cost much and we can achieve this by only buying the already-available APV25 chip.

A signal-originated event timing correlates to the trigger timing, while a background-originated event timing is irrelevant to the trigger timing and random. Since almost all the SVD hits are due to the beam-induced background and the hits that are derived from physics events have almost negligible fraction [1], the narrower the sensitive time is, the less occupancy we obtain.

The occupancy reduction in time wise proceeds in two stages. We show the occupancy reduction scheme in time wise in the next subsections.

[1] In the most case, occupancy due to physics events is estimated to be 0.5%.

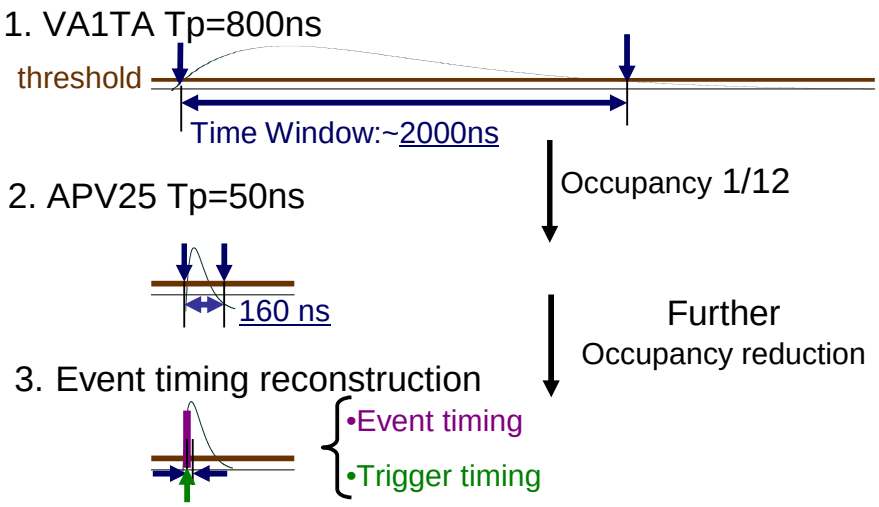

Figure 5.1: Occupancy reduction in time wise using a fast shaping time (1.→2.) and using event timing information (2.→3.).

5.1.1 Occupancy reduction with a fast shaping time

Figure 5.1 shows the idea of occupancy reduction in time wise using *Time Window*. The time window is defined to be the time range when hits above the threshold are accepted as signals. The number of hits and the occupancy can be reduced by the ratio of the time window. If we employ a readout chip with a shorter shaping time, we obtain a narrower time window (See Figure 5.1: 1.→2.). For example, when we set the threshold of the cluster cut to be S/N=3, the time window of VA1TA is measured to be 2000ns, and that of APV25 to be 160ns. Therefore, the occupancy is reduced by a factor of 12.

5.1.2 Occupancy reduction with event timing reconstruction

By only using the multi peak mode, we obtain the precise event timing information. By comparing the reconstructed event timing with the trigger timing, we can suppress off-timing events (*time cut*.) (See Figure 5.1: 2.→3.). The better timing resolution(=the reconstructed event timing - the trigger timing) results in the narrower time window. If we apply time cut using the reconstructed event timing, occupancy can be reduced further than the shaping time ratio.

5.2 Time reconstruction methods

In this section, we discuss how to reconstruct the event timing in the readout system. We must consider when we reconstruct them in the data flow, namely, online or offline. The offline reconstruction gives better resolution of the peak amplitude and the event timing if the bandwidth allows, because of its sufficient CPU power and of the availability of the useful informations such as the precise event timing from the other sub-detectors. On the other hand, the online reconstruction gives us better data reduction power, which is important for the

backend DAQ system with the limited bandwidth. The required bandwidth depends on the background level and the trigger rate at each stage in the backend DAQ system.

We consider three possible reconstruction methods as the candidates:

- Fitting method.
  We fit the sampled points with the parametrized waveform function obtained by internal calibration event by event as shown in Figure 4.11. Due to a huge amount of the iterative calculation, this method requires large CPU power and can be applied to offline analysis.

- Analytic method.
  The APV25 shaper is a precise CR-RC shaper and its output function is well known. We can analytically calculate the peak amplitude and the event timing, and also can obtain the deviations of the measured points from the CR-RC function like the event tag. Taking Figure 5.2 as an example, we measure a set of three quantities, P[1], P[2], and P[3], for input parameters, and obtain three quantities, T, A, and D, for output ones. T indicates the the sampling time of P[2], A the peak amplitude, D the deviation from the ideal CR-RC function. The CR-RC function($W_{cr-rc}(t)$) is written as

$$W_{cr-rc}(t) \quad = \quad A \cdot x \cdot e^{-(x-1)}, \tag{5.1}$$

  assuming the trigger timing as t=0, T_p as the peaking time and x as $\frac{t}{T_p}$.
  Then, T, A, and D can be described as follows:

$$\begin{aligned} T = f_1(P[1],P[2],P[3]) &= \frac{2aT_p \cdot P[2]}{P[3]e^a - P[1]e^{-a}} \equiv x_2\ T_P \\ A = f_2(P[1],P[2],P[3]) &= \frac{e^{x_2-1}(P[1]e^{-a} + P[2] + P[3]e^a)}{3x_2} \propto P[2] \cdot e^{x_2}\frac{X+Y+1}{x_2} \\ D = f_3(P[1],P[2],P[3]) &= \frac{P[1]e^{-a} + P[3]e^a - 2P[2]}{\sqrt{2}P[2]} \propto X + Y - 2, \end{aligned} \tag{5.2}$$

  assuming that T≡T(P[2]), $a \equiv \frac{25[ns]}{T_p[ns]}$, $X \equiv \frac{P[1]\cdot e^{-a}}{P[2]}$, and $Y \equiv \frac{P[3]\cdot e^a}{P[2]}$ [2].

  We check the performance using the beam test data as shown in Figure 5.2. The upper figure shows the shaper output, the six sampling points. The purple arrow points T, the red one A, and the blue one D. We choose the consecutive three samples among the six samples, given in black, red, green, and blue colors. The bottom figures show the distributions of the calculated T, A and D. T is expected to distribute flat and A is expected to distribute as the Landau function. But, the resolutions differ in the range of the selected samples due to the noise of the sampling point with the low amplitudes and the systematic differences from the CR-RC function. Table 5.1 gives the comparison of the performance in each set. The set of three samples that gives the good resolution for both the peak amplitude and the event timing is P[1],P[2] and P[3] (around the peak (the red color.))

  This method is suitable for offline analysis but it consumes much less CPU power than the fitting. But, we *can* implement this algorithm, which consists of the fundamental operation, even in the limited resources of online FPGA on FADC.

[2] Note that the relations between P[1], P[2], P[3] and between X and Y are described as $\frac{P[1]\cdot e^{-a}}{P[2]} + \frac{P[3]\cdot e^a}{P[2]} = X + Y = 2$.

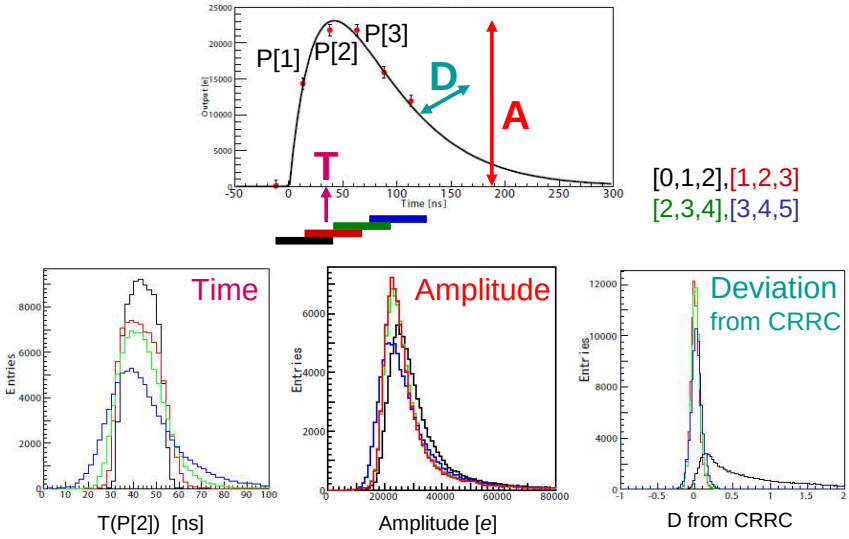

Figure 5.2: Example of the waveform reconstruction with the analytic method (Top.) The vertical axis indicates the output as a function of time, assuming the trigger timing to be 0. The output parameters (T, A, and D) are also shown.) The distributions of T, A, and D are shown (Bottom.)

Table 5.1: Performance of the analytic method with the various sets of the selected 3 samples.

Set	(P[0], P[1], P[2])	(P[1], P[2], P[3])	(P[2], P[3], P[4])	(P[3], P[4], P[5])
Timing resolution [ns]	2.4	3.0	3.2	9.4
Normalized Amplitude	1.2	1	1	0.9

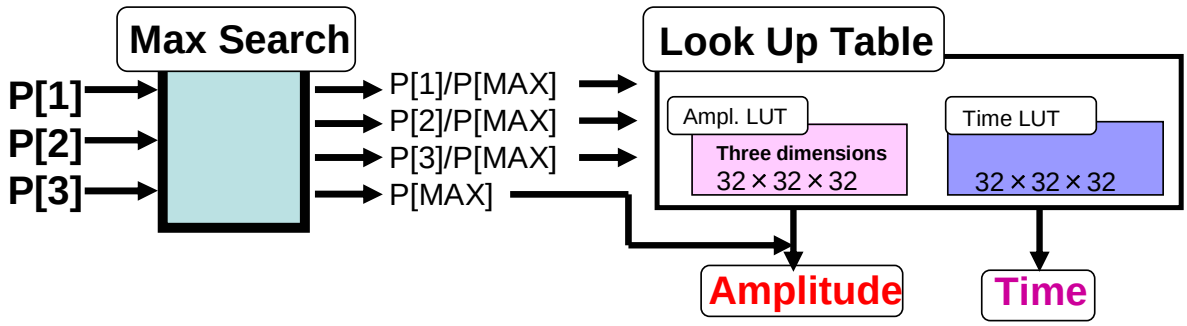

Figure 5.3: The flow chart of Look Up Table method. When we input a set of the sampled amplitude (P[1], P[2], P[3]), we first search the maximum value (P[MAX]) among them. We divide P[1], P[2], and P[3] by the maximum value. We create two sets of the three dimensional look up table using the divided three values: Amplitude Look Up Table and Time Look Up Table. We obtain the peak amplitude by multiplying P[MAX], and the event timing.

- Look Up Table method.
  If the precise timing information is available in online, Look Up Table is the most suitable for online processing. The performance is limited due to the limited memories on FPGA. Using huge [3] internal calibration data obtained from APV25, we create a look up table on the same size of memory as that on FPGA as shown in Figure 5.3 [4] and check the performance.

Table 5.2 shows the comparisons of the three reconstruction methods. Event by event fitting is not realistic due to the CPU power consumption. If we need the powerful background reduction, the online processing at the FPGA is necessary. In the following studies, we employ the analytic method when we reconstruct the waveform.

Table 5.2: Comparison of the waveform reconstruction methods.

Method	Fitting	Analytic	Look Up Table
Timing resolution [ns]	3.0	3.3	3.7
online or offline	offline	offline/online	online

5.3 Simulation of the occupancy reduction power at the expected background level

Under the beam background environment of the Belle experiment, the effects of distorted clusters of pileup events are not negligible. The current occupancy indicates the sizable rate of the hits that are piled up with a beam-induced background [5]. But, in the beam test at KEK 12GeV-PS, the beam intensity is too low to observe signal pileup events that are expected in

[3] 1 million events.

[4] There are two big memory blocks:2×64K×9bits on our FPGA (Altera Stratix EP1S20) and we test the performance of the look up tables with various configurations.

[5] Level-1 trigger rate and beam-induced background rate are 400Hz and ∼30kHz, respectively. Therefore, when we consider a pileup event, the background waveform is merged to a signal.

the high occupancy environment. To estimate the occupancy reduction factor with the time cut, we carry out a simulation study including pileup events. In addition, we estimate the effects of a Level-1 trigger jitter to the timing resolution.

5.3.1 Simulation Setup

We prepare the following three kinds of simulation data: signal events, beam-induced background ones and pileup ones as shown in Figure 5.4.

- Signal event: The real data obtained by the beam test.
- Beam-induced background event: The data generated by MC, assuming that the shape of an output waveform is the same as the one obtained by the internal calibration. The amplitude of the waveform is simulated to match the measured cluster energy distribution of the SVD2 background, and the event timing is assumed to distribute flat because a background event occurs at random and continuous timing.
- Pileup event: A background waveform is merged to a signal. We use beam test data and a simulated beam-induced background data generated by MC. The overlapping background event timing is set to distribute from -130ns to 80ns so as to affect the signal.

As the default background level, we adopt the current background level. At the current background level, the occupancy of Layer-1 with VA1TA is 10%.

5.3.2 Reconstructed energy and timing resolution

From the three sampling points of the waveform of the simulation data, we obtain the cluster energy and the event timing using the analytic method. Figure 5.5 shows the reconstructed cluster energy distribution. For the pileup events, the most probable value of the reconstructed energy distribution is 1.4 times higher than that of the signal events [6]. Figure 5.6 shows the residual distribution of the event timing (A reconstructed event timing (The purple arrow in Figure 5.4) minus a trigger timing (The green arrow in Figure 5.4)). The asymmetry of the residual distribution in the pileup event case is ascribed to the relative position between the background timing and the event timing [7]. The obtained timing resolution (RMS) of the signal event distribution is 3.3ns, while that of the pileup event one is 9.9ns.

5.3.3 Trigger jitter

In the time cut, we check the difference between the reconstructed event timing and the timing calculated from the trigger timing. Level-1 trigger has some jitter, which differs in the trigger source. Level-1 trigger of the Belle experiment has two kinds of sources to determine its timing. One is TOF with a jitter of 3ns and the other is ECL with a jitter of 30ns. Most of the hadron events, which we are interested in, are triggered by a TOF-oriented Level-1 trigger [8]. We assume that the trigger jitter follows a Gaussian distribution with a sigma of 3.0ns. Due to

[6] For the amplitude, we apply only S/N cut and doesn't use the amplitude value itself. If the S/N is larger than the threshold, this case doesn't matter.

[7] The asymmetric shape depends on the timing which the background overlap at: tail (The top left figure of Figure 5.4) or peak (The bottom center and the bottom right figures.) If a tail of the background shaper output overlaps (off timing), it affects the resolution a little (∼5ns), but if a peak of it overlaps (on-timing), the performance deteriorates. But, the probability which a on-time background overlaps is ∼30%.

[8] At the harsh background level expected at the SuperKEKB, TOF will not work at all. Time of Propagation (TOP) counter is a candidate for giving the precise trigger timing.

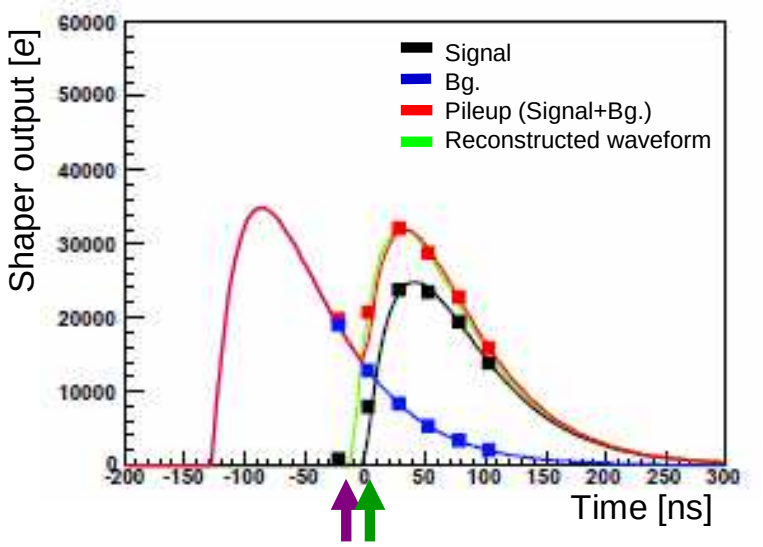

Figure 5.4: Example of the simulation data. The vertical axis indicates the amplitudes and the horizontal one the time, assuming the trigger timing as 0. The squares (curve) correspond to the sampling points (expected shaper output.) The black data, the blue one and the red one correspond to the signal event, the beam-induced background one and the pileup one. The green curve corresponds to the reconstructed waveform using the pileup event. The green (purple) arrow points the trigger timing (the reconstructed event timing.)

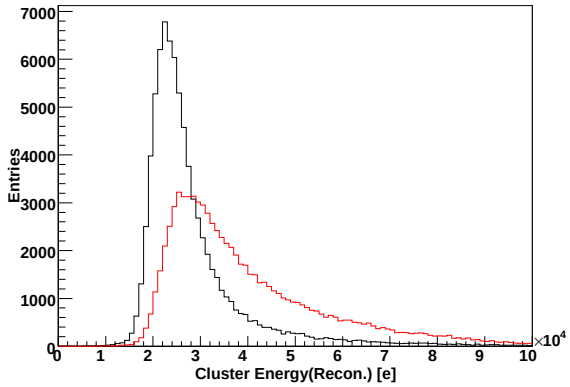

Figure 5.5: The reconstructed cluster energy distribution. The black (red) histogram indicates a signal event (a pileup event.)

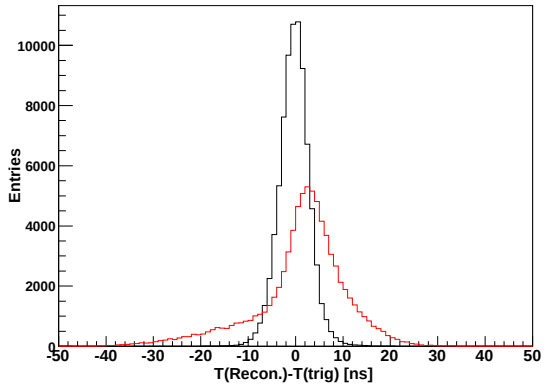

Figure 5.6: The residual distribution of the reconstructed event timing. The black (red) histogram indicates a signal event (a pileup event.)

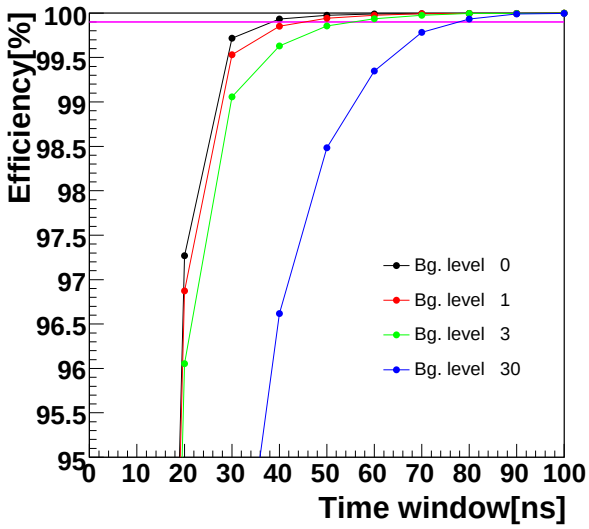

Figure 5.7: Signal efficiency as a function of the time window at the various background levels. The background level is normalized by the current one.

the trigger jitter, the timing resolutions deteriorate to 4.5ns and 10.3ns for a signal event and a pileup event, respectively. In the following study, we include the effect of the trigger jitter.

5.3.4 Efficiency and Time window

We define the *efficiency* as the ratio of the number of samples within the time window to the number of all the samples. We vary the time window by 10ns step and estimate the efficiency for each step. Figure 5.7 shows the signal efficiency as a function of the time window. Here, we define the time window so as to keep the efficiency over 99.9% (the pink line.) For 0, 1, 3, and 30 times relative background levels to the current, the time window is set to be 40, 50, 60, and 80ns, respectively.

Figure 5.8 shows the time window as a function of the background level. We set two levels of the time window and the time cut: the tight cut with the wide time window to keep the efficiency over 99.9% (the black closed circles,) and the loose cut with the narrow time window to keep the efficiency over 99.0% (the red closed circles.)

5.4 Performance of the new occupancy reduction method

In this section, we estimate the occupancy in each background level. Figure 5.9 shows the expected occupancy as a function of the background level. In terms of the data quality, the critical limit of the occupancy is around 10 %. Table 5.3 shows the summary of occupancy reduction factor at the expected background levels. Without APV25, SVD works only by the current background level (the blue line.) By employing APV25, the time window will be reduced from 2000ns to 160ns, and the corresponding occupancy reduction factor will be 12 (the black line.) If we require the efficiency of 99.9%, up to 25 times larger background level is acceptable (the red line.) With the tight cut at the efficiency of 99.0% (the green line), the system will work even at 32 times larger background level, which satisfies the requirement of the SuperKEKB.

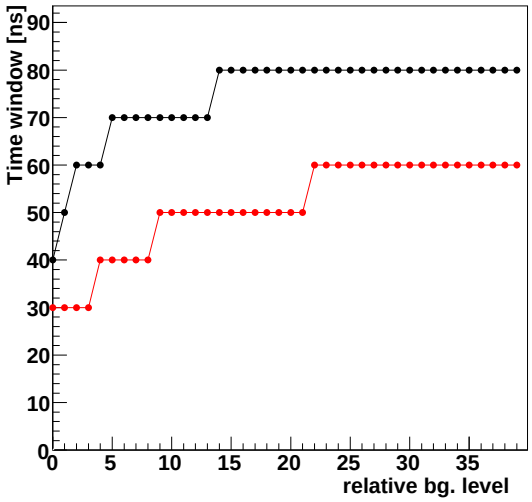

Figure 5.8: Time window as a function of the relative background level to the current. The black and red line correspond to the tight cut case (efficiency: 99.9%) and the loose cut case (efficiency: 99.0%), respectively.

Table 5.3: The occupancy reduction factor at each relative background level. For the loose (tight) time cut, the efficiency is assumed to be 99.9% (99.0%), respectively.

Background level (normalized by the current level)	1	3	30
	SVD2	SVD2.5	SVD3
Occupancy [%] with VA1TA	10	(30)	(∼100)
Time window (loose) [ns]	(50)	60	80
Occupancy reduction factor with time cut	(3.2)	2.7	2
Occupancy [%] without time cut	(0.6)	2.4	24
Occupancy [%] with loose time cut	(0.2)	0.7	12
Occupancy [%] with tight time cut	(0.1)	0.3	9

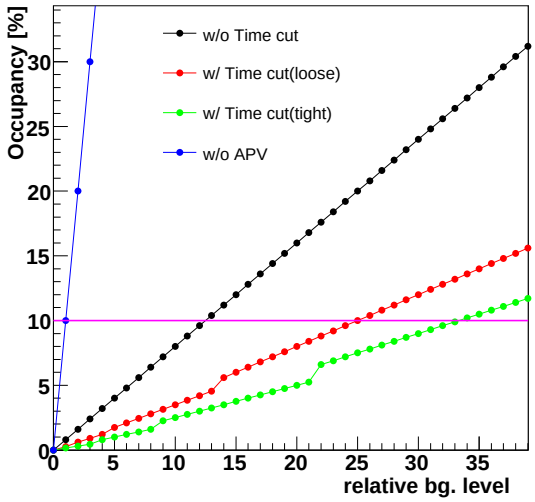

Figure 5.9: Occupancy as a function of the relative background level to the current. The pink line indicates the upper occupancy level acceptable in terms of the data quality.

Chapter 6

Performance of the entire readout system

In this chapter, we discuss the performance of the entire readout system, considering the bandwidth of the backend DAQ and show the possible solutions of the readout system that depend on the background level. We also show the future prospects of the SVD system.

6.1 Performance of the entire readout system

In the previous chapter, we discuss the data sparsification on the reconstructed event timing (time cut) to keep the occupancy level below 10 % in the SVD readout system. In terms of the occupancy level, the system stands 32 times larger background than the current beam condition with applying the event timing cut.

However, for the performance of the entire readout system, the discussion on the data size is more important than that on the occupancy. At the harsh background level that is expected at SuperKEKB, the backend DAQ in the entire readout system would not work efficiently without the data size reduction. We study the time cut against the high background level with respect to the bandwidth [1]. We assume the occupancy and the trigger rate increase proportionally to the background level.

APV25 readout

Here, we discuss the performance of the DAQ system based on the APV25 readout. Figure 6.1 shows the data stream of the entire DAQ system with APV25 and shows two possible applications of the time cut, A or B.

In this system, the primary bottlenecks exist inside SVD FINESSE module. A LAN interface and the FIFOs on SVD FINESSE may not provide the sufficient bandwidth. Here we discuss the required bandwidth against the increase of the background. We assume that the data sparsification used in SVD2 is already applied at FADC with the same reduction factor [2] as of the SVD2 data sparsification.

Figure 6.2 shows the required bandwidth as a function of the relative background level to the current one. Figure 6.3 summarizes the tolerable background level of the APV25 readout system.

If the background level is below 9.3 times from the current level, the system works stably without the online time cut. In this situation, we apply the event timing reconstruction at the

[1] Bandwidth is defined as the data size that can be processed per time.

[2] The reduction factor in the space direction is a function of the trigger rate, the occupancy and the data size.

offline data processing (Case B in Figure 6.1.)

If the background level is above 9.3 times from the current level, the online time cut is necessary, since the bandwidth from the LAN interface at SVD FINESSE is not sufficient without the further data reduction at FADC. In this situation, we apply the event timing reconstruction at the online data processing (Case A in Figure 6.1.) With the tight time cut which keeps the efficiency 99.0%, the readout system works stably at least 15 times higher background level.

However, we expect that the limitation by the LAN interface can be removed easily by replacing it from 100Base-TX to 1000Base-TX, or by dividing the data stream in parallel. Without dividing the data stream, the readout system reaches to the critical limit at the 31 times higher background level than the current one. This is due to the limitation of the processing speed of SVD FINESSE, and the system no longer works without the data loss.

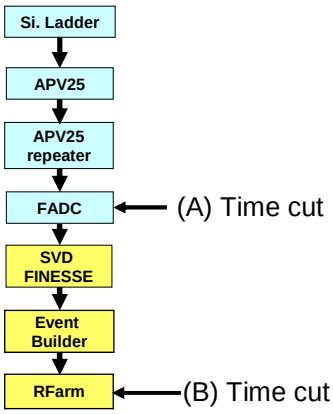

Figure 6.1: The data stream of the entire DAQ system with APV25 for SVD2.5/SVD3. We have two possible applications of the time cut, (A) at FADC (Online) or (B) at Reprocessing PC Farm (RFarm) (Offline.)

VA1TA readout for SVD2.5 [16]

Here, we discuss the performance of VA1TA readout system for SVD2.5. We use the values of the current trigger rate and the averaged occupancy of between Layer-3 and 4 to be 500Hz and 2.0%, respectively. We estimate the performance of the VA1TA readout system using the SVD2 experience. This system has mainly two bottlenecks: the bandwidth of the PCI link in the FADC readout, and the CPU power of the PC farm.

VA1TA readout system uses PCs to readout data from FADC and to perform data sparsification. PCI cards, which send data from FADC to PC, have their transfer performance, which we expect to work stably at 13 times or less background level than the current level.

As mentioned above, we sparse data on PC farm. The data processing speed must be faster than the trigger rate to catch up with the data transfer from FADC. From the SVD2 experience, we estimate that the system copes with 5.7 times larger background than the current level.

The VA1TA readout for SVD2.5 stands up to 5 times larger background level in terms of the occupancy, which is smaller than the limitation by the APV25 readout.

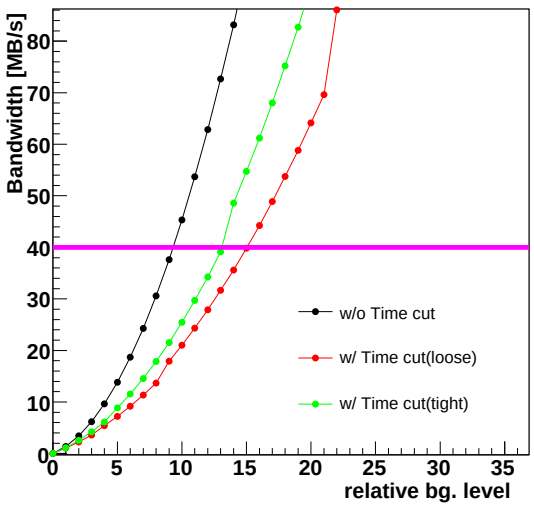

Figure 6.2: Required bandwidth as a function of the relative background level to the current level. We apply two levels of the time cut (See Figure 5.8.) The tight (loose) cut requires 99.0 (99.9)% efficiency. The black, the green and the red lines indicate the cases without the time cut, with the loose time cut and the case with the tight time cut, respectively. The pink line corresponds to the maximum bandwidth of the LAN interface. The critical maximum bandwidth on SVD FINESSE is 160MB/s.

6.2 Future prospects of the SVD system

To reduce the occupancy of SVD, there are two methods as mentioned in Section 5.1: replacing the sensor with a smaller sensitive area per readout channel, or applying a faster readout system.

In this thesis, we mainly discuss the latter method with APV25 readout and with the current DSSD assuming as the silicon sensor. From the discussions above, the readout system is expected to work at ∼30 times higher background level than at the current level using the online time cut.

If the new readout system suffers with much higher background level than the expected tolerable level, the fine segmentation of the sensor area per channel is necessary. There are some sensor options to obtain a small sensitive area: hybrid pixel detectors like LHC's and a dedicated new detector like Monolithic pixel detector (MAPS) [17]. In the former case, the technology is quite mature. The pixel size is large (from $150\times150\mu\mathrm{m}^2$ to $50\times450\mu\mathrm{m}^2$), which is constrained by the front-end electronics density factor and the interconnection technology. In addition, a thickness of each layer would exceed the reduction length of 1%. The huge number of readout channels is not also preferable in general. In the latter case, the technology is potentially very suitable for low-energy and high-luminosity collider experiments. However, it is still under development, such as the long readout time and the radiation weakness.

A double sided strip detector is the current best solution for us because of its low material and good position resolution at the present. To reduce the sensitive area and the detector capacitance, we consider a double sided detector with a shorter strip by a factor of 5, called *Striplet Detector* (See Appendix C.) With the striplet detector together with APV25, we can reduce occupancy by a factor of 5×30=150. The striplet detector plus APV25 readout system is our default option for the SVD3 upgrade.

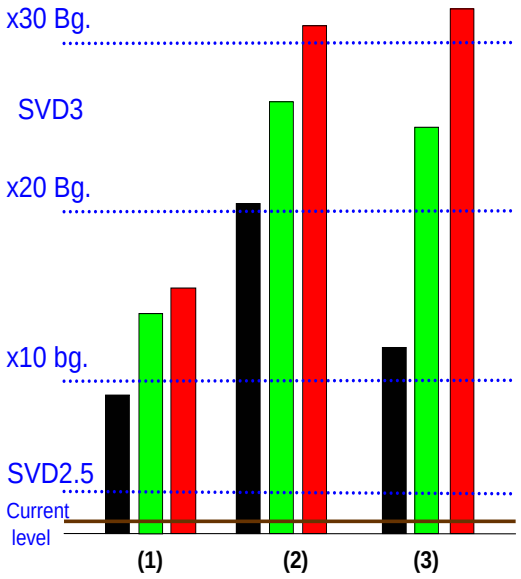

Figure 6.3: The tolerable background level of the APV25 readout system before and after the time cut. The black, the green, and the red bars correspond to the acceptable background level without the time cut, with the tight time cut, and with the loose time cut, respectively. Three sets of the three bars indicate the tolerable level with respects to the limits of (1) the bandwidth from the LAN interface of SVD FINESSE, (2) the bandwidth of the processing speed of SVD FINESSE and (3) Occupancy, respectively. The brown solid line and the blue dotted lines show the current background level and each relative background ones.

6.3 Summary of the performance of the entire readout system

We summarize the performance of the readout system and the future prospects of the SVD system.

SVD2.5 readout system

The SVD2.5 readout system is a combination of the APV25 for Layer-1 and 2 and the VA1TA for Layer-3 and 4. The acceptable background level is limited by the VA1TA readout system. In terms of occupancy, the system operates stably at 5 or less times higher background level than the current one. Concerning the DAQ system, the readout system no longer works without data loss at the 5.7 or more times higher background level than the current one.

SVD3 readout system

The SVD3 data from all the sensors is fully read out by the APV25s. Fig 6.3 shows the tolerable background level of the readout system before and after the time cut. We have two kinds of DAQ bottlenecks. One is the bandwidth of LAN interface at SVD FINESSE and the other is the bandwidth of the FIFOs on SVD FINESSE. At the 9.3 times higher background level, the online time cut is necessary due to the limitation of the bandwidth of LAN interface, which is expected to be solved with the technology improvement in the future. Using to the online time cut, the system is expected to stand 31 times larger background than the current one.

The less occupancy leads to the better detector performance, as shown in Figures 3.3

and 3.4. We can collect data with good quality with this powerful readout system under the harsh background level.

Future prospect of the SVD system

The new readout system copes with up to ∼30 times higher background level. If we aim much higher luminosity, the fine segmentation of the silicon sensor is also necessary. The dramatical improvement of the performance of a vertex detector comes mainly from the geometrical improvements, such as getting the Layer-1 closer to the collision point and getting a large acceptance. The combined system with the APV25 readout and with the fine-segmented striplet detector, will achieve the superb performance at an even higher luminosity experiment in the future.

Chapter 7

Conclusion

The Silicon Vertex Detector (SVD) has been a key device for measurements of all time-dependent CP asymmetries in B meson decays in the Belle experiment. To search for the new physics phenomena beyond the Standard Model through much larger number of rare B decays, the KEKB B factory is gradually increasing the luminosity by storing the larger beam current and employing the new cavities. To further extend reach to the new physics search, SuperKEKB, which will have 30 times higher luminosity than the current KEKB, is also planned.

Due to the increase of the excessive beam-induced background, the occupancy of the SVD will also be raised. We expect the occupancy of the current SVD will increase three times higher than the current one in 2008 and the performance will deteriorate to an unacceptable level.

To avoid this, we plan to upgrade the two innermost layers of the SVD (SVD2.5) employing the fast and pipeline readout chip, APV25, designed for the CMS experiment at LHC. In a full upgrade of the SVD (SVD3) for SuperKEKB, all layers employ the APV25 readout.

We have developed the APV25 readout scheme optimized for SVD. The scheme consists of the waveform sampling (Multi peak mode) and its reconstruction. We have evaluated the performance of the APV25-based readout scheme by the beam test at KEK 12GeV-PS. We confirm that the hit cluster properties of the Double Sided Silicon sensor with this APV25 readout scheme fully meet our requirement. We reconstruct the event timing with a time resolution of 3.0ns.

We have developed a sophisticated occupancy and data reduction method using the reconstructed event timing (Time cut.) We have studied the waveform reconstruction methods. We have performed the simulation study to evaluate the occupancy reduction power at the various background levels. Without the time cut, only 12 times larger background than the current one is acceptable even with the APV25-based readout system. With applying the time cut, the occupancy is expected to be kept at the current SVD2 level even under the 32 times higher background environment, while keeping the signal efficiency 99.0%.

At the severe background level at SuperKEKB, the backend DAQ in the entire readout system would not work efficiently without the data size reduction. For the APV25 readout system, the time cut is effective for the reduction of the data size, and widens the acceptable background level. By considering the bandwidth of the backend DAQ system, the APV25 readout system is expected to withstand 31 times larger background than the current one.

To summarize, we have developed the fast pipelined readout system for SVD upgrade (SVD2.5 and SVD3.) We employ the analog pipeline readout chip (APV25) in the core part of the readout system. We have designed APV25 readout scheme (Waveform sampling and reconstruction) for SVD and have developed the new occupancy reduction method using the reconstructed event timing. Through the beam test at KEK 12GeV-PS and the simulation, we have verified an occupancy reduction by a factor of 12 due to the shorter peaking time of APV25, and achieved an additional factor of 3 using the newly-developed occupancy reduction method. Considering to the entire SVD readout system, we conclude that this system can operate at 30 times higher background level than the current one, which satisfies the requirements of SuperKEKB.

Appendix A

History of CP violation

Until 1956, it was believed that all elementary processes are invariant under C and P. Lee and Yang pointed out the possibility of the violation of these symmetries [19], and subsequent experiments [20] proved that C and P symmetries are really not conserved in weak interactions. However, the products of C and P transformations, CP was still considered to be a good symmetry.

The second impact came in 1964. An experiment using neutral K mesons showed that CP is also not conserved under weak interactions [21]. Neutral K mesons (K^0 and $\overline{K}^0$) are created by strong interactions. The mass eigenstates of the K^0 - $\overline{K}^0$ system can be written

$$|K_S>= p|K^0> +q|\overline{K}^0>, |K_L>= |K^0> -q|\overline{K}^0> \tag{A.1}$$

(choosing the phase so that $CP|K^0>= |\overline{K}^0>$). If the CP invariance held, we would have $q = p$ so that K_S would be CP even and K_L would be CP odd. Because the kaon is the lightest strange meson, it decays through the weak interaction. Neutral kaons can decay into two or three pions. Since pion has CP eigenvalue of -1, K_S always decays into three pions, if CP is conserved in weak interactions. The experiment performed at Brookhaven proved that a small faction of K_L decays into two pions, which means CP is violated in the weak interaction. In the kaon system, the order of observed CP asymmetry is 10^{-3}.

This discovery stimulated many theoretical attempts to understand CP violation. A theory was proposed by M. Kobayashi and T. Maskawa, where CP arises in a natural way. They pointed out that an irreducible complex phase in quark mixing enables CP violation to take place, and it requires at least three generation of quarks. With discovery of the fourth and fifth quark, *cbquark*, in 1970's and the observation of top quark in 1995, it was shown that the key components for the Kobayashi-Maskawa (KM) Model [22] exist. A quark mixing matrix which projects one set of states onto the other was proposed and now is called *Cabibbo-Kobayashi-Maskawa* (CKM) matrix. If the CKM matrix is unitary, there relations between the elements of CKM matrix which can be described as *Unitary Triangles*. Providing precise measurements of the sides and angles of the unitary triangles are good tests of the KM model. A. Carter, I. I. Bigi, and A. L. Sanda [23] suggested that KM mechanism could lead to possibly large CP violation in B meson system. Sizable CP asymmetries can be extract from the time-dependent decay rate difference between $B^0\bar{B}^0$ to a common CP eigenstate. Such measurements have been made at an asymmetric e^+e^- colliders at $\Upsilon(4S)$ resonance was proposed and carried out in two experiments, the Belle in Japan and the BaBar in U.S.A.

In the summer of 2001, the presence of CP violation in the B meson system was established by the Belle [18] and simultaneously by the BaBar [24] through the measurements of the time dependent asymmetry in the decay process B^0 ($\overline{B^0}$) $\rightarrow J/\Psi K^0_S$. The experimental data

indicated that the Kobayashi-Maskawa mechanism is indeed the dominant source of observed CP violation in $Nature$.

Appendix B

Measuring CP Asymmetry in B Meson Decays

B meson can be produced in two energy regions, a center-of-mass energy equal to the $\Upsilon(4S)$ mass or higher center-of-mass energy.

There are some advantages of producing B mesons at the $\Upsilon(4S)$ energy region. The $B\overline{B}$ cross section is higher than center of mass energy. $B-\overline{B}$ pairs are exclusively produced (50% $B^0\overline{B}^0$ and 50% B^+B^-). The energy of the produced B meson is known, which can be used to reduce the combinatorial background. One of the most promising methods to measure CP angles in the B meson system is based on neutral B decays to CP eigenstates f_{CP} which are common to B^0 and $\overline{B}^0$. B^0 and $\overline{B}^0$ can mix through the loop diagrams shown in FigureB.1 i.e. after a certain time, a meson which was B^0 at production will not be a pure B^0 state, but a mixed state of B^0 and $\overline{B}^0$. CP violation is induced by $B^0-\overline{B}^0$ mixing through the interference of the two decay amplitudes of B^0, $A(B^0 \to f_{CP})$ and $A(B^0 \to \overline{B}^0 \to f_{CP})$. In order to detect this CP violation, one must know, or *tag* the flavor of the particle (B^0 or $\overline{B}^0$) at a given time.

On the $\Upsilon(4S)$, tagging one B as a B^0 or a $\overline{B}^0$ identifies the other with certainty. Since both C and P eigenvalues of $\Upsilon(4S)$ is -1 and the decay of $\Upsilon(4S)$ is caused by strong interaction which conserves CP, produced $B-\overline{B}$ should be in a CP eigenstate with eigenvalue of 1. Because spin of $\Upsilon(4S)$ is 1 and that of B is 0, B^0 and $\overline{B}^0$ mesons are produced with the orbital angular momentum of 1, which means the P eigenvalue of $B-\overline{B}$ system is -1. This restricts the C eigenvalue to be -1 and a $B\overline{B}$ pair will remain in a coherent $B\overline{B}$ state as long as neither B has decayed. If one of them is detected to be $B^0(\overline{B}^0)$ at a moment, the other is inevitably $\overline{B}^0(B^0)$ at that time. This is extremely important for measuring CP violation.

For example, consider one B^0 from $\Upsilon(4S)$ decays into semi-leptonic mode, like $B \to D^*\ell\nu$ ($\ell = e$ or μ), after t_1 from its production. If that particle was $B^0(=\overline{b}d)$ at t_1, the charge of lepton is positive (see FigureB.1) and if it was $\overline{B}^0(=b\overline{d})$, the charge of lepton is negative. Thus one can tag the flavor of B mesons by detecting leptons from $B_{\rm S}$.

When the $B^0-\overline{B}^0$ pair is produced with odd relative angular momentum, the rate for one of the neutral B mesons to decay as $\overline{B}^0$ at $t = \ t_1$ and the other (which is B^0 at $t = t_1$) to decay into CP eigenstate, for example $J/\psi K_S$, at $t = t_2$ is written as

$$P(B^0 \to J/\psi K_S; \Delta t) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 + \lambda \sin \Delta m \Delta t) \tag{B.1}$$

where Γ is the B meson total decay width, $\Delta t \equiv t_2 - t_1$, Δm is the mass difference between the two neutral B weak eigenstates and λ is the CP asymmetry parameter

$$\lambda = -\sin(2\phi_1). \tag{B.2}$$

The CP conjugate of this function is

$$P(\overline{B^0} \to J/\psi K_S; \Delta t) = \frac{1}{2} e^{-\Gamma|\Delta t|}(1 - \lambda \sin \Delta m \Delta t). \tag{B.3}$$

The Δt value ranges are from $-\infty$ to ∞ and it is easily seen that CP asymmetry vanishes in the time integrated rate. Therefore, the measurement of decay time difference, Δt, is required to observe CP asymmetry in experiments at the $\Upsilon(4S)$.

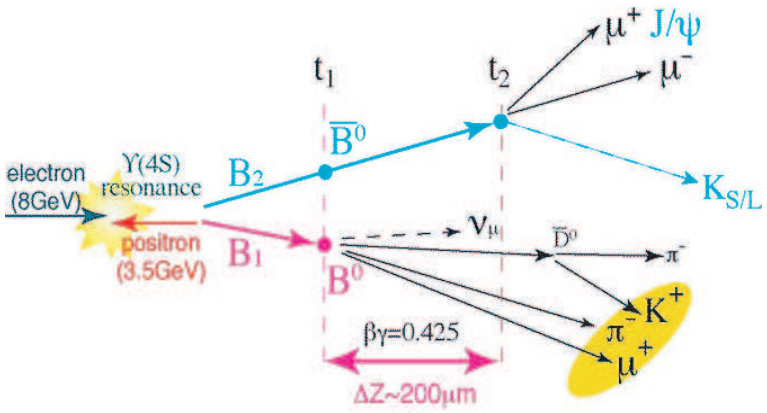

Figure B.1: Event topology

Appendix C

Short Strip detector with UV coordinate

To reduce occupancy, we require fine segmentation of the detector both space-wise and time-wise. Considering the various technical difficulties in pixel detectors, the idea of DSSD with short strips (so-called *Striplet Detector*) is attractive because the technology of DSSD sensors has been established for a long time. If the stripes are placed at an angle of 45 degrees with respect to the DSSD outer shape, the strip length becomes $\sim$1.4 times the sensor width. By introducing the strip configuration with a 45-degree slant angle, the strip size becomes 11mm$\times$50μm. Comparing this shape with normal strip shape, 71mm$\times$50μm, we can expect to reduce the occupancy by a factor of 5. Schematic drawings of the striplet sensor and the strip sensor are shown in Figure C.1. Here, we summarize the merits and the demerits of a striplet detector.

Merits

- Small Sensitive Area per channel
- Small detector capacitance
  Thanks to the small capacitance, the noise of a chip can be small.
- PN sides correlation
  The cluster properties of PN sides, for example PN cluster width, have some correlations, which may help hit finding and remove fake clusters

Demerits

- Dead region
  Due to the existence of the readout pads and polysilicon bias registers, the length of the shortest strips are 2mm. Due to this limitation, triangle dead regions exists in the lower-left and upper-right corners.
- Increase of their readout channels
  By reducing the sensitive areas of each channel, the total number of readout channels increases. The development of a high density readout by using multi-layer kapton film will be necessary for the readout of the striplet sensors.
- Modification of our tracking programs
  We have a lot of offline data processing programs that have been developed and established

since the commissioning of the Belle experiment. However, if we employed a striplet sensor, we would have to modify our programs.

We developed a striplet sensor as a option for SuperB Vertex detector. As a guideline of SVD2.5 upgrade, the modification of our offline programs should be minimized. And the area of the dead region is too large to discard. By just adopting a readout chip with a shaping time 16 times faster than SVD2 readout, the tolerance to background, in other words, occupancy, can be improved without employing a striplet sensor. Therefore, we prefer a normal DSSD sensor to a striplet sensor as a sensor for SVD2.5.

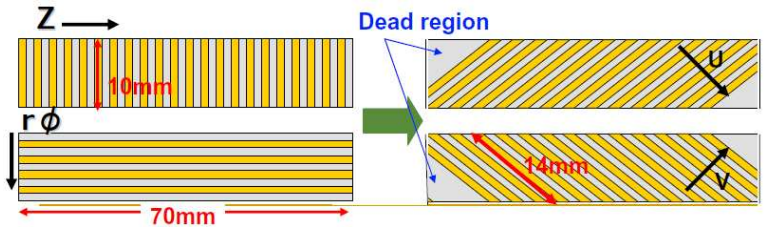

Figure C.1: A schematic drawing of the strip sensor (left) and the striplet sensor (right.)

Acknowledgement

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