Performance Evaluation of Readout Chip for Silicon Vertex Detector for SuperBelle

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Abstract

In order to search for new physics phenomena beyond the Standard Model a major upgrade of the existing Belle detector, referred to as " SuperBelle ", is planned. The primary luminosity target of SuperKEKB, the collider that will be used to produce the luminosity for SuperBelle, is set to $2.0 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

One of the problems under this higher luminosity is the increased beam background caused by synchrotron radiation and beam-gas scattering. In particular, because the Silicon Vertex Detector (SVD) located in the innermost part of the Belle detector is exposed to harsh beam background, an upgrade of SVD is necessary for SuperBelle. With this upgrade, the current VA1TA readout chips are to be replaced with APV25 readout chips, which have a peaking time of 1/16th of that of VA1TA. Thanks to this shorter peaking time we expect a reduction in the occupancy - a measure of the number of background related hits in the SVD.

In order to confirm and evaluate this occupancy reduction due to APV25 we held radioactive source tests and found that the occupancy of APV25 is reduced by a factor of 11.4 relative to VA1TA. Furthermore we estimated the performance of SVD with APV25 for a specific physics mode of $B \to J/\psi K_S$ by utilising a simulation study. The resolution of the distance between the two B decay vertices, which is a directly related to the precision of the measurement of CP asymmetry in the B meson system, was determined from this study. We confirmed that the upgraded SVD achieves good position resolution and satisfies the requirements for the first phase of the SuperBelle upgrade.

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Chapter 1

Introduction

The Standard Model (SM) is a quantum field theory of quarks, leptons, and gauge bosons based on the $SU(2) \times U(1)$ local gauge symmetry. Over the past thirty years, the SM has been confirmed by many experiments. The SM made remarkable success.

However, in higher energy region, existences of new physics (NP) beyond the SM are strongly believed. Many theories beyond the SM [1, 2] are waiting for new experimental discoveries.

There are roughly two approaches to discover NP phenomena beyond the SM in collider experiments.

One approach is to construct energy-frontier collider to make heavier particles directly. For example, Large Hadron Collider (LHC) will start operation in 2009. LHC is anticipated to discover Higgs particle, and other new particles such as supersymmetry (SUSY) particles. In this energy-frontier approach, International Linear Collider (ILC) is also being planned.

Another approach is to build luminosity-frontier collider to make precise measurements to look for new physics effects. For this end, the Flavor-Changing-Neutral-Currents (FCNC) in B meson decays, such as the radiative decay $b \to s\gamma$, the semileptonic decay $b \to sl^+l^-$, and the hadronic decays $b \to s\bar{q}q$ and $b \to d\bar{q}q$ are suitable. All of these processes are suppressed in the SM by the GIM mechanism, and therefore the NP effects are relatively enhanced. These measurements are

realized by the higher luminosity B factory, and the comprehensive studies of B meson decays in clean e^+e^- environment.

Therefore, the latter is the mission of SuperBelle [3], a major upgrade of Belle [4]. The designed luminosity L of SuperKEKB, the collider for SuperBelle, is $4.8 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Figure 1.1 shows the projected luminosity in SuperKEKB. New observables that are currently out of reach will be accessible by this luminosity. In addition to B meson decays, FCNC processes in τ and charm decays will also be studied at SuperBelle.

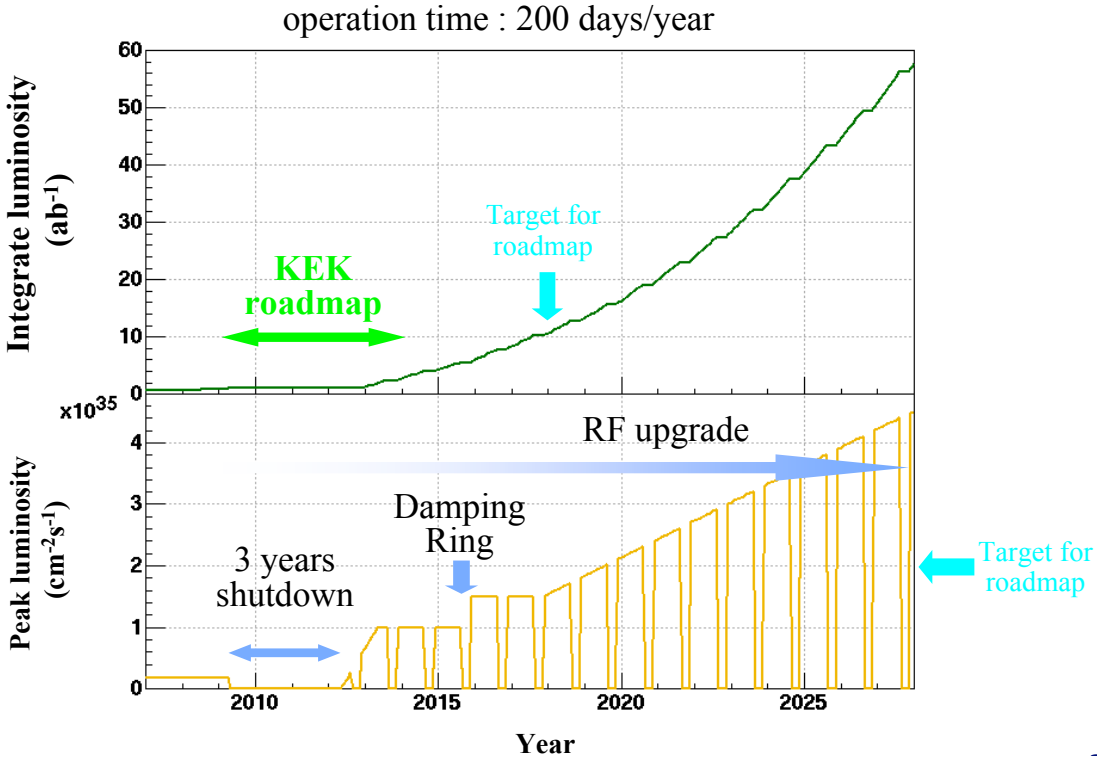


Figure 1.1: Projected luminosity in SuperKEKB

To accomplish these studies, there are several problems to overcome. One of the most difficult problems for luminosity-frontier collider is beam background. Because beam background is caused by synchrotron radiation and beam-gas scattering, it is inevitable that the increase of the luminosity leads to the increase of the beam background.

In Belle detector, beam background is especially serious at Silicon Vertex Detector (SVD). Since

SVD is a detector to determine B meson decay vertices, it is placed at the innermost part of Belle detector (closest to the beam interaction point), and required high position resolution ($\sim$100 μm). Because of the location, SVD is exposed to harsh beam background, and its resolution gets worse.

As Figure 1.2 shows, in SuperBelle under L=2.5 $\times$ 10^{35}cm^{-2}s^{-1}, the beam background on SVD will be about 13 times of current Belle. Under such beam background, current SVD can no longer keep its performance.

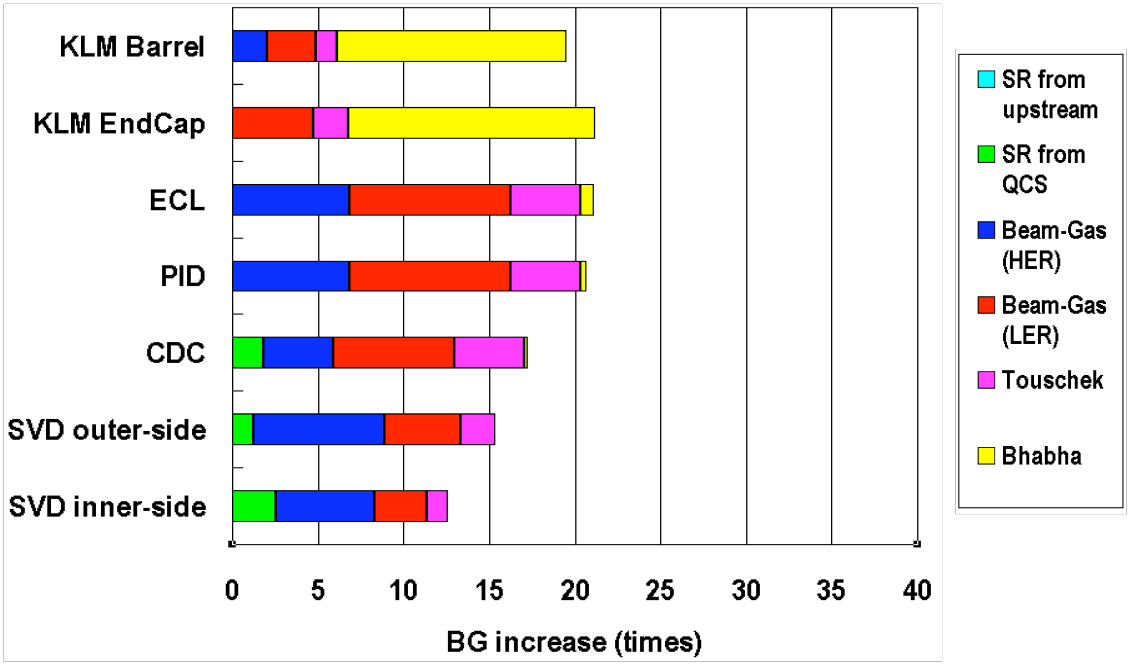


Figure 1.2: Expected beam background level in SuperBelle under 2.5 $\times$ 10^{35}cm^{-2}s^{-1} luminosity (normalized by that of the current Belle)

To cope with this problem, upgrade of SVD is planned for SuperBelle. In this upgrade, readout chips are replaced, from current VA1TA to APV25. As Figure 1.3 shows, since APV25 has 16 times shorter pulse width than that of VA1TA, the rate of timelike overlapping of beam background pulses will decrease accordingly. Accidental coincident hits on SVD will decrease similarly.

Here we define a value "occupancy" as the number of hit channels divided by the number of all channels;

$$Occupancy = \frac{Number\ of\ hit\ channels}{Number\ of\ all\ channels}. \tag{1.1}$$

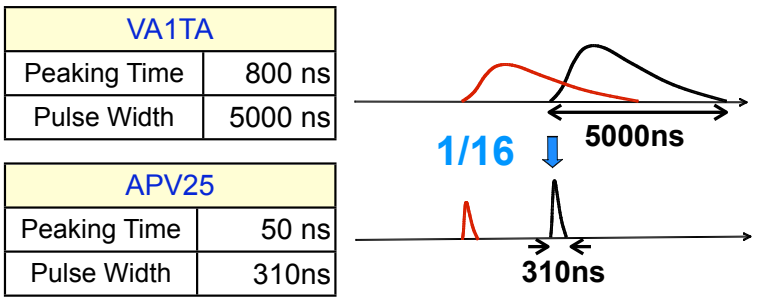


Figure 1.3: Schematic view for the reduction of overlapping of pulses by shortening of the pulse width

That is, we expect APV25 to reduce occupancy and to reduce position resolution.

In order to evaluate and confirm this occupancy reduction of APV25, we have hold beam line tests, radioactive source tests and simulation studies.

The purpose of this thesis is to estimate and discuss the performance of APV25 under high beam background condition. We describe the outline of Belle and SuperBelle experiments in Chapter 2, the details of SVD upgrade in Chapter 3, the performance evaluation of APV25 by radioactive source tests in Chapter 4, the performance estimation of APV25 by simulation studies in Chapter 5 and the summary in Chapter 6. The performance evaluation of APV25 by beam line tests is described in Appendix A.

Chapter 2

Belle and SuperBelle Experiments

2.1 Physics of the Belle experiment

Since the first observation of CP violation in the K^0 system in 1964 [5], an enormous amount of theoretical work has been done trying to understand the phenomenon. In a remarkable paper published in 1973, Kobayashi and Maskawa (KM) noted that CP violation could be accommodated in the Standard Model only if there were at leat six quark flavors [6], which is now considered to be an essential part of the Standard Model.

In 1980, Sanda and Carter pointed out that the KM model contained the possibility of rather sizable CP violating asymmetries in certain decay modes of the B meson [7]. In order to discover this sizable CP violating asymmetries in the B meson system, the Belle experiment at an asymmetric e^+e^- collider, the KEKB collider, commenced in 1999. An asymmetric collider such as KEKB that is able to produce large number of B mesons is referred to as a "B-factory"

At a B-factory, it is predicted that a CP violating asymmetry can be observed in the time-dependent partial decay rates for B^0 and $\bar{B}^0$ decays to a common CP eigenstate "f_{CP}", which is generally written as:

$$\begin{aligned} A(t) &\equiv \frac{\Gamma(\bar{B}^0 \to f_{CP}) - \Gamma(B^0 \to f_{CP})}{\Gamma(\bar{B}^0 \to f_{CP}) + \Gamma(B^0 \to f_{CP})} \\ &= S_{f_{cp}} \sin \Delta m_d t + A_{f_{cp}} \cos \Delta m_d t, \end{aligned}$$

$$S_{f_{cp}} = \frac{2Im\lambda}{|\lambda|^2+1} \text{ and } A_{f_{cp}} = \frac{|\lambda|^2-1}{|\lambda|^2+1},$$

where $\Gamma(\bar{B}^0\ (B^0) \to f_{CP})$ is the decay rate for a $\bar{B}^0(B^0)$ to f_{CP} at a proper time t after production, and Δm_d is the mass difference between the two B^0 mass eigenstates. The $A_{f_{cp}}$ and $S_{f_{cp}}$ are expressed with a complex parameter, λ, that depends both on $\bar{B}^0 - B^0$ mixing and on the amplitudes for $\bar{B}^0(B^0)$ decays to specific CP eigenstates. In the SM, $|\lambda|$ is equal to the absolute value of the ratio of the $\bar{B}^0$ and B^0 decay amplitudes to a good approximation, and for most CP eigenstates it is approximately equal to 1.

In the summer of 2001, the presence of CP violation in the B meson system was established through the measurement of the time dependent partial decay rate asymmetry in the decay process $B \to J/\psi K_S$ [8]. This measurement was the main target of the Belle experiment, and it was achieved as originally planned.

Since then, the Belle experiment has measured a number of decay modes of the B meson and to extract Cabibbo-Kobayashi-Maskawa (CKM) matrix elements. For instance, the measurement of the angle ϕ_1 of the unitarity triangle through the $B \to J/\psi K_S$ time-dependent asymmetry has reached a precision of better than 10% [9].

2.2 Motivation of the SuperBelle Experiment

The results from Belle experiment are in good agreement with the constraints from the KM model of CP violation. However, if the new physics beyond the SM exists, their influence on various aspects of B decays should theoretically be measurable. For example the precise measurement of the time-dependent CP asymmetries in a pure $b \to sq\bar{q}$ process would be expected to show a deviation from the CP asymmetry in a $b \to c\bar{c}s$ process like $B \to J/\psi K_S$ decay. The next target of the SuperBelle experiment is to search for new physics phenomena like the above. For this purpose, we need to upgrade the current KEKB accelerator and Belle detector. These upgraded machines will be referred to as the SuperKEKB accelerator and the SuperBelle detector, respectively.

2.3 SuperKEKB accelerator

To explore new physics beyond the SM, the primary luminosity target of SuperKEKB is set at $2 \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

The SuperKEKB collider will be constructed by re-using most of the components of the present KEKB, in particular the ring magnets and the klystrons used to supply RF power to the cavities. However, there are also many components that need to be modified or newly developed. For instance, in order to achieve the primary luminosity target, the beam current of the low energy ring (LER) needs to be increased to approximately 10 A. A higher beam current implies a larger power loss due to synchrotron radiation, which makes the design of the RF system and the vacuum system challenging.

Now the design of accelerator and the machine parameters are being studied. The detail can be found elsewhere [10].

2.4 SuperBelle detector

The SuperBelle detector will be an upgraded version of the present Belle detector so that it can take full advantage of the high luminosity of SuperKEKB. For this upgrade, the detector performance should be at least as good as the present Belle detector in spite of harsh beam backgrounds, and some improvements are envisaged. Though the detector upgrade is still in the design phase, feature upgrades planned at this stage are briefly summarized below, and the conceptual illustration of the upgraded Belle detector is shown in Figure 2.1. Other detail can be found elsewhere [11].

Vertexing

The Silicon Vertex Detector (SVD) finds the vertex of charged particle tracks with precise resolution. In SuperBelle, the SVD with a shorter shaping time than the current SVD can have smaller occupancy for the same background level. To realize this, new readout chips

called APV25 described in Section 3.2.1 will be used. The shaping time of APV25 is 1/16 of the shaping time of current VA1TA chip. With this lower occupancy, the innermost layer may be moved even closer to the interaction point without any loss of vertexing performance, even if the beam background level is increased by 13 times.

Tracking

The Central Drift Chamber (CDC) detects charged particle tracks and used to reconstruct their momenta. The hit loss rate due to overlapping background hits could be reduced by shortening the time constant in the electronics. Further reduction can be accomplished by using the drift cells of half the present size.

Calorimetry

The Electromagnetic CaLorimeter (ECL) measures the energy and position of photons and electrons from B meson decays. The present background level observed in the end-cap calorimeter is high, and an upgrade to another advanced technology is necessary. Among several candidates, pure CsI crystals with photo-tetrode readout is the most promising choice for the end-cap electromagnetic calorimeter. It will consist of 16 X_0 long pure CsI crystals.

Particle identification

For a particle identification device, the upgrade will be undertaken not only for higher tolerance against background but also for much better K/π discrimination in the momentum range up to 4 GeV/c. Specifically, reduction of material in front of the calorimeter and allocation of more tracking volume for the CDC is being planned. Among several options, the DIRC technology with the Time of Propagation (TOP) scheme is a good candidate for the barrel part while RICH technology with an aerogel radiator is being considered for the end-cap. The K_L^0 and Muon detector (KLM) detects K_L^0 's and identifies muons by measuring their positions.

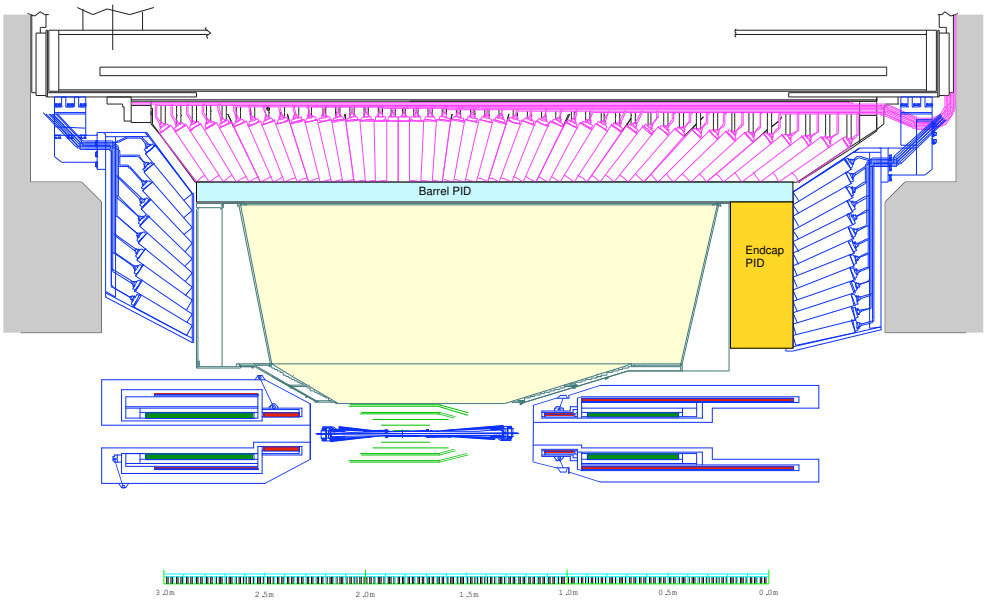


Figure 2.1: Conceptual illustration of the upgraded Belle

Chapter 3

The Silicon Vertex Detector (SVD)

In this chapter, we describe first the SVD system used in the current Belle experiment. Next we discuss the performance of the SVD under higher beam background conditions. Finally, we propose an upgrade of the SVD for the SuperBelle experiment.

3.1 The current Belle SVD

3.1.1 Overview of SVD2

To cope with high radiation (See Chapter 1), the SVD has been upgraded several times since the original commissioning of the Belle experiment. The most recent major upgrade was performed in the summer of 2003, to a detector called "SVD2".

SVD2 consists of four layers of detector ladders. Each ladder is made up of Double-sided Silicon Strip Detectors (DSSD's) and hybrid boards. The analog signal from the DSSD is read out by the VA1TA chip (described in Section 3.1.3) located on the hybrid board.

Figures 3.1, 3.2, 3.3 and 3.4 show the outside view, the ladder structure, the side view diagram and the end view diagram of SVD2, respectively. The characteristics of SVD2 are listed in Table 3.1. The typical trigger rate is ∼400Hz and the average occupancy of the SVD is around 3 %.

Under these conditions, the performance of SVD2 is sufficient, as summarized in Table 3.2.

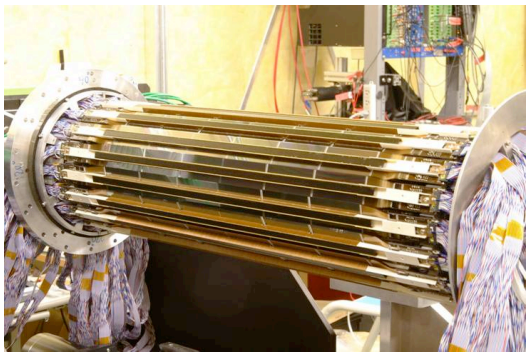


Figure 3.1: Outside view of SVD2

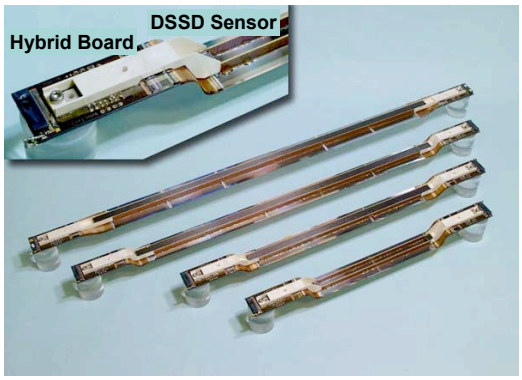


Figure 3.2: Ladder structure of SVD2

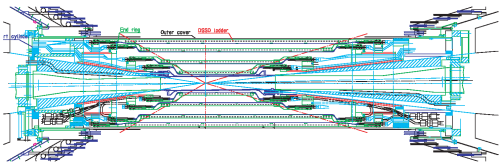


Figure 3.3: Side view diagram of SVD2

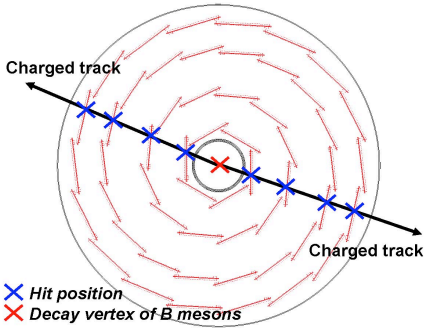


Figure 3.4: End view diagram of SVD2

3.1.2 DSSD

For SVD2, we use the DSSD as the sensor pad. Figure 3.5 shows a diagram of the structure of the DSSD. The DSSD consists of 512 N^+ strips in one side (N-side) and 1024 P^+ strips in the other side (P-side), which are mutually perpendicular. Since the silicon bulk is made from N type semiconductor, P-stops are implanted surrounding each N^+ strip to insulate neighboring strips electrically. At the operation, a bias voltage (N-side +40V: P-side -40V) is applied to the DSSD for the complete depletion. A charged particle passing through the DSSD deposits energy in the sensor and generate electron-hole pairs along its path. Since the electrons have negative charge, they are collected by N^+ strips, and holes will be collected by the P^+ strips. They are observed as electric signals, and hit position of the particle in z direction is read by P-side strips and ϕ direction is read by N-side strips. When a charged particle penetrates with a large incident angle, the signal is

Beam pipe radius [mm]	15
Number of layers	4
Number of DSSD ladders in layers 1/2/3/4	6/12/18/18
Number of DSSD's in a ladder in layers 1/2/3/4	2/3/5/6
Radii of layers [mm] in layers 1/2/3/4	20.0/43.3/70.0/88.0
Angular coverage (acceptance)	$17^\circ < \theta < 150^\circ$ (0.92)
Active area [mm^2] per sensor	76.8×25.6 (73.8×33.3 for Layer-4)
Total number of channels	110592
Strip pitch[μm] for ρ(z)-side	75 (73 for Layer-4)
Readout pitch[μm]	150 (146 for Layer-4)
Strip pitch[μm] for n(rϕ)-side	50 (65 for Layer-4)
Readout pitch[μm]	50 (65forLayer-4)
DSSD thickness [μm]	300
Total material at θ=90° [X_0]	2.6
Readout chip	VA1TA
Readout scheme	Track and Hold
Intrinsic DAQ dead time/event [μs]	25.6

Table 3.1: Characteristics of SVD2

Parameter	
S/N	>16
Occupancy [%] in layers 1/2/3/4	10/3.5/2.0/1.5
Hit detection efficiency [%]	90
Impact parameter resolution [μm] for dz	$26.3 \oplus 32.9/(p\beta(\sin\theta)^{\frac{5}{2}})$
Impact parameter resolution [μm] for dρ	$17.4 \oplus 34.3/(p\beta(\sin\theta)^{\frac{3}{2}})$

Table 3.2: Performances of SVD2

distributed over sequential strips. In this case, the position is determined by calculating the center of gravity of energy deposits in the strips. Table 3.3 shows specifications of the DSSD.

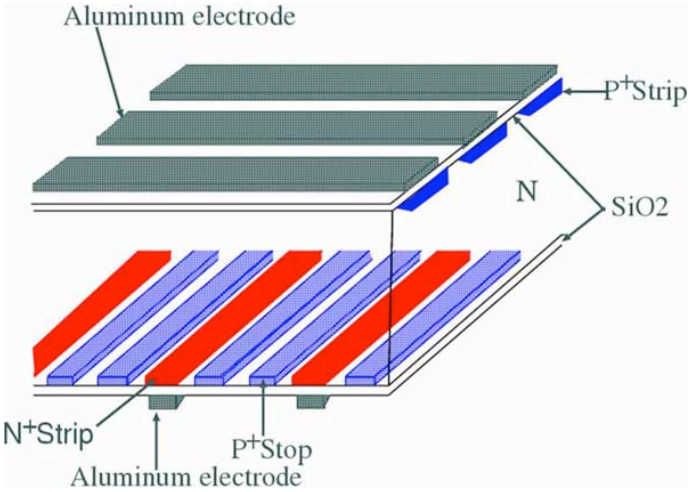


Figure 3.5: Structure of a DSSD

	Layer1-3		Layer4	
	P-side	N-side	P-side	N-side
Chip size [mm]	$79.6 \times 28.4 \times 0.3$		$76.4 \times 34.9 \times 0.3$	
Active area [mm]	76.8×25.6		73.8×33.3	
Strip pitch [μm]	75	50	73	65
Number of strips	1024	512	1024	512
Readout pitch [μm]	150	50	146	65
Strip width [μm]	50	10	55	12
Readout electrode width [μm]	56	10	61	10

Table 3.3: Specifications of the DSSD

3.1.3 VA1TA

For SVD2, the signal from the DSSD is read out by the LSI chip called VA1TA (Figure 3.6). One VA1TA has 128 readout channels. One hybrid board has four DSSD's, and has 512 readout channels in total. Figure 3.7 shows a diagram of VA1TA. The VA1TA consists of VA part for amplifying signal, and TA part for triggering. When a charged particle penetrates the DSSD and the electric charge is generated on the strips, the charge is converted into a voltage with a preamplifier and then integrated by a shaper. This shaper makes a pulse with a peaking time of 800 ns and a full

pulse width of 5000 ns. When an external trigger causes the HOLD state to be asserted, the analog information from all channels is captured and then sequentially read by a single line through a multiplexer. If a level-1 [1] trigger does not occur within 1.2 μs, the HOLD state is deasserted and the system is immediately ready for another event. If the level-1 trigger fires, a readout sequence starts.

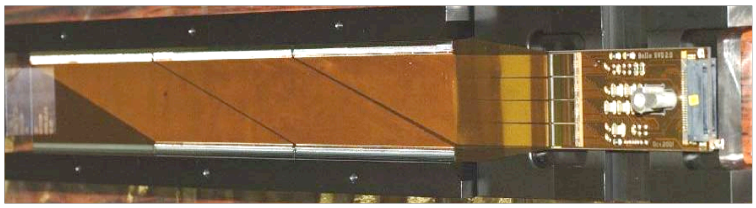


Figure 3.6: DSSD's and a hybrid board with four VA1TA chips

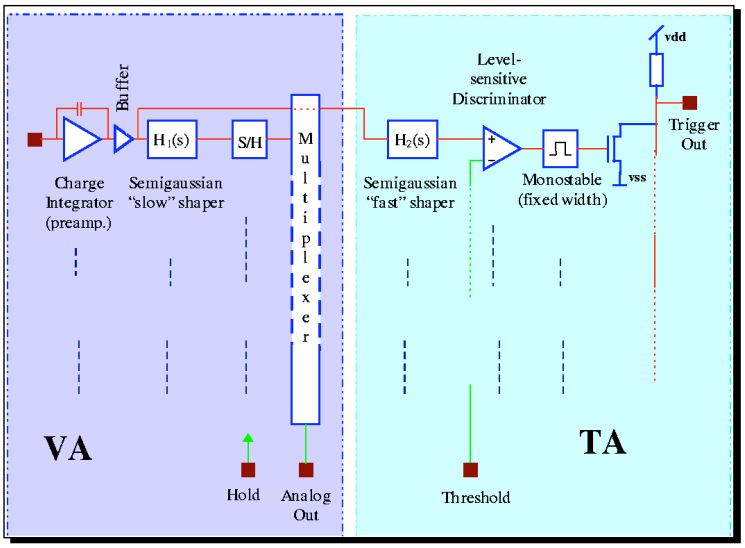


Figure 3.7: Diagram of VA1TA

3.1.4 VA1TA readout system in Belle experiment

Figure 3.8 shows VA1TA readout system. The function of each module is as follows:

CORE (COntrol and REpeater) system

[1] The level-1 trigger is a hardware trigger which consists of track triggers and energy triggers provided by the sub-detectors.

CORE consists of six repeater boards called REBO. The REBO sends the control signals or receives the analog signals from the VA1TA. MAMBO is the mother board which controls the REBO. The MAMBO also controls the power supply. The CORE system is encapsulated in a copper cooling box and it is called DOCK. The REBO is able to read 4 hybrids' data, and six REBOs and one MAMBO are placed in the DOCK. A total of ten DOCKs are used for the readout of the SVD.

FADC (Flash ADC)

FADC is a 9U VME module that converts the analog signal from REBO into a digital signal at 5MHz, and send it to a PC via a PCI control. One FADC can read six hybrids' data. In the SVD2, there are thirty-six FADC modules in total, eighteen module are used for the N-side readout and the other eighteen are used for the P-side readout.

TTM (Trigger Timing Module)

TTM is a 6U VME module that controls the trigger signal and the DAQ system. TTM can send a signal such as ADC start, ADC stop, busy, and 4-bit event tag to the REBO and FADC, and it monitors and controls the readout cycle of the data. There are eleven TTM modules in total.

Power supply

Power supply provides both High Voltage (HV) and Low Voltage (LV). The HV is the bias voltage applied to the DSSD's for depletion. The LV is used for front-end electronics. One each of HV and LV supplies is utilized for each DOCK, and there are ten modules in total.

DAQ system

Twelve PC's in total are used in the DAQ system for the SVD. It reads the data sent from FADC via the PCI bus. Sparsified data are then sent to the Belle event builder. Each PC has three PCI boards and can read the data from three FADC modules.

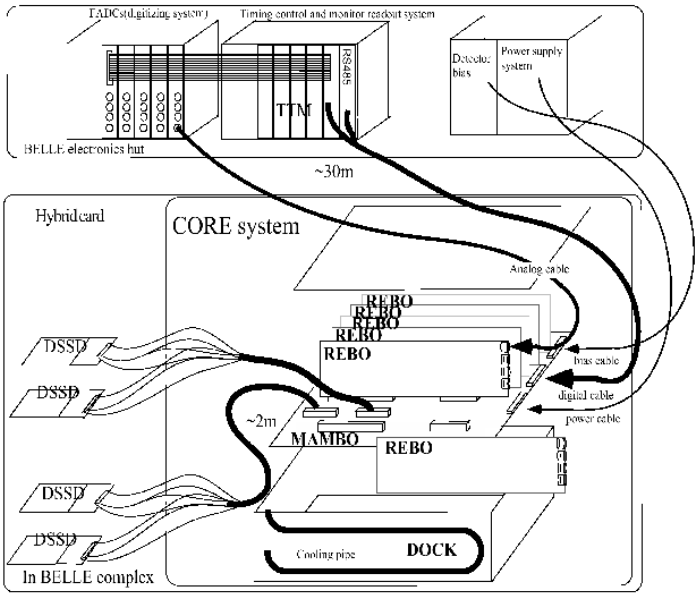


Figure 3.8: VA1TA readout system

3.1.5 Expected degradation of the performance of the SVD2 under the higher beam background

At the current background level, the average occupancy of Layer-1 (Layer-2) is 10% (3.5%) at L_{peak} = 10^{34} cm^{-2}s^{-1}. Since almost all the SVD hits are due to the beam background, the occupancy increases proportionaly to the background level . At the 13 times background level of SuperKEKB relative to the current Belle, the occupancy would reach 100%, and the current SVD would no longer work.

For example, when the background-originated clusters are wrongly associated with the track in the tracking procedure, the trajectory cannot be reconstructed properly. As an another example, if the background-originated clusters are overlapped with the signal-originated clusters, cluster shape could be distorted. The reconstructed track using this distorted cluster shows worse resolution.

In order to avoid these effects, occupancy should be kept below a value of 10%. Though the clustering and tracking software improvements may help to improve the situation, it is essential to reduce occupancy by upgrading the hardware.

3.2 Upgrade of SVD for SuperBelle

We are planning to upgrade the SVD for the SuperBelle. Major change in this upgrade is the replacement of the readout chip, from VA1TA to APV25. We describe our strategy with APV25 below.

3.2.1 APV25

The APV25 has the following major differences from VA1TA.

- **Shorter peaking time (50ns)**

  The peaking time of APV25 is 50 ns, and the full pulse width is 310 ns. Since the pulse width is 16 times shorter than that of VA1TA, we expect APV25 to have lower occupancy.

- **Pipeline memory and sequencer**

  These pipeline memory and sequencer enable us to record the pulse shape information of events. By making the most of this information, we can remove the overlapped background pulses.

These features are realized by the following mechanism: As shown in Figure 3.10, APV25 consists of 128 sets of preamplifier, shaper and pipeline, and a multiplexer. The shaper output is sampled at clock intervals and stored in the pipeline. The pipeline of the APV25 is a ring buffer which has 192 cells with cycling write and read pointers. The signal stored at the pipeline is read after a certain constant latency time. The latency time between the signal input and the trigger is more than 4 μs with 40 MHz clock frequency. APV25 has the sequencer that can generate a series of subsequent APV triggers initiated by a single hardware trigger. By using this feature, a sequence of samples can be readout every 25 ns (multi-sample mode). This can be used to effectively get subsequent samples of the shaping curve from particle signal. The output signal from one APV chip in multi-sample mode is shown in Figure 3.11.

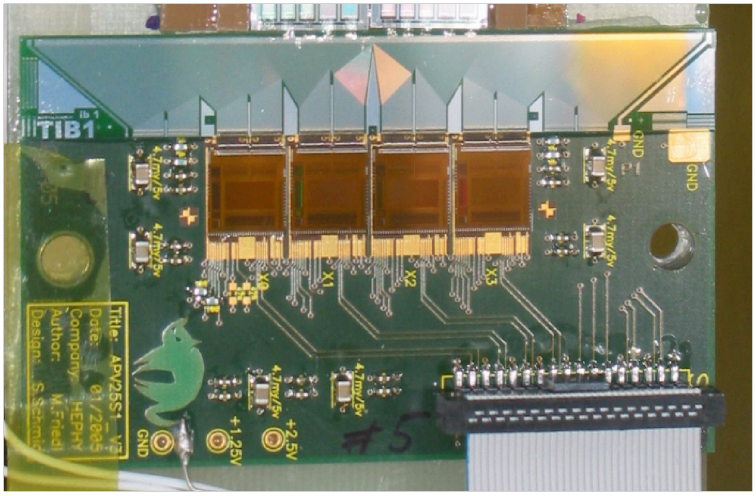


Figure 3.9: Hybrid board with four APV25 chips

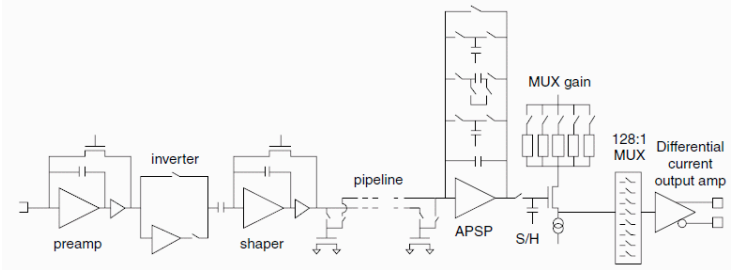


Figure 3.10: Circuit diagram of APV25

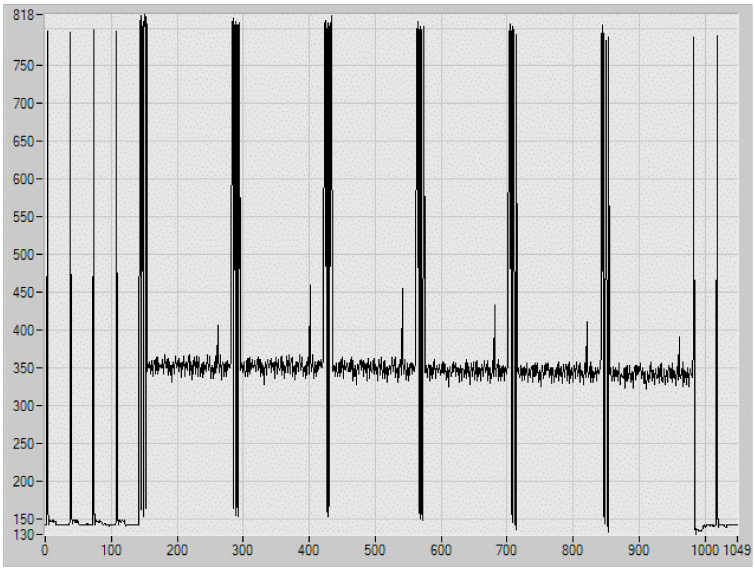


Figure 3.11: Output signal from APV25 in a 6 point multi-sample mode

3.2.2 APV25 readout system in R&D tests

Figure 3.12 shows the APV25 readout system. The output from the APV25 chips are fed to APVDAQ through the AC-coupled repeater.

The APVDAQ (Figure 3.13) is a 6U VME module used for the control and readout from the APV25 chip. It consists of a Stratix Altera, a VME protocol Altera, an ADC daughter board and supplemental electronics. On the front panel of APVDAQ, there is an analog signal input and an output for the controls (clock, trigger etc.), and these are connected to the repeater with a flat cable and CAT7 cables respectively. Furthermore, there is an external clock input and a trigger input on the front panel.

The AC-coupled repeater is an interface between the hybrid and the APVDAQ. It bridges signals to the floating power scheme of the APV chip for clock, trigger, and analog signals. The control of the DAQ system and readout of the analog data is carried out by a PC. The data acquisition software operates with the LabWindows/CVI developed by National Instruments. This software is written in the C programming language.

There are several operation types in the data acquisition system. The measurements are mainly performed with two operation modes: hardware run and internal calibration scan run. The hardware run is a normal operation mode with an external trigger. The internal calibration scan is used for the sampling of the APV output waveform with a software trigger. From this waveform data, the peaking time and chip gain can be calculated.

In order to take data, the VME board and APV are reset first. Next, APV25 chip parameters such as shaping time and number of samples are downloaded. Then 600 events are taken by the internal random triggers to calculate pedestal and noise. After that data acquisition with the hardware run starts.

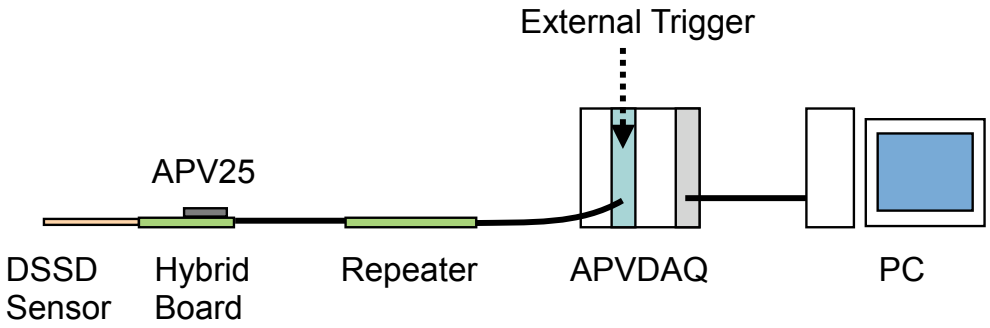


Figure 3.12: Diagram of the APV25 readout system

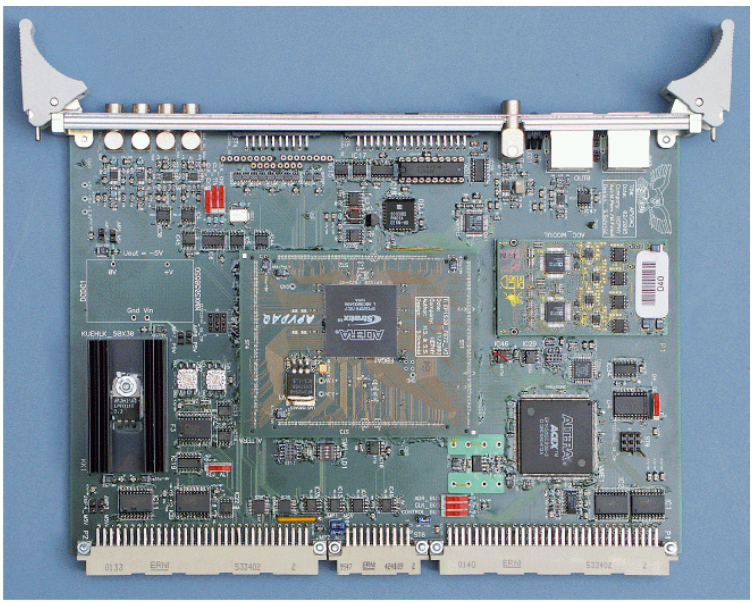


Figure 3.13: APVDAQ

Chapter 4

Radioactive Source Tests

In this chapter, we describe the VA1TA and APV25 tests performed using a radioactive source. We held these tests in order to determine occupancies with moderate radiation, utilizing the results of beam line tests (See Appendix A). With the data obtained from these tests we evaluate the occupancy reduction power of the APV25 chip.

4.1 Outline of the radioactive source tests

We held a total of 5 tests, from 10th of February 2007 till 11th of January 2008, at KEKB Tsukuba Experimental Hall in KEK.

4.2 Setup

In our radioactive source tests, we compared the occupancies of APV25 and VA1TA by counting the number of "hit events" of β-rays from the source using a random trigger. The analysis procedure is described in more detail in Section 4.3. We describe the setup for the tests below.

4.2.1 Detector layout

Figure 4.1 shows a side view of the detector layout. We held tests for VA1TA and APV25 independently. We set a ^{90}Sr radioactive source of 3.7 MBq at a height of 15 mm from the test module. The whole setup was covered with a black sheet to reduce noise.

For the test module for the VA1TA chip, we used a spare ladder (See Subsection 3.1.1) for the first layer of SVD from the actual Belle experiment. It consists of two DSSD's and two hybrid boards. For the test module for the APV25 chip, we used a test module built by the Vienna SVD Group [12]. This module also consists of two DSSD's and two hybrid boards. For both the z-side and the ϕ-side of this module chip ♯1 is connected to a single DSSD, while all other chips are connected to two DSSD's. We presume that this difference of connection will be reflected in a difference of the intrinsic noise, which we confirm later in Subsection 4.4.1.

There was one problem concerning the layout. We used different stages by mistake when placing the source, and the window sizes for the source were different (presumably 7∼10 mm for VA1TA tests and precisely 13 mm for APV25 tests). If these windows work as collimators, the radiation doses of the modules for VA1TA and for APV25 will differ slightly. We will discuss this issue later again in Subsection 4.4.2.

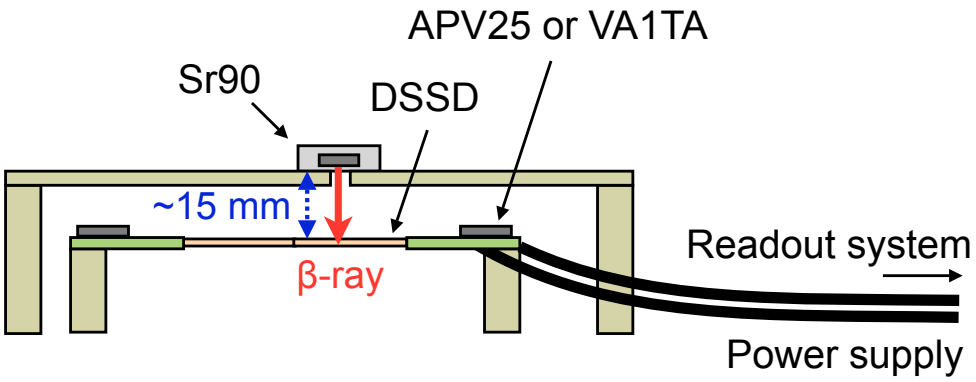


Figure 4.1: Side view of the detector layout for the radioactive source tests

4.2.2 VA1TA readout system

For the readout of VA1TA, we used the same system as the actual SVD readout described in Subsection 3.1.4. For the trigger, we used a 500 Hz random trigger. Figure 4.2 shows the VA1TA readout system for the radioactive source tests.

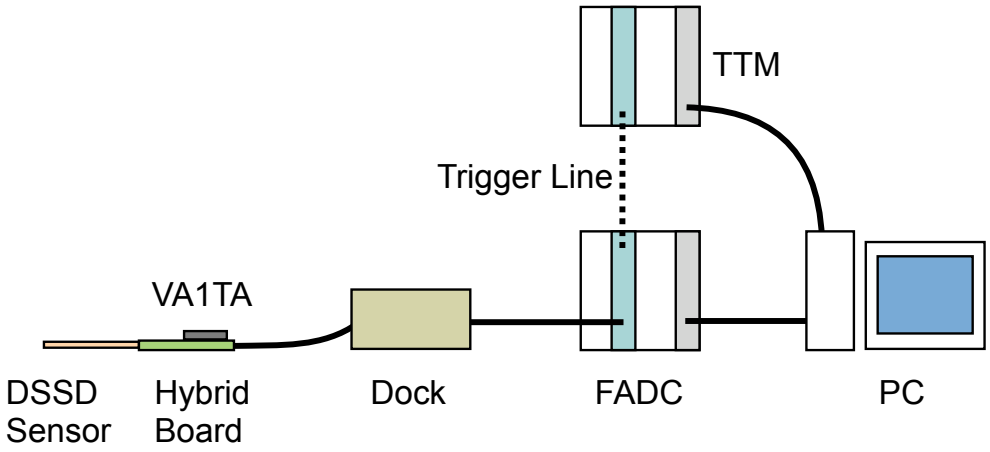


Figure 4.2: VA1TA readout system for the radioactive source tests

4.2.3 APV25 readout system

For the readout of APV25, we used the APVDAQ described in Subsection 3.2.2. We took data in 24-point multi-sample mode. For the trigger, we used a 500 Hz random trigger. Figure 4.3 shows the APV25 readout system for the radioactive source tests.

4.3 Analysis

4.3.1 Outline of analysis

In our radioactive source tests, we measured the ADC value of each channel of the test module with either VA1TA or APV25 by a random trigger. The probability that an event taken with a random trigger will yield a hit will depend on the occupancy of the chip used for the readout. We

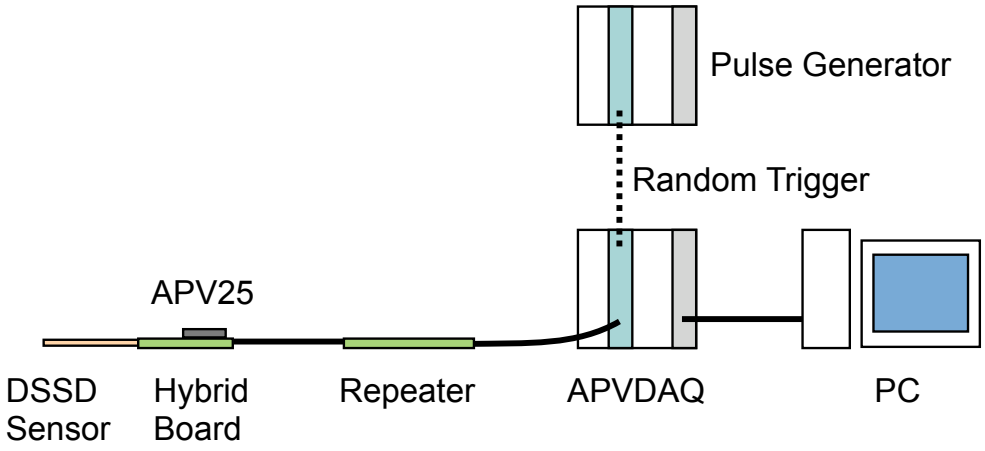


Figure 4.3: APV25 readout system for the radioactive source tests

then analyzed the ADC values, counted the number of hit events, and evaluated the occupancy. We used 400,000 events for VA1TA analysis and 125,000 events for APV25 analysis. An outline of the analysis procedure is as follows:

1. Evaluation of pedestal and noise

2. Evaluation of occupancy reduction power.

We describe details of each of the processes below. Firstly, we define the following words and values.

- **Valid channels**

  In our test modules, some channels are either dead or too noisy. Additionally, some channels are not exposed to the source. Therefore, we selected only healthy channels under typical radiation dosage in our analysis code. We define these selected channels as **valid channels**.

- **Hit channel, hit event**

  When the ADC count of one channel is higher than the threshold ADC count, we define the

channel as a **hit channel**. We set the threshold at one third of the ADC count for a minimum ionizing particle (MIP). The ADC count for a MIP was 100 for VA1TA and 70 for APV25. When one or more hit channels are detected in an event, we define the event as a **hit event**.

4.3.2 Evaluation of pedestal and noise

In all experimental runs we used the first 600 events to evaluate pedestal and noise. These events were taken with a random trigger, just the same as the events used for the main analysis.

The first 300 events are used for pedestal calculation. Pedestal is an offset ADC count obtained when there is no energy deposit. The signal yield from the sensor for each channel is obtained by subtracting this pedestal from the raw ADC count. The pedestal of each channel is first calculated by averaging the raw ADC counts over 300 events.

$$Pedestal_i = \frac{1}{300}\sum_{j=1}^{300} RawADC_i^j \tag{4.1}$$

where $RawADC_i^j$ is the raw ADC count of the i-th channel for the j-th event.

The second 300 events are used for noise calculation. Noise is defined as the RMS of the signal. There are two components of noise. The first one is intrinsic noise, which is caused by leakage current and detector capacitance. Intrinsic noise is different in each channel. The second component is external noise. External noise influences the ADC counts of the entire chip by the same amount for all channels. This noise is called as common mode shift (CMS). The CMS for each event is calculated by averaging pedestal-subtracted raw ADC counts over the valid channels:

$$CMS^j = \frac{1}{N_v}\sum_{i=1}^{N_v}(RawADC_i^j - Pedestal_i), \tag{4.2}$$

where N_v is the number of valid channels. The intrinsic noise is calculated as the RMS of the signal, after subtracting both pedestal and CMS noise, as:

$$Intrinsic\ noise_i = \sqrt{\frac{1}{300}\sum_{j=301}^{600}(RawADC_i^j - Pedestal_i - CMS^j)^2}. \tag{4.3}$$

The events after these first 600 calibration events are used for the main analysis, to measure occupancy. In this main analysis, we used:

$$ADC_i^j = RawADC_i^j - Pedestal_i - CMS^j, \tag{4.4}$$

where ADC_i^j is the calibrated readout of the i-th channel for the j-th event. From now on we will use the word "ADC" in this meaning. Intrinsic noise information is also used in the main analysis to determine the valid channels.

4.3.3 Evaluation of occupancy reduction power

In our radioactive source tests, the number of hit channels is always small (0, 1, 2) in every event, so we cannot evaluate occupancy properly according to Equation 1.1.

Therefore, as an alternative, we use the value of the "*hit event ratio*" to evaluate occupancy reduction power. We define this hit event ratio as:

$$Hit\ event\ ratio = \frac{Number\ of\ hit\ events}{Number\ of\ all\ events}, \tag{4.5}$$

where "hit event" is an event with at least one hit strip. The hit event ratio of APV25 must be suppressed compared to that of VA1TA due to its shorter peaking time. Hence, we can evaluate the occupancy reduction power of APV25 "R" as ratio of the two hit event ratios:

$$R = \frac{Hit\ event\ ratio\ of\ VA1TA}{Hit\ event\ ratio\ of\ APV25}. \tag{4.6}$$

Figure 4.4 shows how to evaluate occupancy reduction power of APV25 in our tests.

4.4 Results

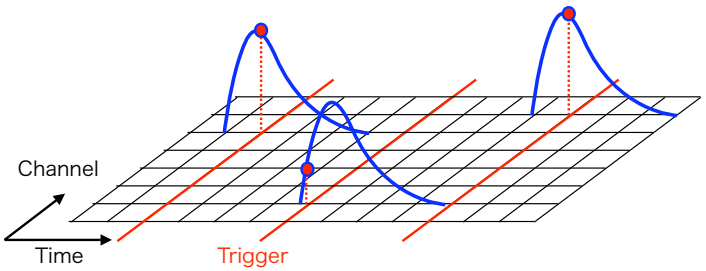
4.4.1 Evaluation of pedestal and noise

Figures 4.5 and 4.6 show the pedestal of each channel of the test module with VA1TA and APV25, respectively. The channel corresponding to the end of each readout chip (128, 256,,) has a large

VA1TA

Peaking time : 800 ns

Pulse width : 5000 ns

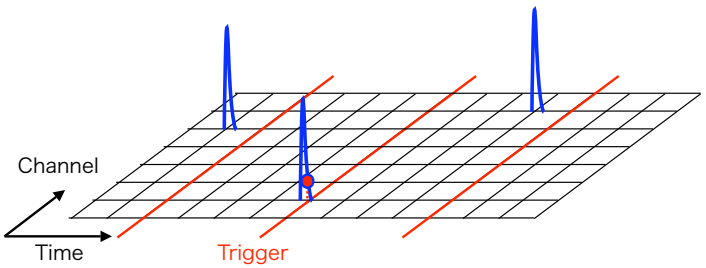


$$\textbf{Hit event ratio} = \frac{\textbf{Number of hit events}}{\textbf{Number of all events}} = \frac{\textbf{3}}{\textbf{3}}$$

APV25

Peaking time : 50 ns

Pulse width : 310 ns



$$\textbf{Hit event ratio} = \frac{\textbf{Number of hit events}}{\textbf{Number of all events}} = \frac{\textbf{1}}{\textbf{3}}$$

$$\mathbf{R} = \frac{\textbf{Hit event ratio of VA1TA}}{\textbf{Hit event ratio of APV25}} = \mathbf{3}$$

Figure 4.4: A schematic illustrating how to evaluate the occupancy reduction power "R" of APV25 in our radioactive source tests

pedestal because of a wire bonding problem between the sensor and the readout chip. The valid channels do not include these channels. In the test module with APV25, some dead channels which can be seen in Figure 4.6 were removed from the analysis.

Figure 4.5: Pedestal of each channel of the test module with VA1TA

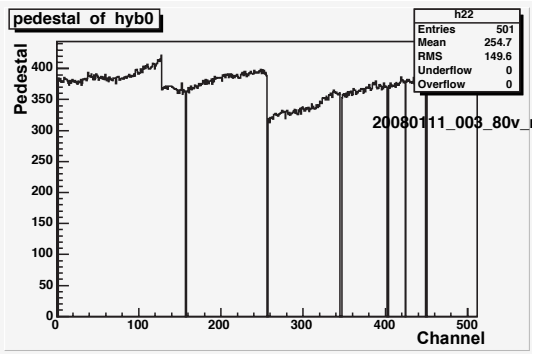


Figure 4.6: Pedestal of each channel of the test module with APV25

Figures 4.7 and 4.8 show the intrinsic noise of each channel of the test module with VA1TA and APV25, respectively. In the test module with VA1TA, intrinsic noise was higher around the area exposed to the source. In the test module with APV25, the intrinsic noise of chip ♯1 (the second chip) was lower than that of the other chips. We regard this noise difference as reasonable, because chip ♯1 is connected to only 1 DSSD, while all other chips are connected to two DSSD's (See Subsection 4.2.1). To take advantage of this low noise level in chip ♯1, we aimed the radioactive source at this location.

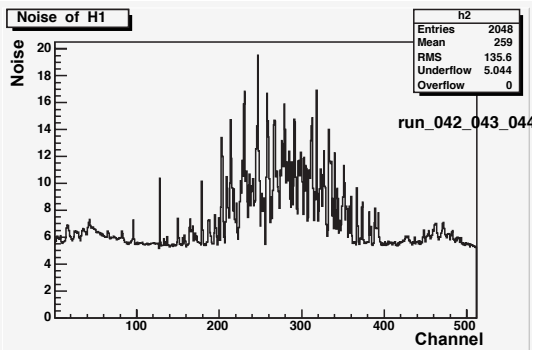


Figure 4.7: Intrinsic noise of each channel of the test module with VA1TA

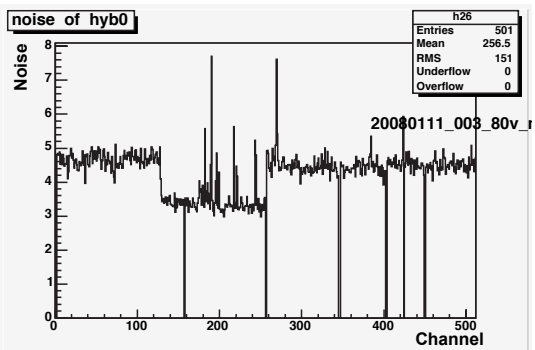


Figure 4.8: Intrinsic noise of each channel of the test module with APV25

4.4.2 Evaluation of occupancy reduction power

Figures 4.9 and 4.10 show the distribution of hit position in the test module with VA1TA and APV25, respectively. The distribution for VA1TA is narrower than APV25 because of the different window size, as described in Section 4.2.1.

Therefore, to make the condition as similar as possible in VA1TA analysis and in APV25 analysis, we chose the channels of the peak part of each distribution as the valid channels for each analysis. Specifically, we chose 50 channels from 260th till 309th (from 4th till 53rd of chip ♯2 of the z-side) for VA1TA, and also 50 channels from 180th till 229th (from 52nd till 101st of chip ♯1 of the z-side) for APV25.

After we decided the valid channels, we evaluated pedestal and noise again over these channels only.

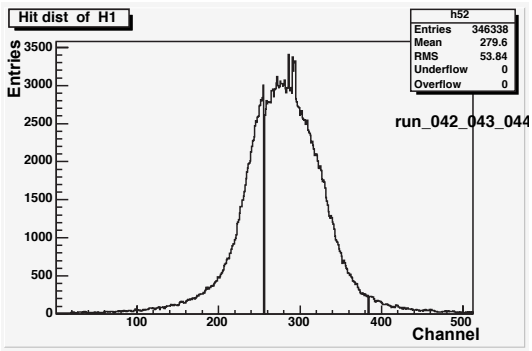


Figure 4.9: Distribution of hit position in the test module with VA1TA

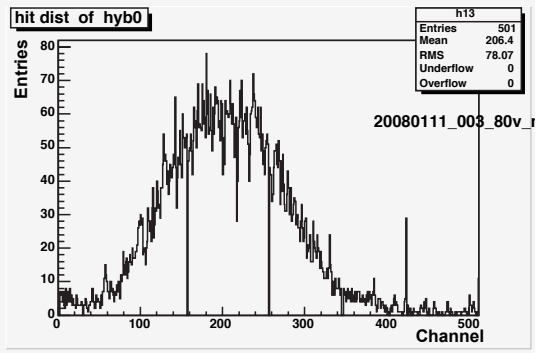


Figure 4.10: Distribution of hit position in the test module with APV25

Figures 4.11 and 4.12 show the ADC distributions of the test module with VA1TA and APV25, respectively, without the radioactive source. Figures 4.13 and 4.14 show the ADC distributions of the same modules, with the radioactive source. It can be seen that each distribution was broadened by the source. Additionally, the distribution of the test module with APV25 with the radioactive source was narrower than that of the module with VA1TA. We presume that this is because the gain of APV25 is lower than that of VA1TA as already known. It means the signal to noise ratio of APV25 is worse than that of VA1TA.

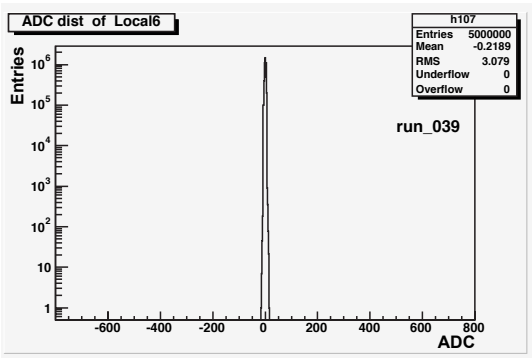


Figure 4.11: ADC distribution of the test module with VA1TA, without the radioactive source

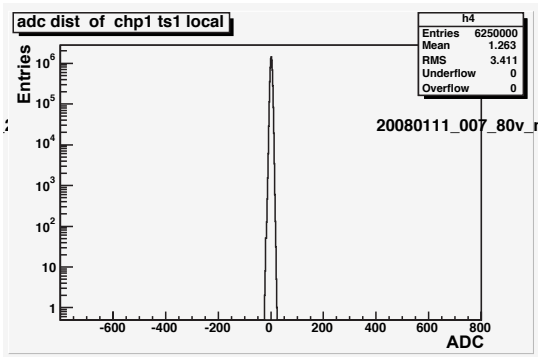


Figure 4.12: ADC distribution of the test module with APV25, without the radioactive source

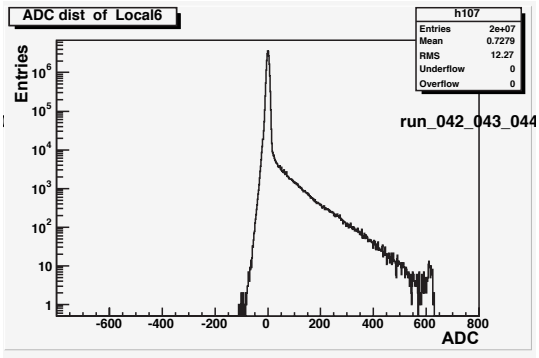


Figure 4.13: ADC distribution of the test module with VA1TA, with the radioactive source

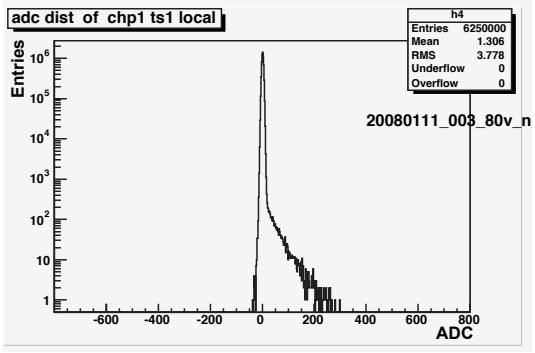


Figure 4.14: ADC distribution of the test module with APV25, with the radioactive source

Figures 4.15 and 4.16 show the distribution of the number of hit channels in the test module with VA1TA and APV25, respectively. The hit event ratio (equation 4.5) is 64,147/400,000=16.0% for VA1TA, and 1,768/125,000=1.41% for APV25. Thus, the occupancy reduction power, R (equation 4.6) is 11.4.

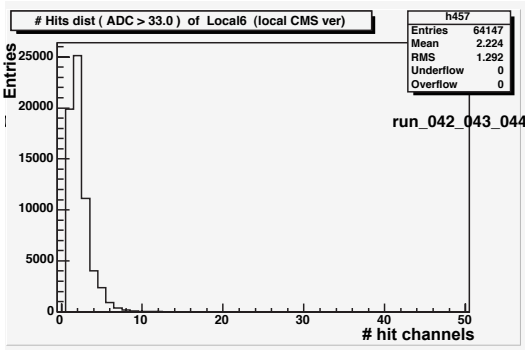


Figure 4.15: Distribution of the number of hit channels in the test module with VA1TA

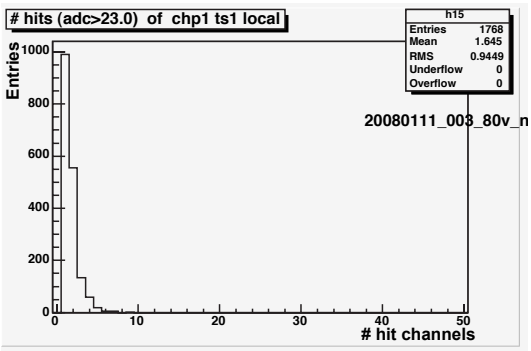


Figure 4.16: Distribution of the number of hit channels in the test module with APV25

4.5 Discussion

Here we discuss the results of the radioactive source tests.

The first topic is the difference in the window size for VA1TA and APV25. Since the window size for APV25 was larger, even in the valid channels, APV25 might have had higher radiation, and thus higher occupancy. If this is the case, the value of R quoted above will be underestimated.

The second topic is the distribution of the number of hit channels. As Figure 4.15 and Figure 4.16 show, the VA1TA results show a larger number of hit channels than the APV25 results. This means that the actual occupancy of VA1TA is higher than the occupancy reflected in R. This suggests that the R defined by Equation 4.6 is underestimated. This effect could be minimized by lowering the rate of β-ray source.

Because of these two points, the result of our evaluation is somewhat underestimated. However, it is difficult to evaluate the effect of these underestimations precisely. Therefore, we decide to use the above result for the simulation study in the following chapter.

4.6 Summary of the radioactive source tests

Based on the radioactive source tests, the APV25 has 11.4 times higher occupancy reduction power R than VA1TA. This value is used in the following simulations.

Chapter 5

Simulation

In this chapter, we estimate the performance of the SVD with the APV25 readout chip under the expected beam background at the Super Belle experiment. Specifically, we simulate the first phase of the upgrade for SuperBelle where the beam background level will be five times that of the current level. In this phase, we plan to replace the VA1TA of first and second layers of the SVD to APV25. We assume that the occupancy reduction power R is equal to 11.

5.1 Simulation Procedure

5.1.1 Estimation of the beam background effect on the SVD with VA1TA

In the Belle experiment, we estimate the effect of the beam background on analyses by embedding real beam background events taken with a random trigger on the simulated B meson decay events.

Figure 5.1 shows how to add beam background onto the simulated events for SVD with VA1TA. In practice, the VA1TA holds the pulse height at the level-0 trigger timing coming from the global trigger. Usually, the level-0 trigger timing is adjusted so that the VA1TA can capture the pulse height at the peak of the signal events. On the other hand, beam background events are generated by spent particles and synchrotron radiation which are not correlated with the signal event timing. Therefore, only the pulses which are created by beam background and coincide with the hold signal

are recorded by the VA1TA. To simulate this, we simply add the information of the pulse height of a single beam background event onto that of a simulated event. This procedure is applied channel-by-channel to data of the VA1TA. The pulse height of a certain channel, which is caused by a signal beam background event, is added onto the same channel whether or not this channel has already had a simulated signal pulse. In the case of higher beam background, multiple different beam background events are added onto a singe simulated event.

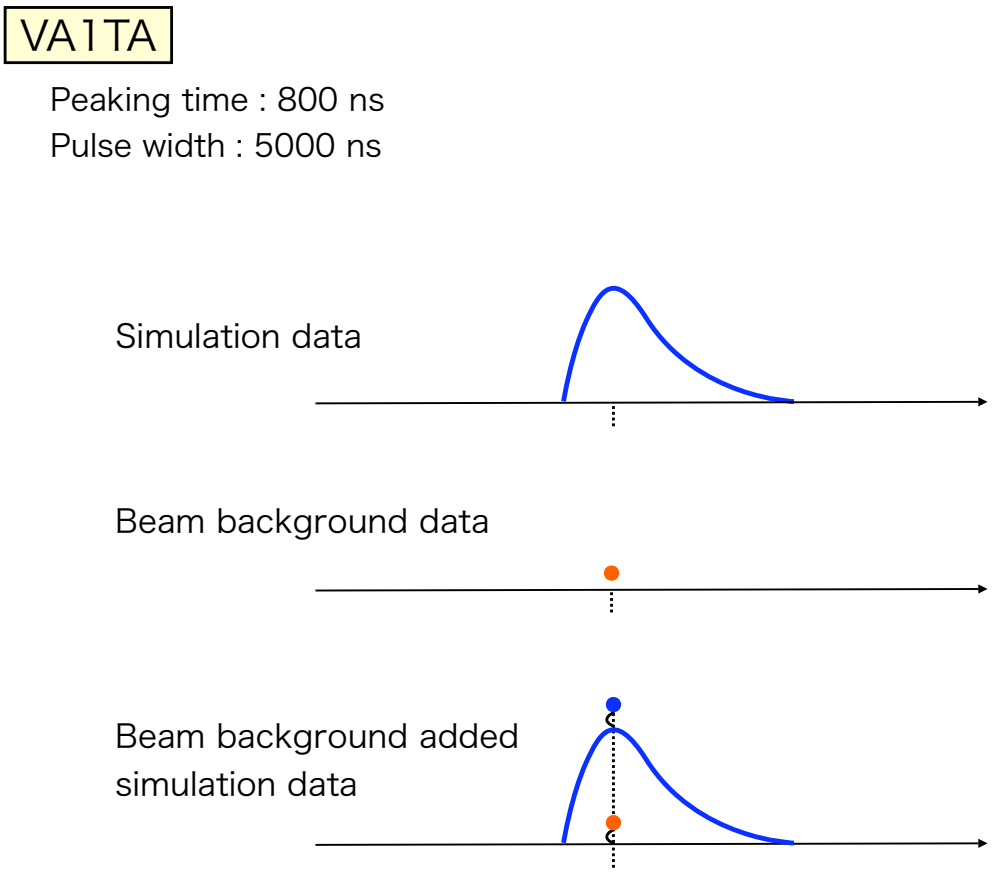


Figure 5.1: Method of adding the beam background to the simulation data of SVD with VA1TA

5.1.2 Estimation of the beam background effect on the SVD with APV25

The procedure of the simulation of the beam background on the SVD with APV25 is basically the same as that of the VA1TA case. However, there are some differences between the VA1TA and APV25 methods. First of all, as mentioned previously, VA1TA can keep the pulse height only at

the level-0 trigger timing, and the pulse shape information is lost. On the other hand, the APV25 can record the pulse height every 25 ns. Second, the peaking time of the APV25 (50 ns) is much shorter than the VA1TA (800 ns). All of the beam background events we have are taken using the current SVD with VA1TA. Therefore, we need to convert the beam background data recorded with VA1TA to that of APV25 under some assumptions explained below.

Figure 5.2 shows the schematic process of the conversion of the beam background data of the VA1TA to that of the APV25, and the procedure of embedding the converted beam background events onto the simulated event of APV25. At first we assume that the pulse width of the VA1TA is typically 5000 ns and that the rising time of the beam background pulse of the VA1TA is distributed between -4200 ns and +800 ns (relative to the level-0 trigger timing) uniformly. This is because only the pulses rising in this range can overlap with the simulated events. Secondly we make a 5000 ns-wide modeled VA1TA pulse rising at the decided timing of the beam background pulse. We then compress the pulse shape in time by a factor 1/16 while maintaining the rising time and the pulse height. Only if the compressed beam background pulse overlaps with the simulated pulse, the pulse height information in each time-slice bin is added to that of APV25.

To increase the occupancy reduction power of APV25 we have one more technique, so-called "pulse shape filter".

Firgure 5.3 shows the basic concept of the pulse shape filter. In this thesis, we use the pulse height at three points, 25ns, 50ns (peak position) and 100ns. The top figure shows the case without overlapping beam background. The selected three points form a mountain-like shape. On the other hand, in the other three cases (different types of overlapping of the beam background) these three points shows a monotonic decrease, a monotonic increase and a valley-like shape respectively. Therefore, by requiring the mountain-like shape we can select events without an overlapping beam background pulse. We believe that this requirement improves the B meson decay vertex resolution.

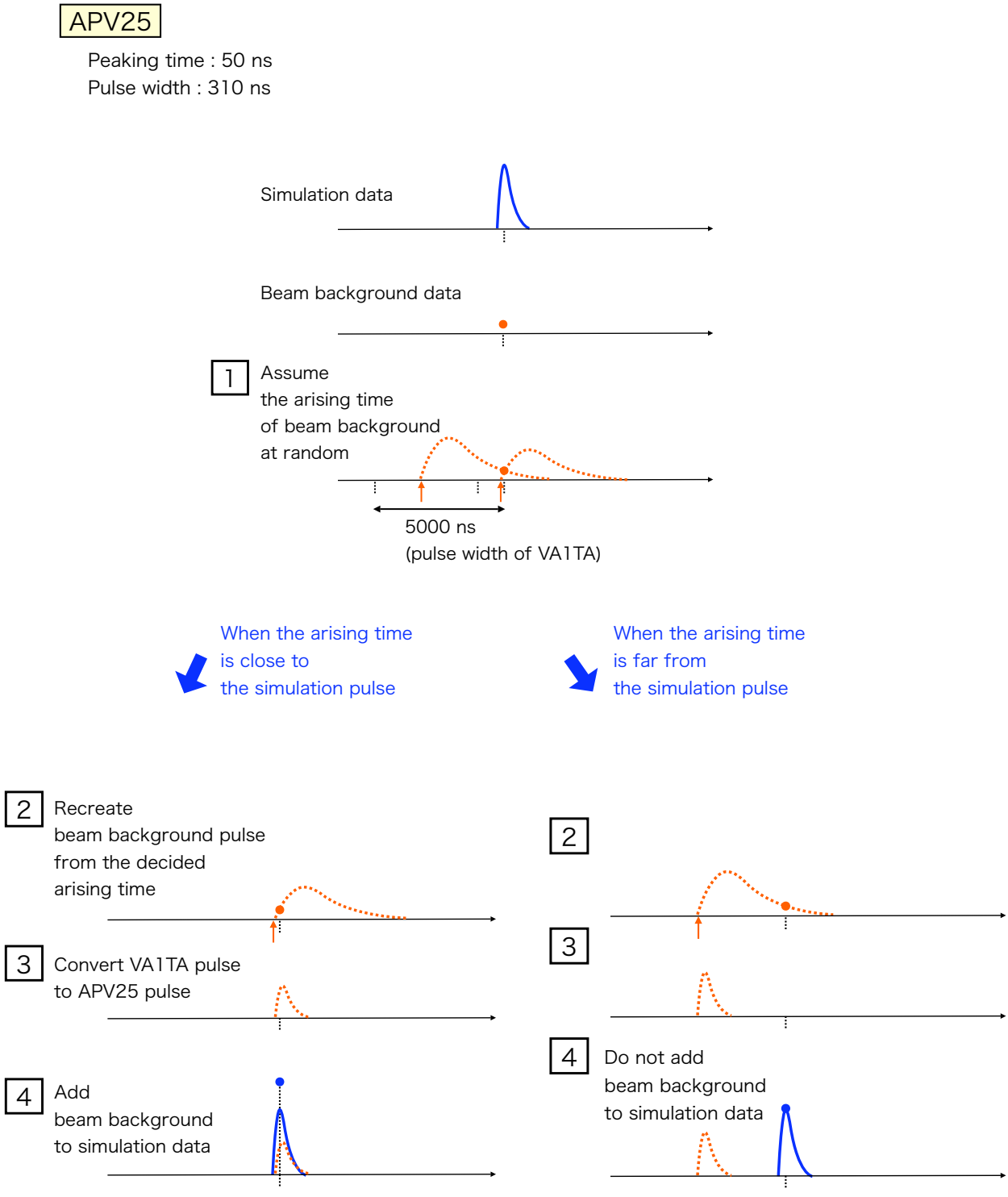


Figure 5.2: How to convert the beam background data of VA1TA to that of APV25, and add the converted beam background data onto the simulation data of APV25.

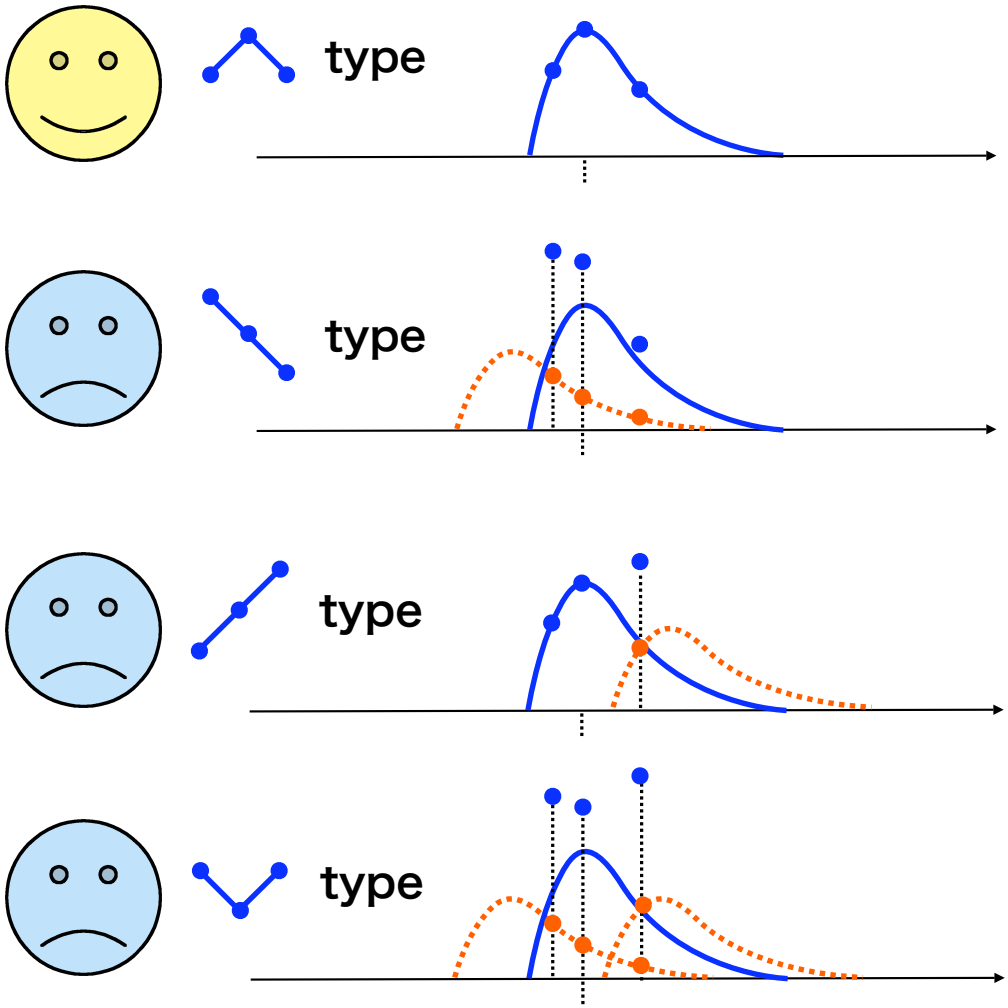


Figure 5.3: Pulse shape filtering technique for the APV25 pulse

5.1.3 Vertex resolution ($\Delta Vdif$)

Here we explain the value used to estimate the performance of the SVD with VA1TA and APV25. In the Belle experiment we measure the distance of the B^0 and $\bar{B}^0$ decay vertices to study CP violation. For simplicity, we name one of the two decay sides as "CP-side" and the other as "Tagging-side". The vertex position of each side is defined as V_{cp} and V_{tag}, respectively, and then the distance between these two vertices is defined as $Vdif$ (illustrated in Figure 5.4). Each vertex position can be reconstructed by the standard Belle tracking and vertexing algorithms. To estimate the performace of the SVD with VA1TA and APV25, we introduce $\Delta Vdif = Vdif_{rec} - Vdif_{MC}$ where $Vdif_{rec}$ is the reconstructed value of $Vdif$ and $Vdif_{MC}$ is the true value of $Vdif$.

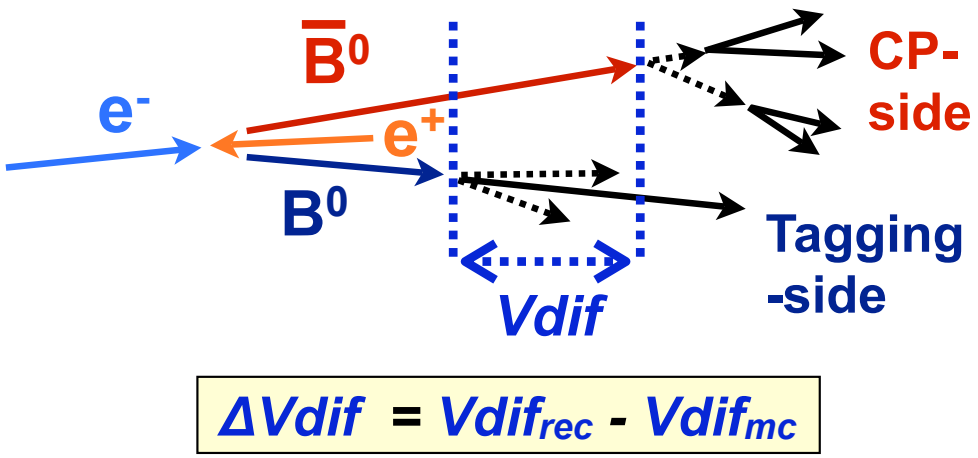


Figure 5.4: Schematic view of the measurement of $Vdif$

5.2 Results

Figures 5.5 and 5.6 show the distribution of $Vdif$ of the SVD with VA1TA, and APV25 with the pulse shape filter, respectively. They are taken under single beam background level. Figures 5.7 and 5.8 show similar distributions under five times beam background level. We confirmed that even under five times beam background level, APV25 maintains a performance of 1.0 times $\Delta Vdif$ of under the single beam background, whereas VA1TA worsens by a factor of 1.4 times.

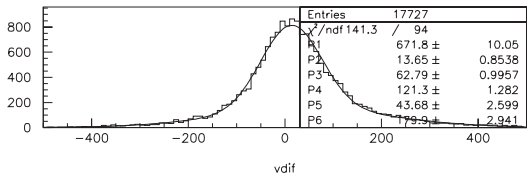


Figure 5.5: Distribution of Vdif of the SVD with VA1TA under single beam background level; fitting parameter P4 corresponds $\Delta Vdif$

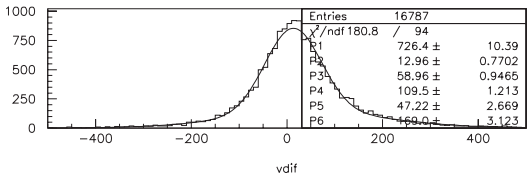


Figure 5.6: Distribution of Vdif of the SVD with APV25 with pulse shape filter under single beam background level; fitting parameter P4 corresponds $\Delta Vdif$

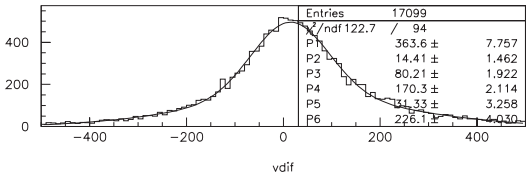


Figure 5.7: Distribution of Vdif of the SVD with VA1TA under five times beam background level; fitting parameter P4 corresponds $\Delta Vdif$

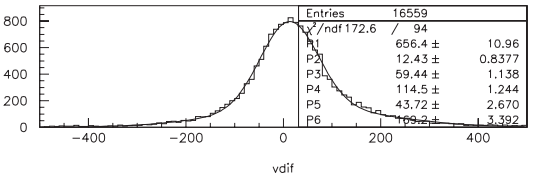


Figure 5.8: Distribution of Vdif of the SVD with APV25 with pulse shape filter under five times beam background level; fitting parameter P4 corresponds $\Delta Vdif$

Figure 5.9 shows the vertex resolution $\Delta Vdif$ as a function of the beam background level. In the first phase of the upgrade for SuperBelle, the expected beam background level at SVD is five times higher than at the current Belle experiment. The simulation results for this phase show that the average $\Delta Vdif$ with APV25 is $114.5 \pm 1.2\mu$m with the pulse shape filter, and $117.1 \pm 1.4\mu$m without the pulse shape filter. On the other hand, $\Delta Vdif$ with VA1TA reaches $170.3 \pm 2.1\mu$m. We confirm that the upgraded SVD achieves high resolution and satisfies the requirements for the first phase of upgrade.

Next, we check if APV25 can reduce the vertex resolution by shortening the peaking time to obtain higher occupancy reduction power. Figure 5.10 shows the vertex resolution ($\Delta Vdif$) as a function of the occupancy reduction power, R, under 15 times the beam background level of the current Belle experiment. The results show that the improvements in the resolution of $\Delta Vdif$ have almost plateaued at ~ 140 μm for $R \geq 6$. This resolution is 16% worse than the current VA1TA resolution (121μm).

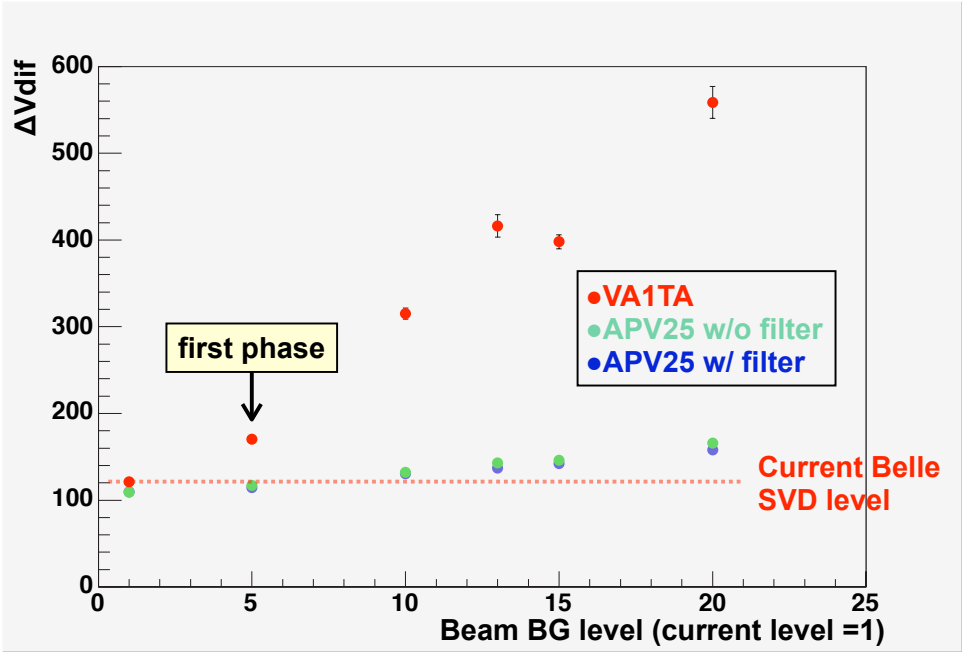


Figure 5.9: Vertex resolution $\Delta Vdif$ as a function of the beam background level relative to the current Belle background level: APV25 with the pulse shape filter (blue); APV25 without the pulse shape filter (green); VA1TA (red)

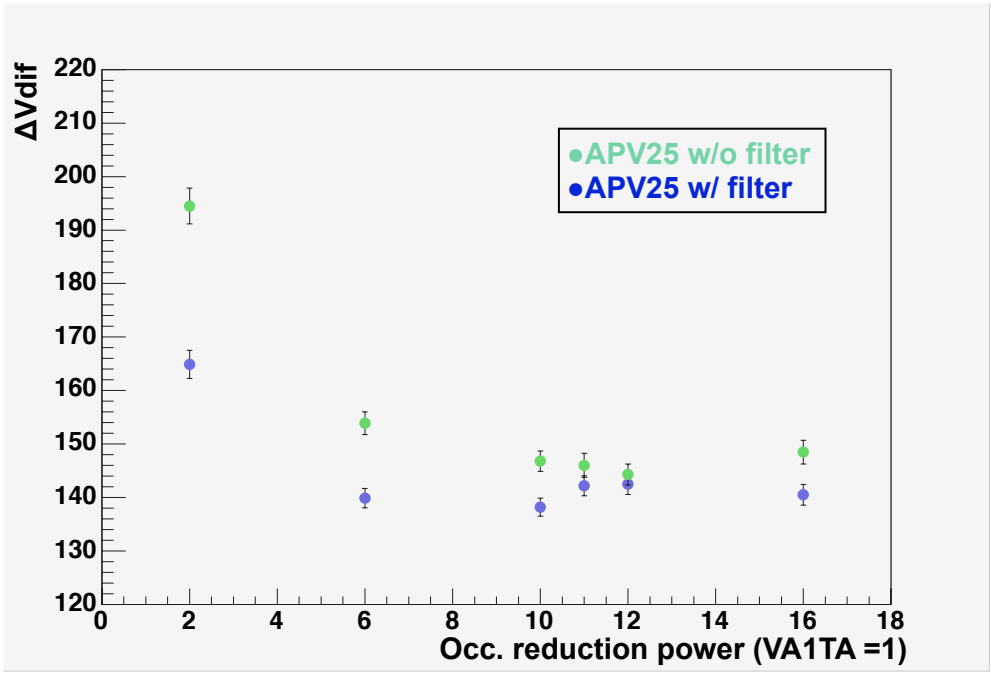


Figure 5.10: Vertex resolution ($\Delta Vdif$) as a function of the occupancy reduction power R under 15 times the beam background level of the current Belle experiment: APV25 with the pulse shape filter (blue); APV25 without the pulse shape filter (green);

5.3 Discussion

Here we discuss how we can reduce the vertex resolution of APV25 to the level of the current VA1TA.

First of all, we can make improvements to the pulse shape filter. Instead of just simply using the shape of the three points, we can use the ratio of the heights of the three points. Since the pulse shape is fixed by the circuit, the ratios should be fixed for uncontaminated events.

Additionally, other studies suggest further methods. For example, Y. Nakahama [13] suggests improvements by utilizing a "time cut". This time cut is similar to our shape filter in a sense, but performs a different filtering by using time information. This cut reconstructs the timing of the event from the recorded multiple-point-sample data, and compares the reconstructed timing with the triggered timing. They show that by the effect of the peaking time shortening and that of tight time cut, APV25 will keep similar performance to that of VA1TA in the current Belle even under the 32 times higher beam background level.

Furthermore, studies on clustering [14] and tracking softwares will also help to improve the vertex resolution.

5.4 Summary of the simulation study

We estimated the performance of SVD with APV25 with 11 times occupancy reduction power relative to VA1TA, and obtained following results.

- Under the conditions of the first phase of the upgrade for SuperBelle, APV25 achieves high resolution and satisfies the vertex resolution requirements for this phase.
- APV25 under higher (>5 times) beam background level has 13% larger vertex resolution than VA1TA under the current beam background level. It is hard to improve this resolution only

by shortening the peaking time. However, by applying the pulse shape filter and the timing cut further improvement is expected.

Chapter 6

Summary

In order to evaluate and confirm the occupancy reduction power of APV25, we have held radioactive source tests and simulation studies.

As the results of the radioactive source tests;

- We confirmed that the APV25 has 11.4 times occupancy reduction power R relative to VA1TA. We used this value in following simulation studies.

As the results of the simulation studies;

- We confirmed that under the conditions of the first phase of the upgrade for SuperBelle, APV25 achieves high resolution and satisfies the requirements for this phase.
- We also confirmed that APV25 under higher (>5 times) beam background level has 13% larger vertex resolution than VA1TA under the current beam background level. It is hard to improve the resolution only by shortening the peaking time. However, by applying the pulse shape filter and the timing cut further improvement is expected.

Appendix A

Beam Line Tests

In this appendix, we describe the VA1TA and APV25 tests performed in the actual KEKB beam line. We held these tests at first in our studies, before the radioactive source tests (See Chapter 4). We planned to compare the occupancies of VA1TA and APV25 chips and to evaluate the occupancy reduction power of the APV25 chip, with the data obtained from these tests.

A.1 Outline of the beam line tests

In order to observe high occupancies, we held these tests from 19th to 26th of October 2006, at roughly 10 m upstream from the interaction point (IP) where harsh beam background is expected.

A.2 Setup

In our beam line tests, we evaluated and compared the occupancies of VA1TA and APV25 by using synchronized random triggers. We describe the setup for the tests below.

A.2.1 Detector layout

Figure A.1 shows the installation location of the test modules. We set the modules between the two beam lines at the distance of 10 m from the interaction point. At this location, the level of fast neutron was 1.6 mSv/2weeks and the level of EM showers was assumed to 200∼500 counts/sec. Figure A.2 shows the installation of the modules.

Figure A.3 shows a schematic view of the detector layout. We held tests for VA1TA and APV25 at the same time. We set these test modules as the DSSD sensors became perpendicular to the beam lines and received much beam background.

For the test module for the VA1TA chip, we used the same module as we used in the radioactive source tests (See Subsection 4.2.1). This module consists of two DSSD 's and two hybrid boards, and almost full (512) readout channels are available for both z-side and ϕ-side. For the test module for the APV25 chip, we used a slightly different module from that we used in the radioactive source tests. The module we used this time consists of one DSSD and one hybrid board, and the total number of available readout channels was 59 for z-side. Figure A.4 shows the upside view of the modules installed between the two beam lines. The whole setup was covered with a black sheet to reduce noise.

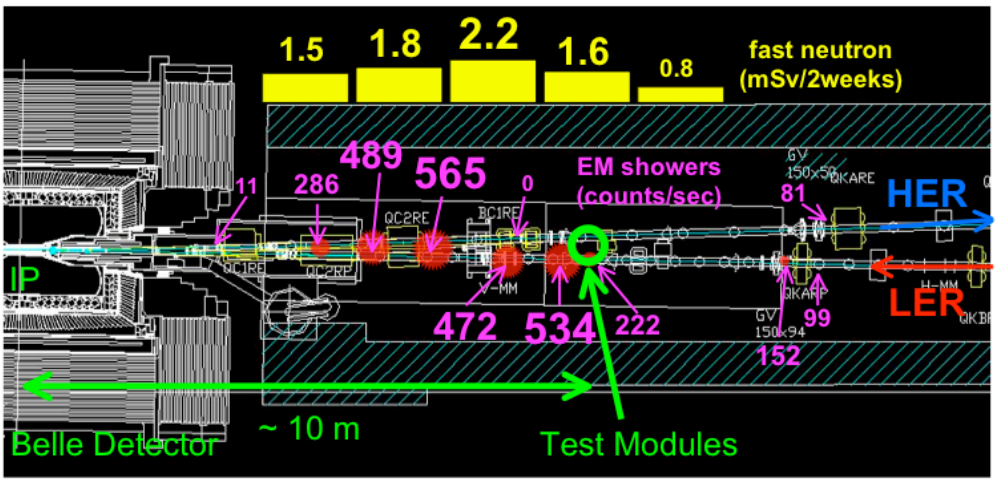


Figure A.1: Location of the test modules for the beam line tests

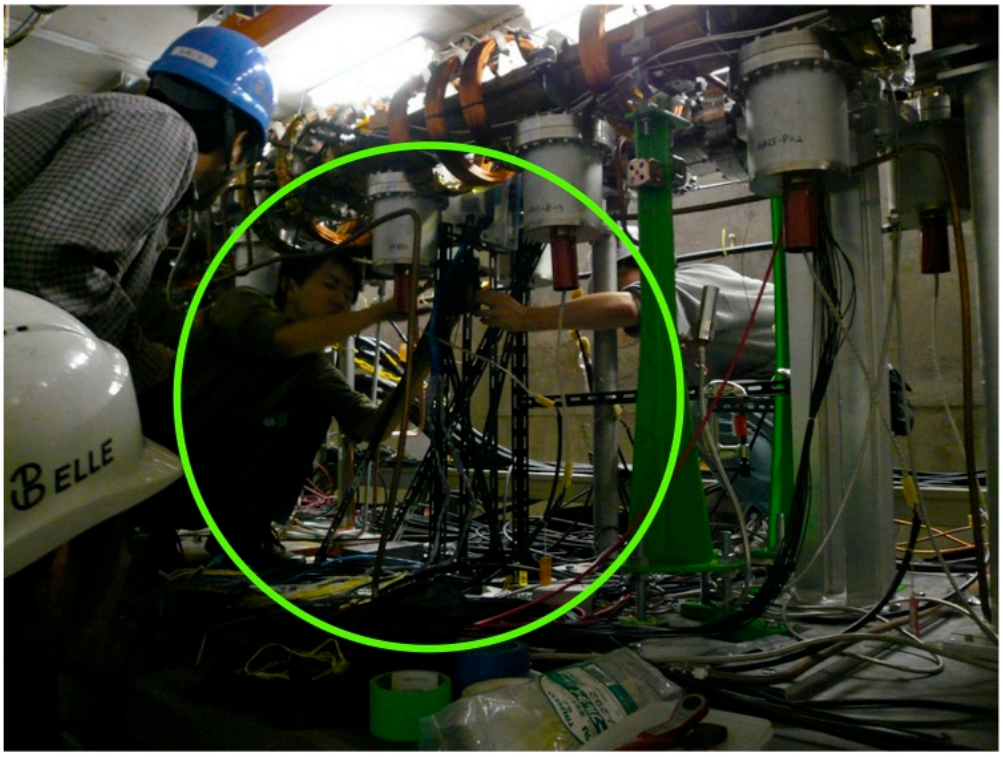


Figure A.2: Installation of the test modules for the beam line tests

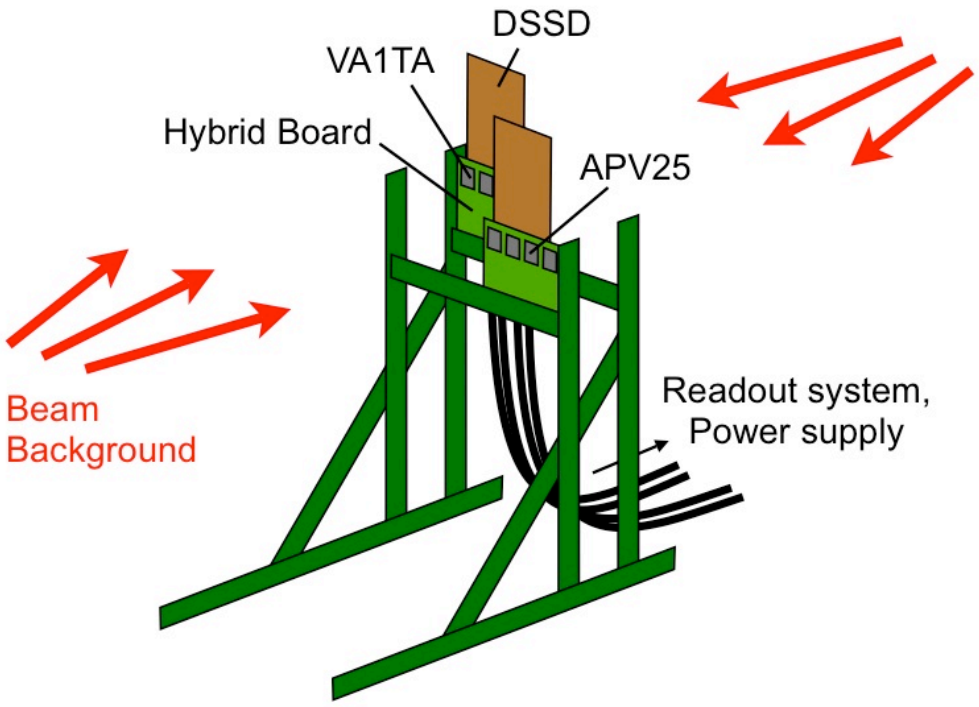


Figure A.3: Schematic view of the detector layout for the beam line tests

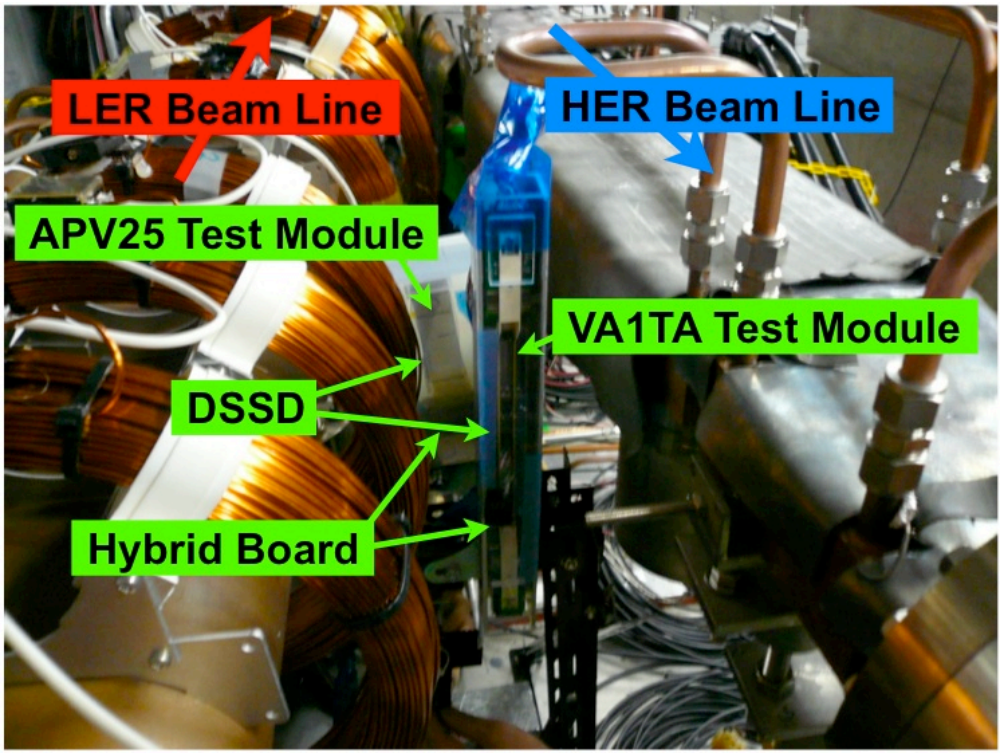


Figure A.4: Upside view of the detector layout for the beam line tests

A.2.2 Readoutsystem

We used similar readout systems as weusedintheradioactivesourcetests, except for the synchronized random triggers for both test modules. Figures A.5 and A.6 show readout systems for VA1TA and APV25 respectively.

A.3 Analysis

The basic idea of the analysis for the beam line tests was also similar to that for the radioactive source tests (See Section 4.3). The analysis procedure was as follows:

1. Evaluation of pedestal and noise

   At first we evaluated pedestal, CMS and intrinsic noise in order to calibrate ADC counts of each channel.

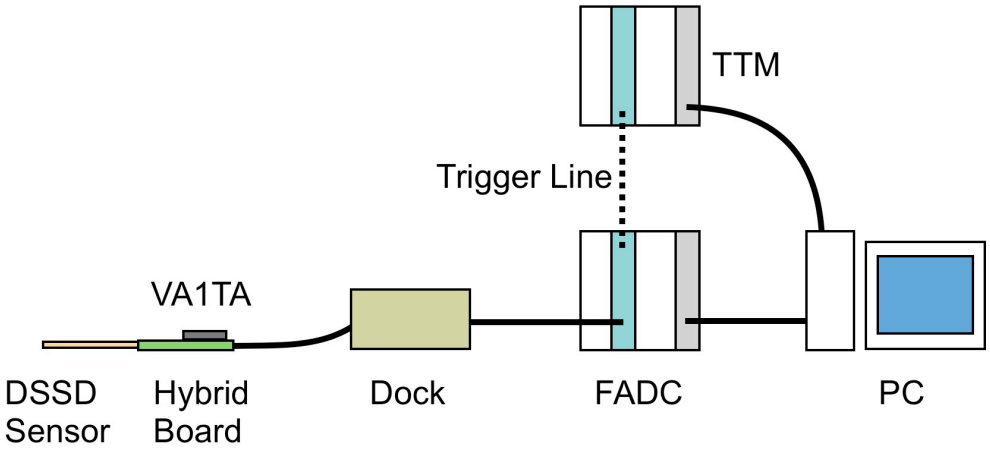


Figure A.5: VA1TA readout system for the beam line tests

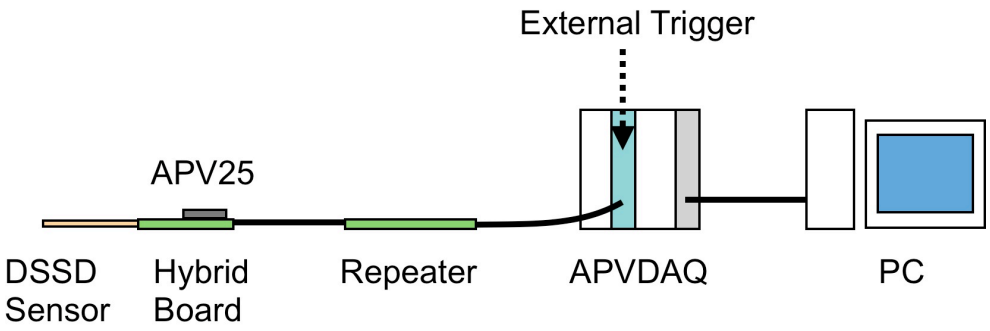


Figure A.6: APV25 readout system for the beam line tests

2. Evaluation of occupancy reduction power.

   With the calibrated ADC counts, we determined the number of hit channels and the occupancy for each event. Finally, we compared the occupancies of VA1TA and APV25 and evaluated the occupancy reduction power of APV25.

A.4 Results

A.4.1 Results of the module with VA1TA chip

For the results of the module with VA1TA chip, we could not evaluate the occupancy properly because of presumable too many beam background hits on the module, as the following results implied:

Figures A.7 and A.8 show the event dislay (the raw ADC counts of each channel) of the test module with VA1TA in one event without beam background (during KEKB 's stopping) and with beam background (during KEKB 's running), respectively. In the latter figure, many spikes were observed and the difference between hit channels and non-hit channels was not obvious.

Figures A.9 and A.10 show the CMS of the chip ♯0 of the test module with VA1TA for each event without and with beam background, respectively. The range of the CMS jumped by ten times during KEKB is running.

And Figures A.11 and A.12 show the intrinsic noise of each channel of the test module with VA1TA without and with beam background, respectively. The level of the intrinsic noise jumped by 16 times during KEKB is running.

Finally, we concluded that we could not neither calibrate the ADC counts properly nor evaluate the occupancy of the module with VA1TA chip. We confirmed this conclusion by the following results of the module with APV25 chip.

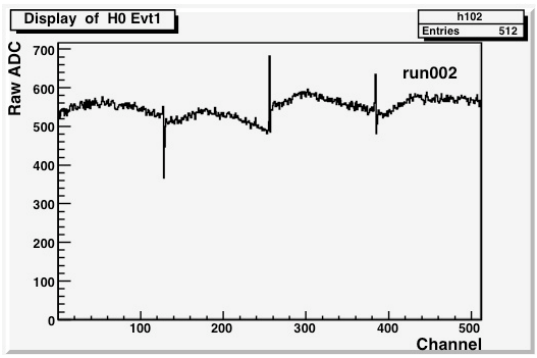


Figure A.7: Event display of the test module with VA1TA in one event without beam background

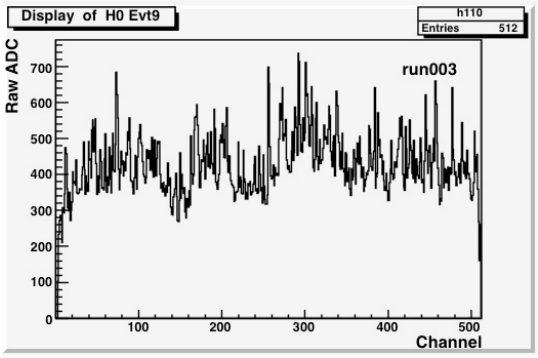


Figure A.8: Event display of the test module with VA1TA in one event with beam background

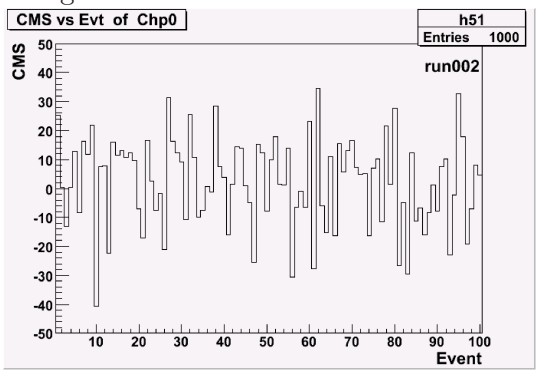


Figure A.9: CMS of the chip ♯0 of the test module with VA1TA for each event without beam background

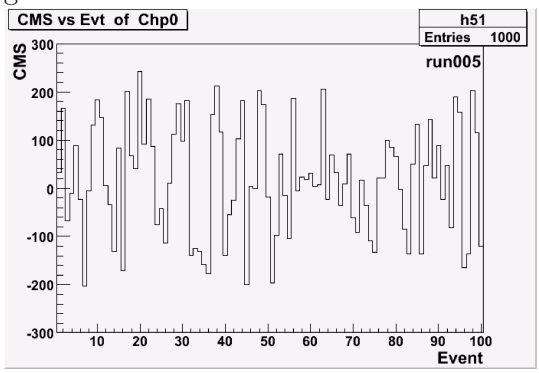


Figure A.10: CMS of the chip ♯0 of the test module with VA1TA for each event with beam background

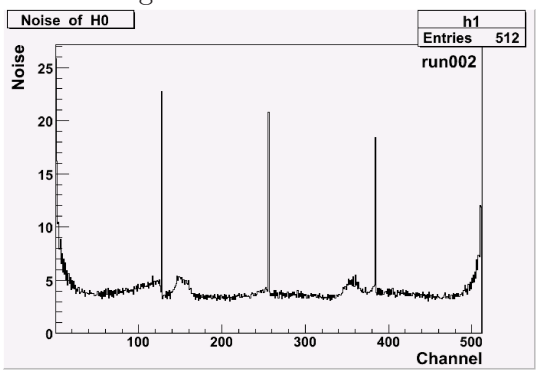


Figure A.11: Intrinsic noise of each channel of the test module with VA1TA without beam background

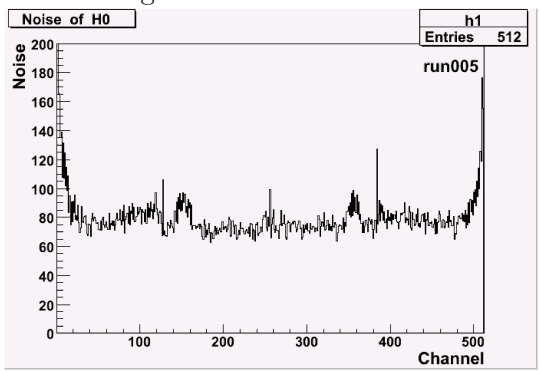


Figure A.12: Intrinsic noise of each channel of the test module with VA1TA with beam background

A.4.2 Results of the module with APV25 chip

For the results of the module with APV25 chip, the situation caused by the presumable high beam background level was not so serious as that for VA1TA. The increase of the level of the intrinsic noise caused by beam background remained at four times and we could analyze the data.

Figure A.13 shows the distribution of the occupancy of the test module with APV25 with beam background, where the threshold for hit channels was set at 25 ADC counts. The average occupancy was 17%. If we assume the occupancy reduction power of APV25 as 11 [1] (16), this result means that the average occupancy of the test module with VA1TA would be 190% (270%) and it was reasonable that we could not analyze the results of VA1TA.

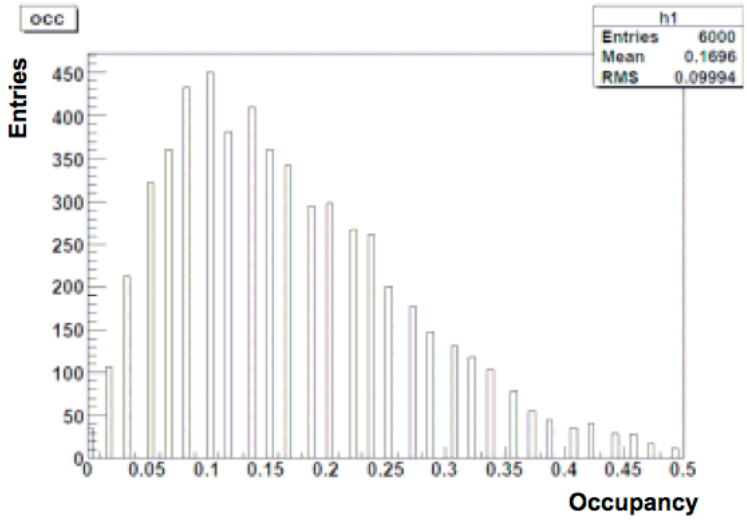


Figure A.13: Distribution of the occupancy of the test module with APV25 with beam background

A.5 Discussion

The beam background level at the location of these tests turned out to be too high for the module with VA1TA. Under this condition we suspected that the test module could malfunction by the large radiation dose. Therefore, we decided to stop these beam line tests and to use the radioactive

[1] The result of the radioactive source tests.

source.

A.6 Summary of the beam line tests

Because of the presumable too high beam background level;

- We could not evaluate the occupancy of the module with VA1TA.
- We evaluated the average occupancy of the module with APV25 as 17%.
- We planned the radioactive source tests.

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