Nuclear Instruments and Methods in Physics Research A ▮ (▮▮▮▮) ▮▮▮–▮▮▮

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

Online data processing and hit time reconstruction for silicon detector readout

C. Irmler *, M. Friedl, M. Pernicka

Institute of High Energy Physics, Nikolsdorfergasse 18, A-1050 Vienna, Austria

ARTICLE INFO

Keywords:
Belle
APV25
Silicon detector
Time measurement
Electronics
Readout system

ABSTRACT

A major upgrade of the KEKB factory (Tsukuba, Japan) is foreseen until 2013, aiming at a luminosity of up to $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, which is about 40 times the present value. Accordingly, a similar increase is expected for trigger rate and occupancy of the Silicon Vertex Detector (SVD). The current readout system has a shaping time of 800 ns, no multi-event memory and thus requires a trigger within this period. As it already operates at its limit, it obviously has to be replaced for the upgrade.

We developed a readout system using the APV25 chip with a shaping time of 50 ns and an integrated analog pipeline. By taking six consecutive samples of the shaper output and processing these data with FPGAs on a VME module we can determine timing information of the hits with a precision of about 3 ns RMS, which enables occupancy reduction and thus eases subsequent track finding. Thanks to reading several samples the system can tolerate a trigger jitter of up to ± 2 clocks.

A dedicated pipelined data processor is implemented for each input, which encodes position, pulse height and time information of a hit in a single 32 bit word. The acceptable trigger rate is limited by the time needed to read out six samples from the APV25.

1. Introduction

The Belle experiment [1] is located at the interaction point of the KEK B-factory in Tsukuba, Japan. Since its inauguration in 1999 the luminosity of the KEKB machine was continuously increased and reached a new word record of $1.96 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in May 2009. Up to this point, a total integrated luminosity of $925\,\mathrm{fb}^{-1}$ has been recorded by Belle and its operation will be continued until early 2010. Thereafter a major upgrade of the accelerator and the Belle detector (Belle II) is foreseen until 2013, aiming at a luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

The current Silicon Vertex Detector (SVD2) is read out by the VA1TA chip [2] with a peaking time of 800 ns and no multi-event buffer. It already operates at its limit in terms of occupancy and trigger rate and thus cannot meet the requirements of the upgrade, where both figures are expected to scale with the luminosity.

2. Readout chain

We built a prototype readout electronics system using the APV25 [3] amplifier, which was originally developed for the CMS Silicon Tracker at CERN. It is operated at 40 MHz, has a shaping time of nominally 50 ns and a 192 cells deep analog pipeline. The readout chain is composed of APV25 hybrids, so-called DOCK boxes located close to the front-end and the VME back-end electronics. Each DOCK box is equipped with one mother and up to six repeater daughter boards. They are used for signal level translation, signal refreshing and buffering, power monitoring and over voltage protection. The back-end consists of 9U VME crates with a single controller, providing trigger, clock and slow control signals, and several FADC+Processor boards which digitize and process the APV signals before they are forwarded to the data acquisition system.

3. Online data processing

Data processing is performed on the FADC+Processor module (Fig. 1), a 9U VME board with 16 input channels. It is equipped with four ADC daughter boards, each used to digitize the APV signals of four input channels with a 10 bit ADC. The core function is implemented in FPGAs, of which the four chips located in the front part of the board are used to process the data of four inputs, each. The fifth one in the center collects the data of the front chips, buffers them and builds the final output data frame, which is then forwarded to the data acquisition (DAQ). A simplified block diagram of the data processing chain is shown in Fig. 2. In the first stage the strip data are extracted from the digitized APV25 signals

* Corresponding author. Tel.: +43 1 544 7328 58; fax: +43 1 544 7328 54.
E-mail address: irmler@hephy.oeaw.ac.at (C. Irmler).

0168-9002/$ - see front matter © 2009 Elsevier B.V. All rights reserved.
doi:10.1016/j.nima.2009.10.023

and reordered. Then a two-pass pedestal subtraction and common mode correction is performed, followed by a hit finder for zero suppression. A dedicated pedestal and threshold memory is foreseen at each of these stages, allowing the definition of individual cuts. These first stages of the processing chain are implemented for each input, in order to ensure parallel and continuous processing.

The subsequent hit time finder is used to determine the timing of a hit. Therefore, the APV25 is operated in the so-called *multi-peak mode*, which allows to read out six consecutive samples of the shaper output. Three points around the peak are used to obtain hit timing and amplitude with lookup tables, built from the calibration pulse of the APV25 [4]. Thanks to using only three out of six samples, a trigger jitter of up to ± 2 clocks can be tolerated. Finally, position, timing, quality of time and pulse height are encoded in a single 32 bit word for each hit. In case of distorted pulse shape (e.g. pileups), where timing cannot be determined, all six samples are transmitted to the DAQ in order to avoid data loss. The knowledge of the correct timing allows to identify and suppress the vast majority of off-time background hits, leading to a occupancy reduction of up to a factor of 8. This can either be done online in case of a trigger with negligible jitter or otherwise in the offline data analysis, where the timing can be used in the track finder to match hits across several layers of the detector.

Thanks to the pipelined design with several FIFOs and two 64 bit wide local buses between front and central FPGAs, data can be processed continuously as long as they are fetched by the downstream DAQ system without congestion. Thus the acceptable trigger rate at a clock frequency of 42 MHz is about 50 kHz, limited by the time needed to read out the samples from the APV25 chips.

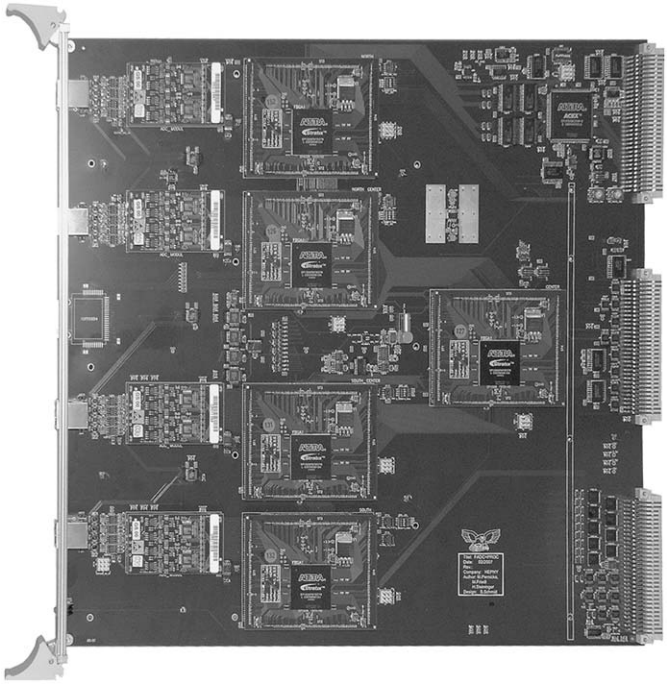

Fig. 1. FADC+Processor 9U VME module. From left to right, there are four ADC daughter boards to amplify and digitize the APV signals, the front FPGA boards for data processing and time finding and finally the central FPGA, where the event data frame is built.

4. Beam test measurements

The readout system was operated with various front-end prototype modules in several beam tests at KEK and CERN, where it has shown excellent performance. As the hit time finder was not yet implemented in the FPGA firmware at the time of the beam tests, a numerical offline fit was used instead. As a time reference the distance between the incoming trigger and the next clock edge was measured by a TDC, which is implemented on the controller board. The achieved precision of the determined peaking time is about 2–5 ns RMS, depending on the signal-to-noise ratio (Fig. 3).

5. Summary

We introduced a readout system for silicon strip detectors that uses the APV25 front-end chip and provides online data proces-

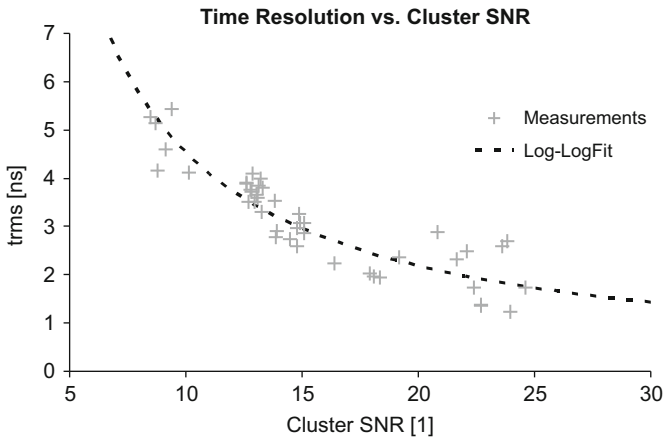

Fig. 3. Residuals of the hit timing vs. cluster signal-to-noise ratio. The measured points can be fit by a straight line in a double-logarithmic mode.

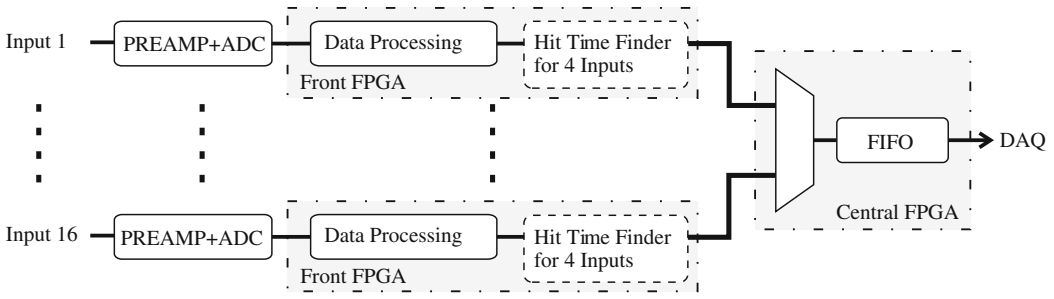

Fig. 2. Simplified block diagram of the data processing chain. While preamplifier, ADC and data processing (strip reordering, pedestal subtraction, common mode correction, zero suppression) are implemented individually for each input, there is a common hit time finder for groups of four inputs.

Please cite this article as: C. Irmler, et al., Nucl. Instr. and Meth. A (2009), doi:10.1016/j.nima.2009.10.023

sing. Due to its pipelined design trigger rates up to 50 kHz can be accepted at a system clock of 42 MHz. It further allows to obtain hit timing with a precision of 2–5 ns, which was verified by several beam tests. This information can be used to identify and suppress off-time background, which can reduce the data volume by up to a factor of 8.

References

[1] H. Aihara, et al., Nucl. Instr. and Meth. A 568 (2006) 269.
[2] VA1TA Chip ⟨http://www.ideas.no/products/ASICs/pdf/Va1Ta.pdf⟩.
[3] M. French, et al., Nucl. Instr. and Meth. A 466 (2001) 359.
[4] M. Friedl, et al., Nucl. Instr. and Meth. A 572 (2007) 385.

Please cite this article as: C. Irmler, et al., Nucl. Instr. and Meth. A (2009), doi:10.1016/j.nima.2009.10.023