Study of semiconductor detector for upgrade of Silicon Vertex Detector in Belle

Department of Physics, Graduate School of Science and Engineering
Tokyo Institute of Technology
Shun Ono

February 15, 2006

Abstract

The main purpose of the Belle experiment is to measure CP violation parameters in the decay of neutral B mesons. Since a precise determination of the distance of the decay vertex position the of B meson is required for this purpose, a Silicon Vertex Detector (SVD) is used in the Belle detector. The SVD consisting of Double-sided Silicon Strip Detectors is able to measure the position with an accuracy of 100μm or better.

A further performance improvement of the KEKB accelerator is anticipated within a few years. Therefore we expect that the beam background level increases by a factor of several. In order to cope with the higher background level, we have a plan to upgrade the SVD by replacing the readout chips of the inner layers from VA1TA to APV25 which has a faster shaper. The current DSSD was designed to be minimized the radiation damage, only P-side is read by floating strip connection. However, because of the change of the readout chips, the noise from the detector capacitance becomes dominant compared with the shot noise. So we need to develop a new designed DSSD to be optimized for the APV25 readout. More concretely, the readout directions of N and P-side is flipped and both sides use the floating strip scheme. Therefore, there are many changing points for N-side. In this thesis, we evaluate the performance of N-side single-sided strip detector (SSD) for the development of a new designed DSSD.

First, I evaluate the detector noise for three different types of a N-side SSD with APV25 readout. I find that the detector noise is less than 1000 ENC(Equivalent Noise Charge) for the three types. Then, I perform a laser scan on the sensor to see the charge sharing and estimate the position resolution. The charge sharing between two strips is clearly seen. The position resolution is estimated to be about 10μm. Finally, the performance of the SSD is evaluated with a charged pion beam. The charge collection efficiency at the floating strip is more than 80%.

Finally, we could obtain the sensor parameters that can be used for new DSSD with low noise. And then a prototype DSSD for the SVD upgrade will be developed based on this result.

Contents

List of Figures

Chapter 1

introduction

To search for the origin of CP violation between matter and antimatter, an international experiment called Belle is conducted at the High Energy Accelerator Laboratory Organization (KEK) in Tsukuba city Japan. In this experiment, CP violation is detected with huge amount of B mesons. In 2001, CP violation in neutral B meson systems was first observed at the KEKB e^+e^- asymmetric-energy (3.5 or 8GeV) collider operating at Υ (4S) resonance using B meson decays into $J/\psi K_S$. We expect that further investigation of the CP violation mechanism in Kobayashi-Maskawa theory will continue with successful data taking.

Since the branching fractions of B meson decays needed for the CP violation study is small ($\leq 10^{-4}$), it is very important to generate a large number of B mesons in this experiment. The collision rate of the beam (Luminosity) has been improved year by year. In December 2005, the peak luminosity reached to $1.6 \times 10^{34} cm^{-2} s^{-1}$. This is the highest world record of luminosity for electron-positron colliders. A further increase in the beam luminosity is in progress. Although we have much more B meson data, we also have increasing beam backgrounds.

The Silicon Vertex Detector (SVD) is a detector for determining the decay positions of B mesons. It is placed at the innermost position of the Belle detector. Therefore, the SVD is exposed by much beam backgrounds ($\sim$1krad/day). What we concern is the degradation of the position resolution due to much background accidental hits. Hence the upgrade of the SVD is planed to suppress the background hits. The readout circuit of the SVD will be replaced to APV25 having much faster shaper. Since we will use a much faster shaper for the readout, the detector capacitance become the dominant component of the noise instead of the shot noise caused by the leakage current, which is the dominant component of the current readout chip. Therefore we need to modify the DSSD design by optimizing the signal-to-noise ratio with APV25 readout.

The purpose of this thesis is to develop a new DSSD for this SVD upgrade. I will describe the outline of the Belle experiment in Chapter 2, the detail of the SVD upgrade in Chapter 3, the performance of the sensor used by research in Chapter 4. Then I will describe the result of the sensor scanning that use a semiconductor laser in Chapter 5, the data analysis of the beam test that was carried out at KEK/PS $\pi 2$ beam line in Chapter 6. Finally, I describe the conclusion of this research in Chapter 7.

Chapter 2

Belle experiment

In this chapter, details of CP violation and Belle experiment are described.

2.1 CP violation

According to the present astrophysics, it is supposed that this universe was formed with the Big-bang and the same number of particles and antiparticles were generated at that time. However, antiparticles hardly exist in the present universe. The hint to solve this mystery is CP violation. Here C means electric charge and P indicates parity. CP symmetry is the symmetry between a particle and an antiparticle.

The most promising model to explain CP violation is Kobayashi-Maskawa theory. According to this theory, if six kinds of quarks exist, CP violation can be derived through the mixture between quarks within the Standard-model framework of modern particle physics.

2.2   Belle experiment

The Belle experiment is an experiment to measure CP violation parameters with a good accuracy, and is performed at High Energy Accelerator Research Organization (KEK). The main purpose of Belle experiment is to observe CP violation in B meson decays. These B mesons are generated at the KEKB e^+e^- asymmetric-energy collider. Since the probability of a B meson decay to a CP eigenstate is extremely low with $10^{-4} \sim 10^{-5}$, a large number of B mesons are required for this study.

In the Belle experiment, CP violation is measured as the asymmetry of the distribution of the proper time difference between B^0 and $\bar{B}^0$ decays. This time difference is too short ($\sim$1ps), and it is very difficult to measure it directly. In the Belle experiment, the energy asymmetry of the electron and positron beams enables us to measure the time difference. Thanks to the energy asymmetric collider, the produced B mesons are boosted by a Lorentz factor of $\beta\gamma = 0.425$. Therefore we can measure the time differences ($\sim$1.5ps) by determining the decay position difference of $\sim 200\mu$m (Figure2.1).

Figure 2.1: Decay diagram of B mesons

2.3 KEKB accelerator

The collider used for the B meson production is called KEKB (Figure2.2), this is an electron positron collider with a circumference of about 3km.

Figure 2.2: KEKB accelerator

The features of the KEKB accelerator are as follows:

1. an asymmetric energy collider

2. the high luminosity

The energy of electron and positron beams are 8GeV and 3.5GeV, respectively. Since the probability of a B meson decaying to a CP eigenstate is very low, the high luminosity is required. The peak luminosity is 1.6×10^{34}cm^{-2}s^{-1}, which is the world record. Figure2.3 shows the luminosity history of the KEKB compared with the PEP-II at the BaBar experiment, which is our rival experiment at SLAC, USA .

Figure 2.3: Luminosity comparison between KEKB and PEP-II

2.4 Belle detector

The Belle detector consists of several detectors to detect various particles coming from the collision point (Figure2.4). It has a cylindrical shape surrounding the beam pipe. In the Belle experiment, the coordinates in the vicinity of the collision point are defined in cylindrical coordinates: z-axis is defined as a direction anti-parallel to the position beam and r-ϕ plain is vertical to the z-axis.
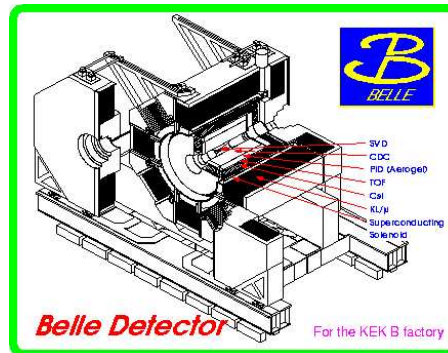
Figure 2.4: Belle detector

The detectors are described belows:

Silicon Vertex Detector (SVD)

The SVD is a position sensitive semiconductor detector which is located at the most inner position in the Belle detector. To detect CP violation of B mesons, we need to measure the decay position differences between two B mesons. Because an average decay length of a B meson is about 200μm, position resolution less than 100μm is required for the SVD. The

8

SVD was upgraded in 2003, and the position resolution has been improved by 20%. A detail of the SVD will be described in Chapter3.

Central Drift Chamber (CDC)

The CDC detects the charged particles, with position resolution of a few millimeters for the z direction and about 130μm for the r-ϕ direction. The trajectories of charged particles detected in the CDC are extrapolated to the SVD, and initiating the SVD tracking. The energy loss in the CDC is obtained by measuring the electric charges, which is useful for an identification of a particle type. The position information in the z and r-ϕ directions measured by the CDC is used for a trigger signal.

Aerogel Cherenkov Counter (ACC)

The ACC is a Cherenkov detector for an identification of π and K mesons. The momentum range of the particle identified is between 1.2GeV/c and 3.5GeV/c. The Silica-aerogel which has a reflactive index between 1.01 and 1.03 is used.

Time Of Flight detector (TOF)

The TOF is composed of 128 plastic scintillators and 256 photomultipliers placed at the both ends of the scintillators. The TOF measures the Time of Flight of a charged particle. Combined with the momentom measurements in the CDC, the TOF can measure the mass of the particle, hence identifies the particle type. The signal from TOF is used for the trigger generation.

Electromagnetic Calorimeter (ECL)

The ECL consists of CsI(Tl) scintillators. The ECL detects electrons and photons. The signal from CsI is also utilized for the trigger generation.

KL/μ detector (KLM)

The KLM is able to detect muons and neutral K_L mesons. The KLM is placed at the most outside of the Belle detector and consists of high resistance plate chambers and iron plates. Hadron shower occures if K_L mesons interacts with the KLM. The muons are identified as a particle which goes through all the iron layers. The signal from KLM is also used for the trigger generation.

Chapter 3

The Silicon Vertex Detector (SVD)

3.1 Construction of the current SVD

Because the SVD is located at the nearest position to the beam pipe, the radiation level of the SVD is very high. The SVD upgrade have been performed three times until now. The SVD operating at present is called the SVD2 and it was installed in the summer of 2003 (Figure3.1).
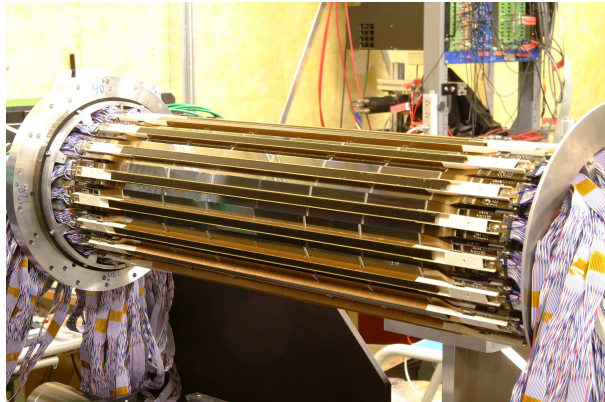
Figure 3.1: SVD2 outside

Since B mesons decay inside the beam pipe, they cannot be detected directly. In the SVD, the detector ladder (Figure3.2) is arranged by four layers around the beam pipe, and we can reconstruct the B meson vertex position by detecting the trajectories of charged particles of B meson decay products. Figure3.3 and Figure3.4 shows $r - \phi$ and z views of the SVD2.

Figure 3.2: Ladder structure

Figure 3.3: SVD2,$r - \phi$ direction diagram

Figure 3.4: SVD2,z direction diagram

3.2 Double-sided Silicon Strip Detector (DSSD)

A Double-sided Silicon Strip Detector (DSSD) is a semiconductor detector used by the SVD. The DSSD fabricated by Hamamatsu Photonics has 300μm thickness. It comprises of 512 N^+ strips in one side (N-side) and 1024 P^+ strip in the other side (P-side), which are mutually perpendicular (Figure3.5). Because the silicon bulk is made from N type semiconductor, the P-stops is implanted around the $N^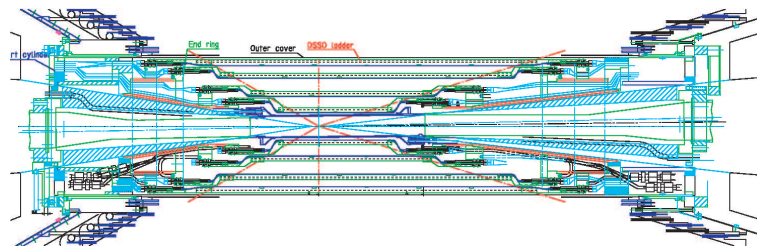+$ strips to insulate neighboring strips electrically. In the SVD2, z direction is read by P-side and $r - \phi$ direction is read by N-side.
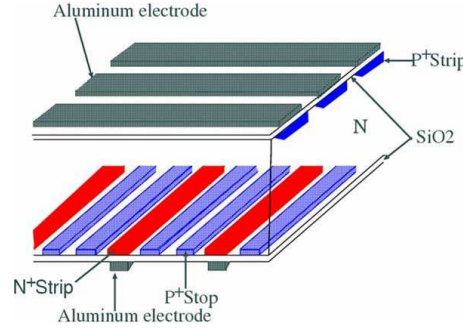

Figure 3.5: DSSD structure

At the operation, the bias voltage (N-side +40V: P-side -40V) is applied to the DSSD for the complete depletion. If a charged particle goes through the DSSD, the particle deposits its energy in the sensor, and electron-hole pairs are created. The electrons and holes are collected by the N^+ and P^+ strips respectively, and they are observed as electric signals. Therefore, we can obtain two dimensional position of the particle with the mutually-perpendicular strips. If the charged particle enters the DSSD vertically, the signal found by the N and P side are given by one strip. But if it penetrates with a large incident angle, the signal are distributed with the sequential strips. In this case, the position is calculated by a center of gravity method. Table3.1 shows specification of the DSSD used by the SVD2. Because of the sensor size, the number of strips in the P-side is twice that in N-side. In the P-side, every other strips are connected to the readout circuit (floating strip connection).

	Layer1-3		Layer4	
	P-side	N-side	P-side	N-side
Chip size [mm]	$79.6 \times 28.4 \times 0.3$		$76.4 \times 34.9 \times 0.3$	
Active area [mm]	76.8×25.6		73.8×33.3	
Strip pitch [μm]	75	50	73	65
Number of strips	1024	512	1024	512
Readout pitch [μm]	150	50	146	65
Strip width [μm]	50	10	55	12
Readout electrode width [μm]	56	10	61	10

Table 3.1: DSSD specification

3.3 VA1TA

In the SVD2, a LSI chip called VA1TA is used for reading signals from the DSSD. The VA1TA consists of VA in the analog amplifier part and TA in the trigger part, and it has 128 input channels.

If a charged particle penetrates the DSSD and the electric charge is generated on the strips, the charge is converted into the voltage with a preamplifier and then integrated by a shaper. Then, the signals are read by a single line through a multiplexer (Figure3.6).

Because there are 512 readout strips at one side in a DSSD, they are read by four VA1TA chips. These four chips are integrated on a hybrid circuit. Figure3.7 shows a picture of the VA1TA and the hybrid.
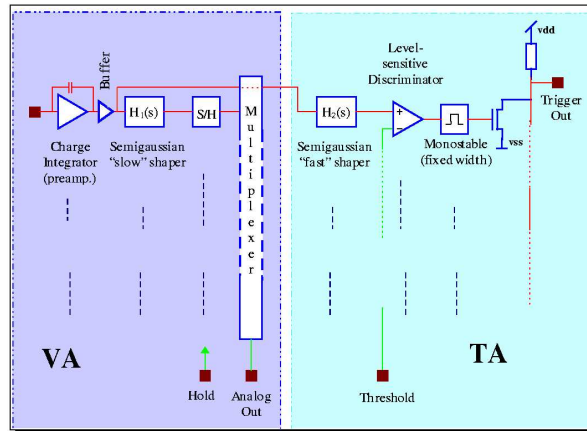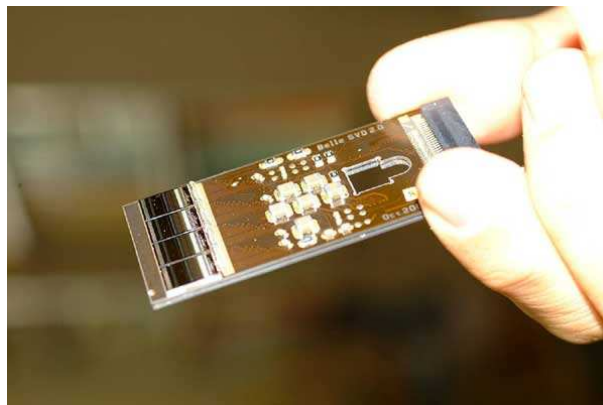

Figure 3.6: VA1TA diagram

Figure 3.7: hybrid picture

13

3.4 Readout system of the current SVD

Figure3.8 shows the readout system used in the SVD2. The function of each module is explained as follows:

CORE (COntrol and REpeater) system It consists of six repeater boards called REBO. The REBO sends the control signal or receives the analog signals from the VA1TA. MAMBO is the mother board which controls the REBO. The MAMBO also controls the power supply. The CORE system is encapsulated in a copper cooling box and it is called DOCK. The REBO is able to read 4 hybrid data, and six REBOs and one MAMBO is placed in the DOCK. Total ten DOCKs are used for the readout of the SVD.

FADC (Flash ADC) A flash ADC (FADC) is a 9U VME module that converts the analog signal from REBO into the digital signal at 5MHz and send it to PC via a PCI control. One FADC can read six hybrid data. In the SVD2, there are thirty-six FADC modules in total, and eighteen module out of them are used for the N-side readout and the other eighteen are used for the P-side readout.

TTM (Trigger Timing Module) TTM is a 6U VME module that controls the trigger signal and the DAQ system. TTM can send the signal such as ADC start, ADC stop, busy, and 4 bit event tag to the REBO and FADC, and it monitors and controls the readout cycle of the data. There are eleven TTM modules in total.

Power supply Power supply provides both High Voltage (H.V) and Low Voltage (L.V). The H.V is the bias voltage applied to the DSSDs for the depletion. The L.V is used for the front-end electronics.Each one of H.V and L.V supply is utilized for the one DOCK, and there are ten modules in total.

DAQ system Twelve PCs in total are used in the DAQ system of the SVD. It reads the data sent from FADC via the PCI bus. And then, the sparsified data are sent to the Belle event builder. One PC has three PCI boards and can read the data for three FADC modules.
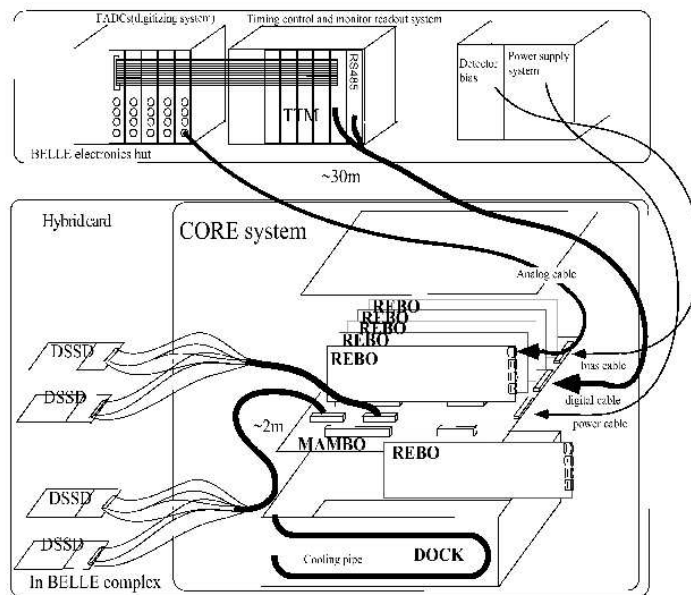
Figure 3.8: SVD readout system

3.5 Upgrade of the SVD

Currently, the luminosity of the KEKB accelerator reaches $1.6 \times 10^{34} \mathrm{cm}^{-2} \mathrm{s}^{-1}$, and a further luminosity improvement is planned. The luminosity of the KEKB will increase several times of the current value in 2007. Therefore, the SVD will be exposed by more radiations, and beam background level will increases.

Because of the higher luminosity for the KEKB upgrade, the occupancy in the first layer reaches $\sim 10\%$ (Figure3.9), where occupancy is defined as a fraction of the number of the hit strips over all the readout strips. As the occupancy increases, the detector performance degrades significantly. Therefore the modification of the SVD readout is necessary for the reduction of the occupancy.
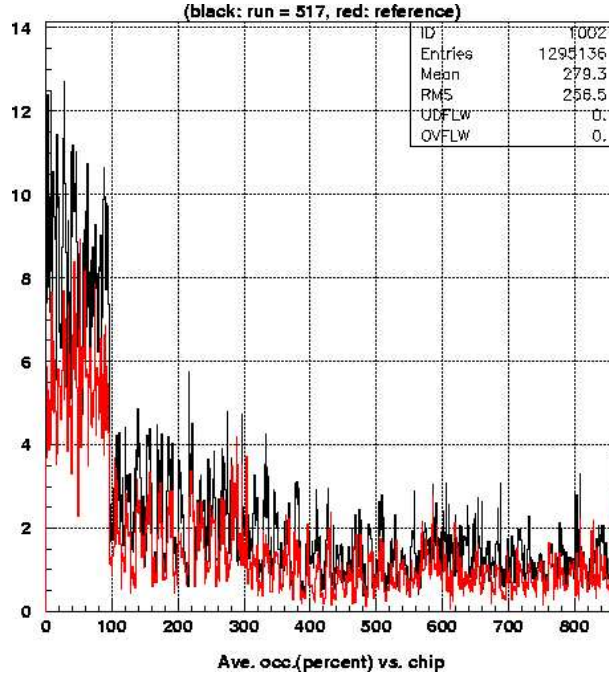
Figure 3.9: Occupancy vs. chip (Exp.47 Run:517)

In the present schedule, the luminosity of the KEKB accelerator will increase by three times in 2007. The upgrade of SVD is planned along with the schedule. We call the new SVD SVD2.5. The biggest improvement in the SVD2.5 is to replace the readout circuit in the first and second layer ladders. VA1TA used in the current SVD will be replaced by APV25 which has a faster shaper (~ 50ns). By this modification, the occupancy of the SVD is expected to be reduced by 1/16. Details of the APV25 will be described in next section.

3.6 APV25

The APV25 has been developed for a silicon detector used at CMS. It consists of a preamplifier, shaper, pipeline and multiplexer (Figure3.10). One APV25 chip has 128 input channels.

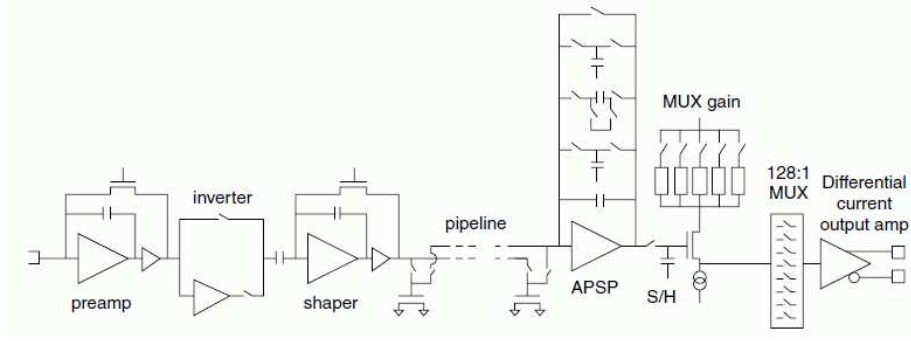Figure 3.10: APV25 block diagram

When the signal is fed to the APV25, it goes through a integrating preamplifier and it is shaped with some peaking time by the shaper. The output signal from the shaper is sampled at the clock intervals and stored in the pipeline. The pipeline of the APV25 is a ring buffer which has 192 cells with cycling write and read pointers. The signal stored at the pipeline is read after a certain constant latency time. The latency time between the signal input and the trigger is more than $4\mu s$ with 40MHz clock frequency. The signal that comes out from the pipeline is finally read in single line through the multiplexer.

APV25 has the sequencer that can generate a series of subsequent APV triggers initiated by a single hardware trigger. By using this feature, a sequence of samples separated by a single clock cycle can be obtained (multi-peak mode). This can be used to effectively get subsequent samples of the shaping curve from particle signal. The output signal from one APV chip in multi-peak mode is shown in Figure3.11.
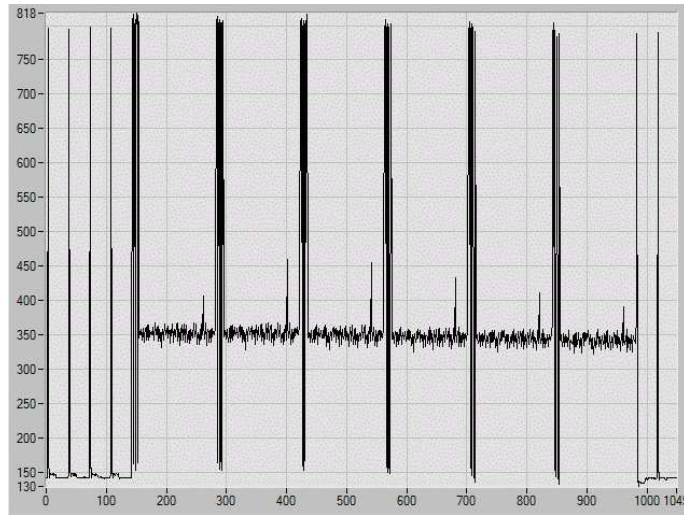

Figure 3.11: Output signal from APV25 in a 6 sample multi-peak mode

17

3.7 New design of DSSD for the upgrade

In the SVD2.5, the readout chips of the first and second layer ladders will be replaced from VA1TA to APV25. Therefore, DSSD of the inner layers should also be replaced. The main reason of this change is to reduce the detector noise. The noise from a semiconductor detector greatly depends on the detector capacitance in the case of short peaking time (Appendix A).

If we use the current DSSD with APV25, the noise from the detector capacitance will become larger. The current DSSD is designed to be minimized the radiation damage. Therefore, the strip width is maximized as much as possible and the interstrip capacitance is very large. Especially, the capacitance of the N-side is larger than P-side because of the P-stop. The noise from N-side will therefore become larger than that from P-side. The relation between detector noise and capacitance C with APV25 is,

$$Noise[\text{ENC}] = 270 + 38 \times C[\text{pF}], \tag{3.1}$$

where ENC is the equivalent noise charge. If we apply the LEP-SI model (Appendix B) for the capacitance calculation, we obtain a noise value of 415 (1125)enc for the P (N) side. The noise of the N-side is about two times as large as that of the P-side. In order to reduce the noise, we need to modify the DSSD design so as to minimize both P- and N-side capacitance. However, the sensor size is not changed since we want to keep the current DSSD arrangement.

The item that we can modify for a new DSSD of SVD2.5 are as follows:

1. Optimization of the strip width

2. Swap the readout direcitions (z and r-ϕ) between P and N sides

According to the LEP-SI model, the interstrip capacitance depends on the ratio of the strip width to the pitch size. Because z and r-ϕ strip pitch size of the DSSD have been decided to be 75μm and 50μm respectively beforehand, the interstrip capacitance is optimized by changing the strip width. The capacitance is also proportional to the strip length. The DSSD size is 25.6mm×76.8mm, and the strip length of r-ϕ side is longer than that of z. So the readout directions between P and N are swapped, and the capacitance of both side is kept balanced.

Every other strips on both side will be read out (floating strip connection). By employing this scheme, we can reduce both load capacitance and readout channels without degrading the position resolution. Since the bias voltage is applied to the strips, the charge generated at a floating strip is collected to its strip. Then, the signal is read by the adjacent strips through the interstrip capacitance.

However it is necessary to confirm whether the modified sensor is usable for our purpose. Especially, a charge loss may happen if a charged particle goes through a floating strip or goes between P-stops. So we need to study charge collection efficiency of a newly designed sensor with wide strip pitch and floating strip readout. We check the performance using N-side single-sided strip detector developed for determining new design of an SVD2.5 DSSD. From the next chapter, the various study of this sensor is described.

Chapter 4

Performance of a test sensor

In this chapter, details of a test sample used (the N-side SSD) are described. The leakage current, capacitance, and read out noise are measured.

4.1 Structure of the test sensor

The test sensor fabricated by HPK is an N-side single-sided strip detector (SSD). The test sensor is made since we want to determine the design of the N-side structure. In P-side, the whole region is implanted by P^+. The blue print of this sensor is shown in the Figure4.1.

Figure 4.1: N-side SSD blue print
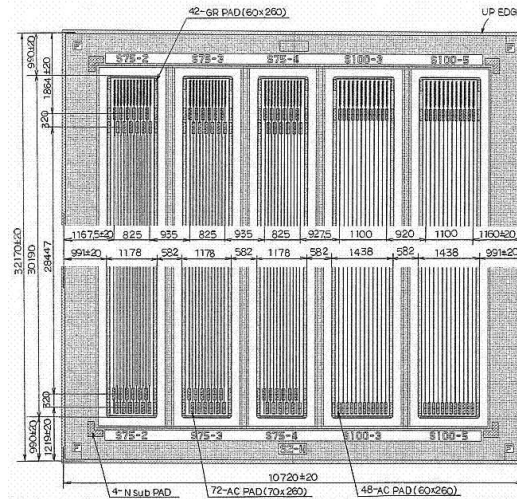
To optimize the strip pitch and width, we prepare different structure as shown in Table4.1, and the cross section view of the SSD is shown in Figure4.2.

The detail of one region in the sensor is shown in Figure4.3. In P-side, there are two slits perpendicular to strip direction. These slits are used for laser scan of the sensor. And there are individual bias pads through which we are able to

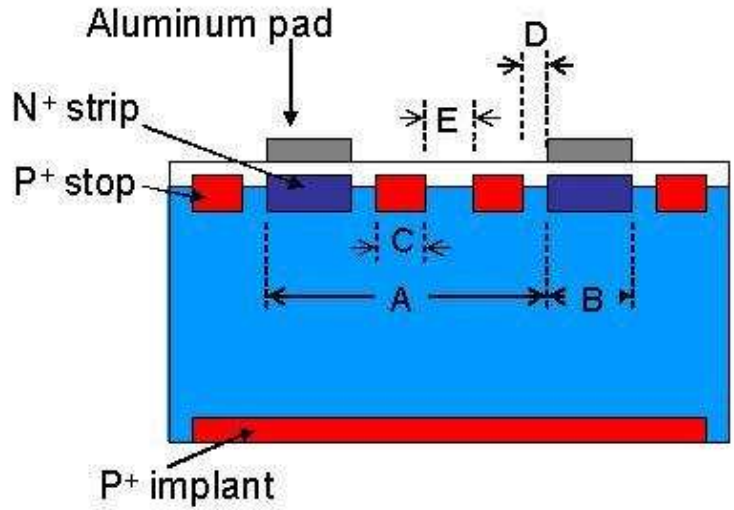|	S75-2	S75-3	S75-4
Sensor size [mm]	10.7 × 32.2		
Active area [mm]	8.3 × 28.4		
Strip pitch [μm] (A)	75		
Number of strips	12		
N-strip width [μm] (B)	32	24	12
P-stop width [μm] (C)	12	12	7
Gap between N-strip and P-stop [μm] (D)	6	6	6
Gap between P-stops [μm] (E)	7	15	37

Table 4.1: SSD parameters

Figure 4.2: The cross section view of the test sensor

apply bias voltage to individual regions. The leakage current can be measured individually. As described in Section 3.2, there are P-stop to insulate neighbor strips each other in N-side strip

4.2 A test sample

A picture of a test sample is shown in Figure4.4.

This test sample consists of the SSD described in Section 4.1, a bias line for the bias voltage, and a hybrid with 4 APV25 chips. The negative bias voltage (0 ∼ -80V) is applied to the sensor from the P-side. Every strip of the sensor is connected to the APV25 chip (floating strip connection).

This test sample was also used for the laser scan and the beam test described in Section 5 and Section 6.
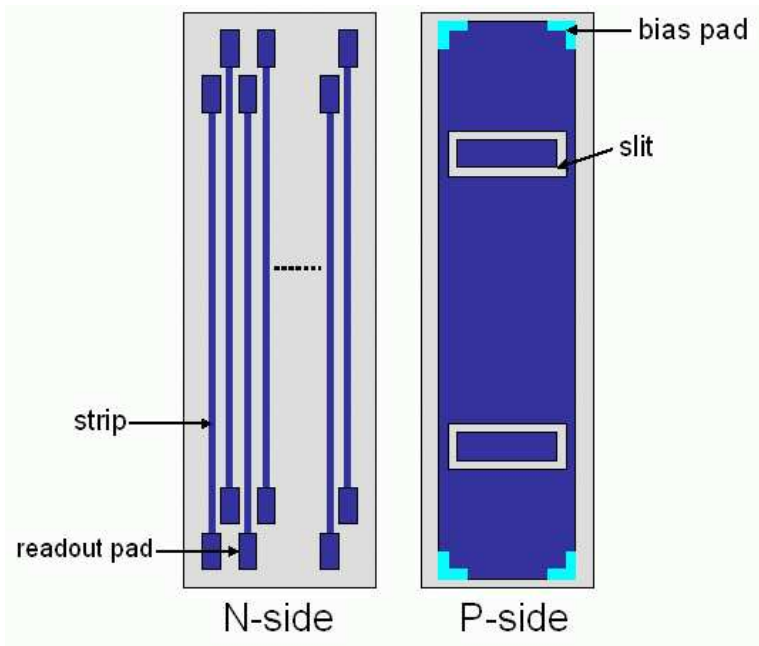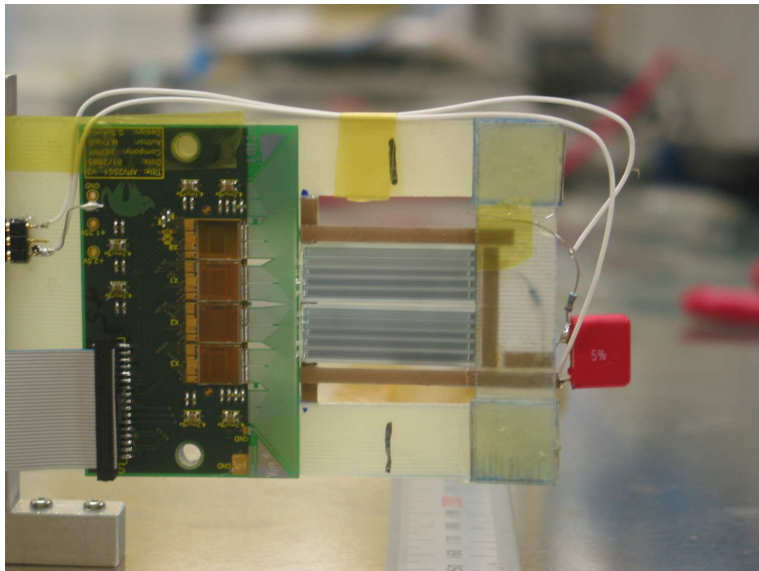
Figure 4.3: The detail of one area in the test sensor

Figure 4.4: Picture of the test sample

4.3 Readout from APV25

Figure4.5 shows a DAQ system of APV25 readout. The output from the APV25 chips are fed to APVDAQ through the AC Repeater.
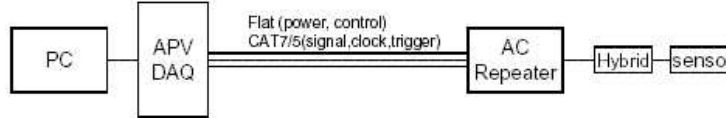

Figure 4.5: APV DAQ system

The APVDAQ (Figure4.6) is a 6U VME module used for the control and readout from the APV25 chip. It consists of a Stratix Altera, a VME protocol Altera, an ADC daughter board and supplemental electronics. On the front panel of APVDAQ, there are an analog signal input and an output for the controls (clock, trigger etc.), and these are connected to the Repeater with flat cable and CAT7 cables respectively. Furthermore, there are an external clock input and a trigger input on the front panel.

The AC reapeater is an interface between the hybrid and the APVDAQ. It bridges signals to the floating power scheme of the APV chip for clock, trigger, and analog signals.

The control of the DAQ system and readout of the analog data is carried out by a PC. The data acquisition software operates with the LabWindows/CVI developed by National Instruments. This software is written in the C programming language.

There are several operation types in the data acquisition system. The measurements are mainly performed with two operation modes: Hardware run and Internal calibration scan run. The Hardware run is a normal operation with an external trigger. The Internal calibration scan is used for the sampling of the APV output waveform. From these waveform data, the peaking time and chip gain can be calculated.

In a data acquisition, the VME board and APV are reset first. Next, APV25 chip parameters such as shaping time and number of samples are fixed. And then 600 events are taken by the internal triggers. These 600 events are used to calculate pedestal and noise. After that, a data acquisition with Hardware run starts.
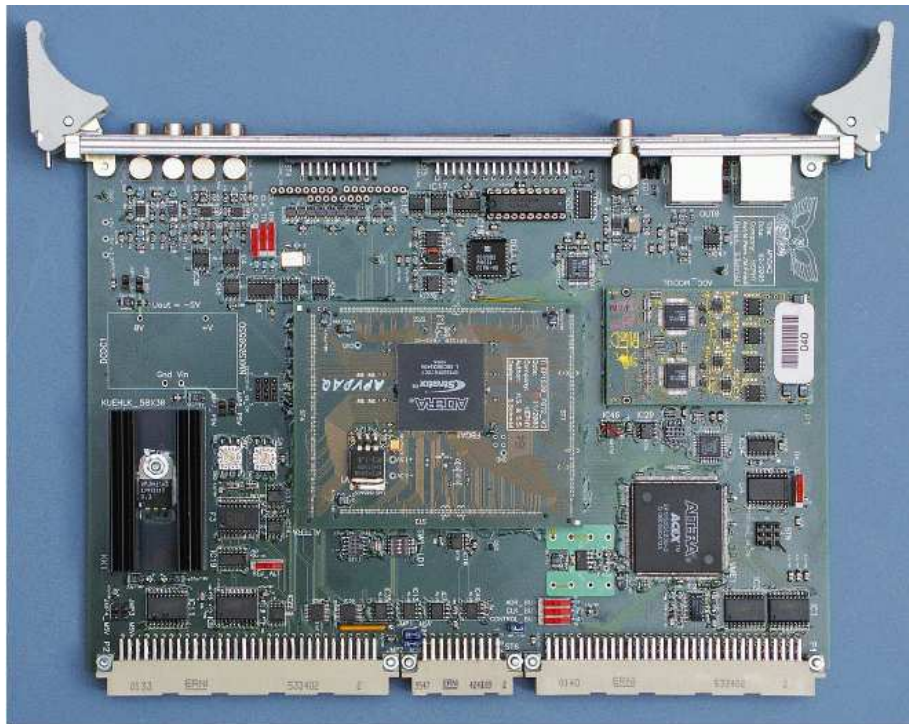
Figure 4.6: APVDAQ

4.4　Leakage current

In the semiconductor detector, the reverse bias voltage is applied for forming the depletion layer and collecting the carriers effectively. Under such condition, the electric current hardly flow because the carriers do not exist in the depletion layer. However, the sensor actually has certain conductivity and the leakage current flows constantly.

A DSSD used in the SVD has an oxide film (SiO_2) on the surface of the silicon bulk. The crystal structure of the boundary of Si and SiO_2 is discontinuous, and there is a distortion in the potential. It is called dangling bond. If electron and hole pairs are generated near the boundary with radiation, it is easy to be trapped. Since the mobility of an electron is three times as large as that of a hole, the hole is mainly trapped. A new energy level is made in the forbidden band by these trapped holes, and the leakage current flowing in the sensor becomes larger. This is the main cause of the radiation damage by γ-rays.

The leakage current is induced by trapped holes at the boundary of the sensor surface as described above. Therefore the surface damage by radiation is proportional to the boundary area. Because there are a lot of carriers in the implanted region, the nonimplanted region in the interstrips contribute more greatly to the leakage current. Therefore, The wider strip width make the smaller leakage current originating for the radiation damage.
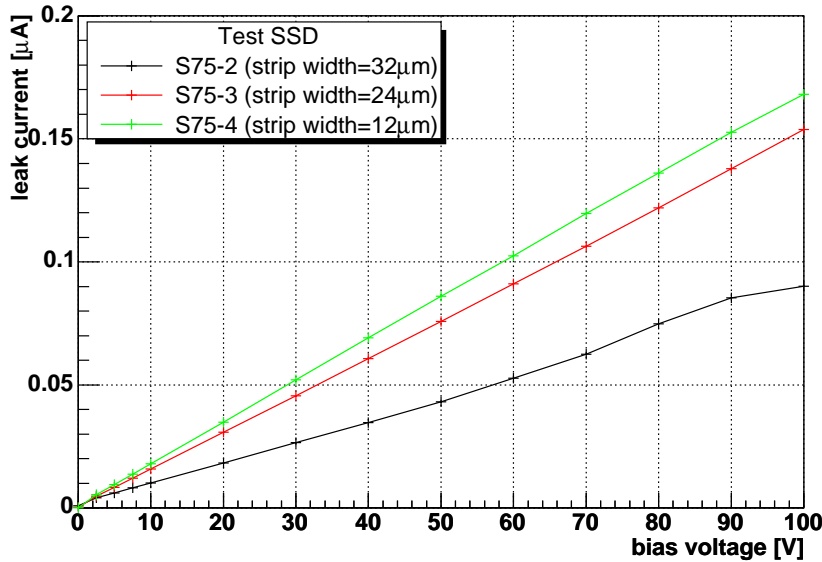

Figure 4.7: The bias voltage dependence of the leakage current

The test SSD has electonode pads through which the bias voltage is individually applied on each region. The leakage current of each region is measured with bias voltage applied to the P-side. The bias voltage is changed from 0 to -100V. The leakage current is measured one hundred times at each voltage

24

and the average is taken. Figure4.7 shows the bias voltage dependence of the leakage current in each region (see the Table4.1 for details of each region). The bias voltage is reversed in the horizontal axis. The region with narrow strip width and thus the large non-implanted region has the large leakage current. However, the leakage current in each region was very small and under 0.2μA. Therefore, it is expected that the shot noise from the leakage current is small in short peaking time of APV25.

4.5   Sensor capacitance

There are two kinds of DSSD capacitance: the interstrip capacitance C_i and the capacitance between strip and back plane C_b. Because the distance between P and N side is about 300μm, the back plane capacitance C_b is very small compare to C_i. So the interstrip capacitance C_i mainly contribute to the detector capacitance. According to the LEP-SI model (Appendix B), C_i is a function of the ratio of the strip width to the pitch size. Since N-side has the P-stop structure, N-side is more complicate than P-side and C_i becomes larger. The magnitude of these capacitance is determined by the sensor structure.

Figure4.8 shows the bias voltage dependence of the interstrip capacitance of each region. The bias voltage is reversed and displayed in the plot. The measurement is performed by applying 1MHz AC voltage between two adjoined strips. The bias voltage is applied from P-side and changed from 0 to -100V. The capacitance is measured one hundred times at each voltage and the average is taken.
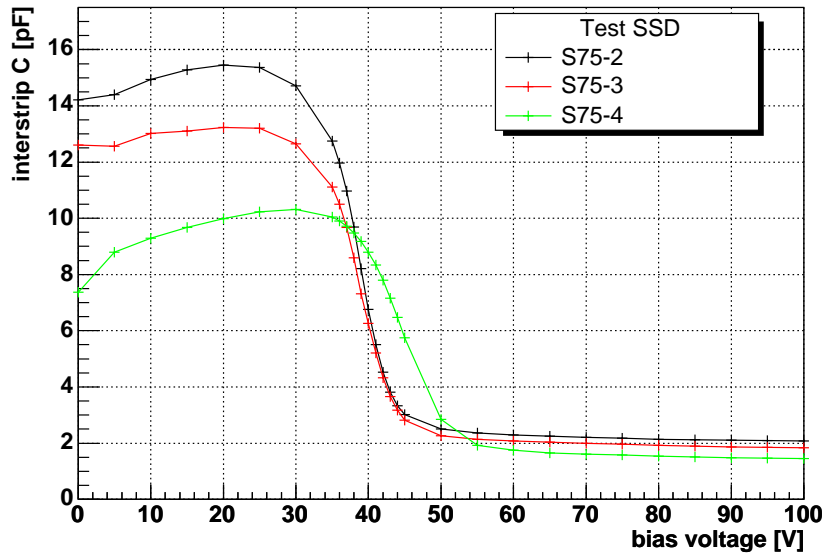

Figure 4.8: The bias voltage dependence of the interstrip capacitance

At the low bias voltage, the interstrip capacitance is large because a depletion

zone is not formed. As the bias voltage increases, the capacitance become small. At 60V or more, a depletion zone is completely formed and the capacitance is minimized. The interstrip capacitance with this bias voltage is about 2pF. The region with narrower strips width has smaller capacitance. Therefore the noise cause by load-capacitance is small for the narrow strip width. Table4.2 shows the interstrip capacitance in each region at 0, -20, -40, -80V bias voltage. Then, Table4.3 shows the interstrip capacitance calculated by LEP-SI model in each reigion. The measured capacitance is slightly smaller than LEP-SI model.

	S75-2	S75-3	S75-4
0V	14.2pF	12.6pF	7.4pF
-20V	15.4pF	13.2pF	9.9pF
-40V	6.7pF	6.3pF	8.8pF
-80V	2.1pF	1.9pF	1.5pF

Table 4.2: SSD interstrip capacitance

S75-2	S75-3	S75-4
2.6pF	2.3pF	1.6pF

Table 4.3: SSD interstrip capacitance by LEP-SI model

4.6   Peaking time dependence of the intrinsic noise

The sensor noise depends on the peaking time of the readout chip (Appendix A). APV25 can arbitrarily change the peaking time of the shaper output by changing the chip parameters. Since it is supposed that noise also depends on the shapring time, it is important to measure the noise with various shaping time.

The peaking time of APV25 was measured by the internal calibration mode. In this mode, a test pulse is fed to APV25 and the output of the shaper is observed. Figure4.9 shows the shaper outputs with three different peaking time.
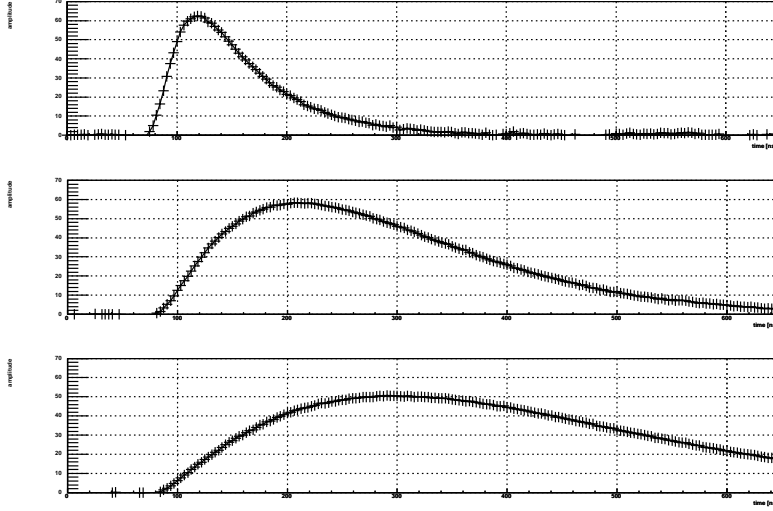

Figure 4.9: The shaping curve of APV25 output

The shaping time curve is discribed by the following formulas:

$$S_{out}(t) = A \cdot \frac{t - T_0}{T_p} \cdot e^{-\frac{t - T_0}{T_p}} \tag{4.1}$$

where A is the signal amplitude, T_0 is the time offset, and T_p is the peaking time. The peaking time is obtained by fitting the calibration data with this function. The sensor intrinsic noise is defined as the pulse signal fluctuation of each channel. The detail of intrinsic noise calculation method is described in Appendix C. The noise is averaged for each region and shown in the unit of ENC (Equivalent Noise Charge). The plot of the peaking time dependence of the sensor noise is shown in Figure4.10.

The measurement is performed with -80V bias voltage. It is shown that the noise decreases as the peaking time increases. In shorter peaking time, the noise of the S75-2 region having wide strip width is about 100 ENC larger than that of the S75-4 region having narrow strip width. This difference is due to the influence of the difference of the sensor capacitance. Table4.4 shows the intrisic noise at 50ns peaking time.
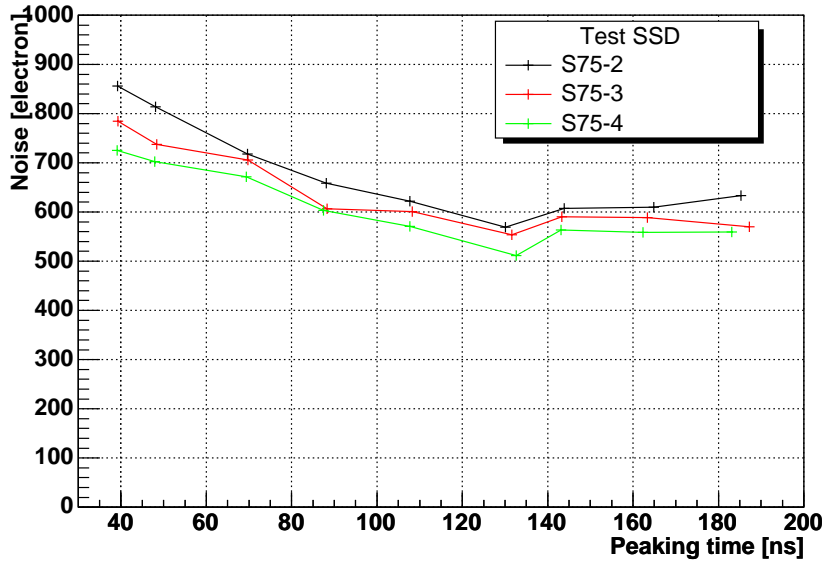
27

Figure 4.10: The peaking time dependence of the sensor noise

	Intrinsic noise [ENC]
S75-2	814
S75-3	737
S75-4	703

Table 4.4: Intrinsic noise

Then, the same measurement is done with bias voltage changed from -80V to -40V. Figure4.11, Figure4.12, and Figure4.13 show the peaking time dependence of the sensor noise of S75-2, S75-3, and S75-4 region.

In all the regions, the noises with -80V and -60V bias voltage are almost equal and rapidly increase with -40V. This is due to the rapid change of the interstrip capacitance around -40V shown in Section 4.5.

As a result, it has been confirmed that the sensor with narrower strip width is better in short peaking time. And so, it has been understood that the bias voltage greater than 40V is preferable at the experiment.
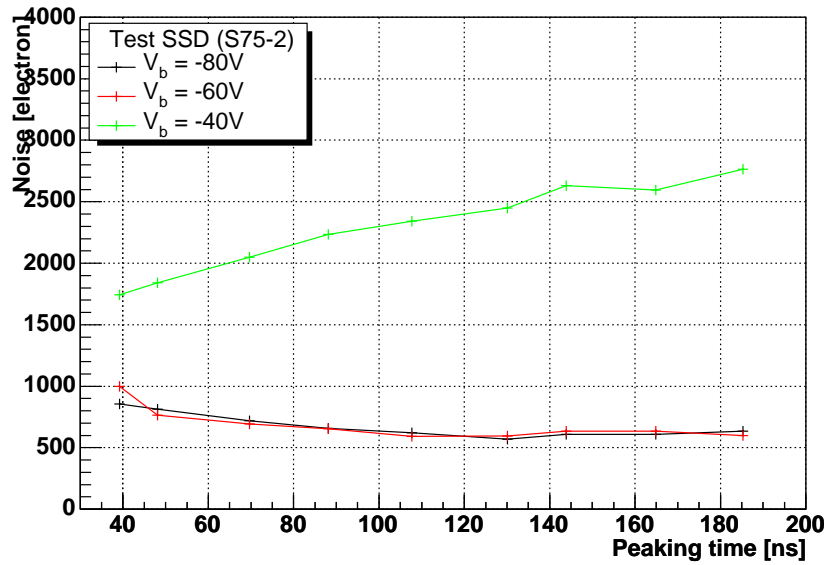
Figure 4.11: The peaking time dependence of noise in -80, -60, -40V bias voltage (S75-2)
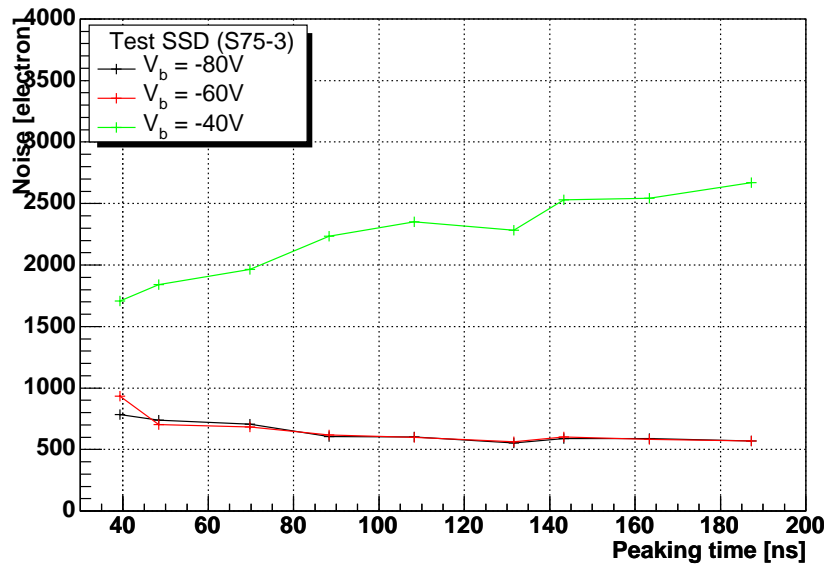

Figure 4.12: The peaking time dependence of noise in -80, -60, -40V bias voltage (S75-3)
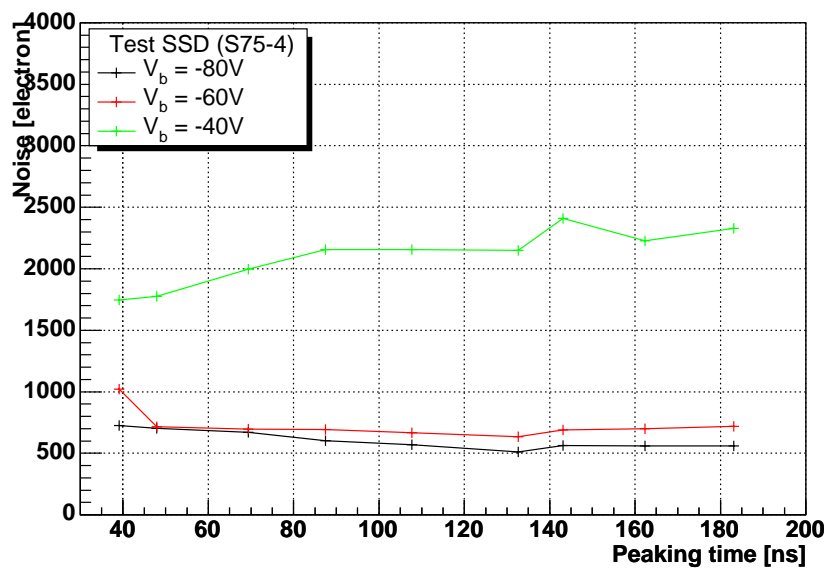
Figure 4.13: The peaking time dependence of noise in -80, -60, -40V bias voltage (S75-4)

Chapter 5

Laser scan

In this chapter, a laser scan on the test sensor is described. The test sensor used for this laser scan is the same as described in Section 4.2.

5.1 Purpose of the laser scan

As described in Chapter 3, the new DSSD is read with floating strip connection. The electric charges collected by a floating strip are read by the adjacent strips through the interstrip capacitance. There may be charge loss however. In order to study the charge loss, I perform the laser scan and see the amount of charge collected. One of the advantages to use a laser is that we can identify the illuminated position with an accuracy of a few μm, since the spot size is the same order.

5.2 Detail of laser system and measurement procedure

A laser used at this measurement is Picosecond Light Pulser (PLP-01) produced by HPK. This consists of a controller and a laser diode head. The pulse width is less than 50ps and can be adjusted. It has an external trigger input and it can irradiate the laser light according to arbitrary timing. The detail of this laser is shown in Table5.1.

Wave length	$859nm$
Wave length tolerance	$< \pm 10nm$
Peak power	$23mW$
Pulse width	$50ps$
Timing pulse jitter	$< \pm 10ps$

Table 5.1: Characteristic of Hamamatsu PLP-01 Light Pulser

The wave length of this laser is 859nm. The light stops near the silicon surface and its energy is deposited completely. Figure5.1 shows energy distribu-

tion of the laser light. The energy is distributed around 150 ADC counts. The output of laser is stable with ∼5% level.
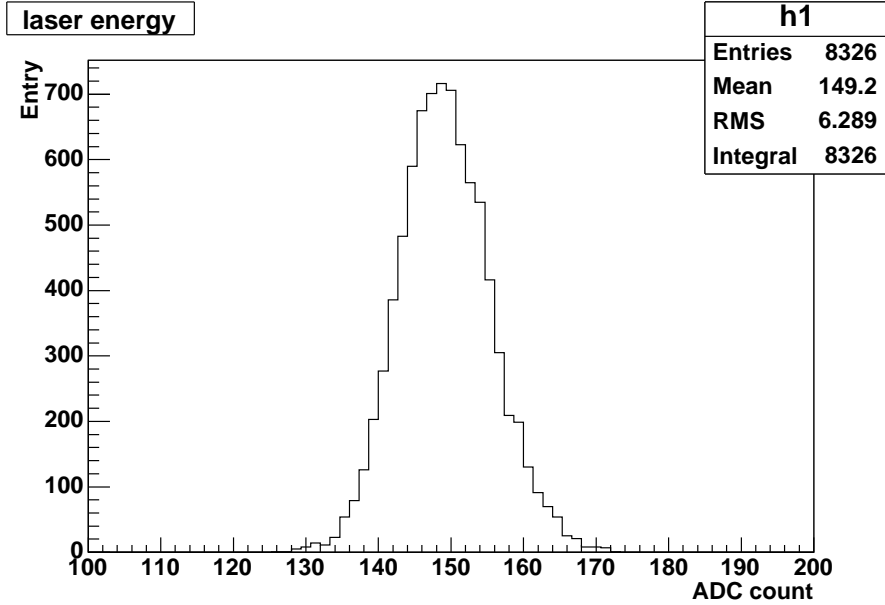

Figure 5.1: The energy distribution of laser output

The laser light is injected to the slit on the P-side, and the electron charge are collected by the N^+ strips.

The laser injection position to the sensor is varied using motor movable table system. The motor movable system consists of a table and two motors. A microscope and a fiber optics cable from the laser light source is arranged on the table. The table can be moved in two directions by the two motors. The table can move with 0.25μm step. The motors are controlled by a PC, and these can be operated with the data acquisition synchronously.

Figure5.2 shows an overview of the laser scan system. The APV25 readout is carried out by APVDAQ described in Section 4.3. The motor control and the data acquisition is operated by one PC through the VME modules. The trigger signal for the laser light output and the data acquisition is generated by a pulse generator. The data acquisition trigger is delayed by about 800ns than the laser light trigger. The laser light signal is detected almost surely in one event. A picture of the system is shown in Figure5.3.

Figure5.4 shows a data taking flow chart of the laser scan. Six hundred event data for the pedestal and noise measurement are taken after APV25 initialization. In this measurement, we use the 50ns peaking time and the 6 sample multi-peak mode. The trigger timing is adjusted such that the shaping curve peak is found in second sample. The trigger signal is generated by pulse generator with 1kHz rate.

The laser light is injected to the P-side slit of the sensor, and is scanned to the direction perpendicular to the N^+ strips. The sensor is moved with a step size of 1μm and 100 events data are taken at the each point. To prevent from
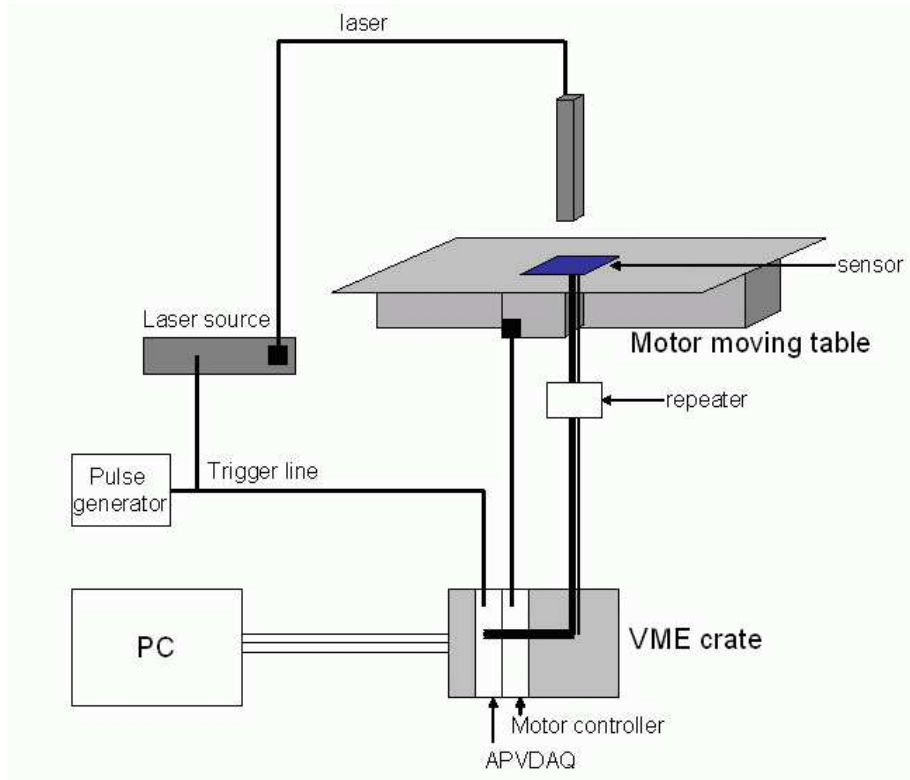
Figure 5.2: The schematic diagram of laser scan system

the noise from the motor, we leave the system for 1 second between the motor operation and the data acquisition.
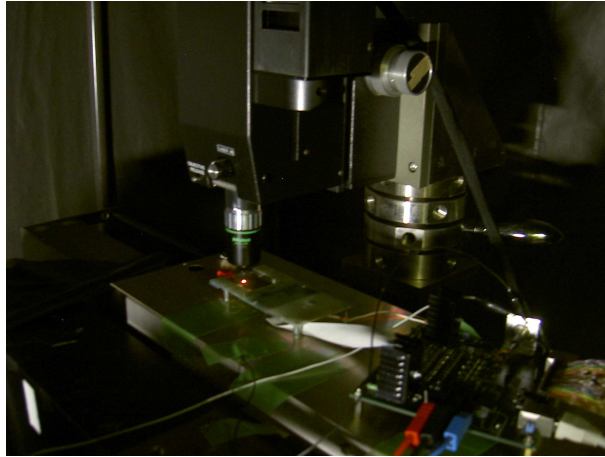
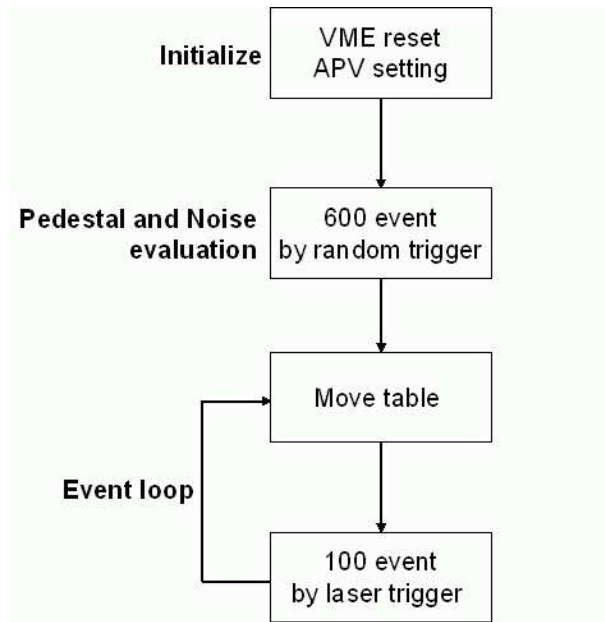Figure 5.3: A picture of the laser scan system

Figure 5.4: A data taking flow chart of the laser scan

5.3   Analysis procedure

First I calculate pedestal and noise, and then obtain signal charge yield. The definition of pedestal and noise is described in Append C. The six sample data are taken with an interval of 25ns in one event. Since the trigger timing was adjusted so that shaping curve peak is found in a second sample, only the second sample data are used. The signal of each channel is obtained by subtracting pedestal and common mode shift (CMS) from raw ADC data. The CMS is calculated for every event. In the calculation of the CMS, we remove the strips whose signal-to-noise ratio (S/N) is greater than 3. If we find an event in which more than half of all the strips have a S/N ratio greater than 3, we regard this event as a noise event, and discard it. Then, we extract strip data which have large signal yields (S/N>5). Figure5.5 shows an example event of the signal yield obtained by the laser scan.
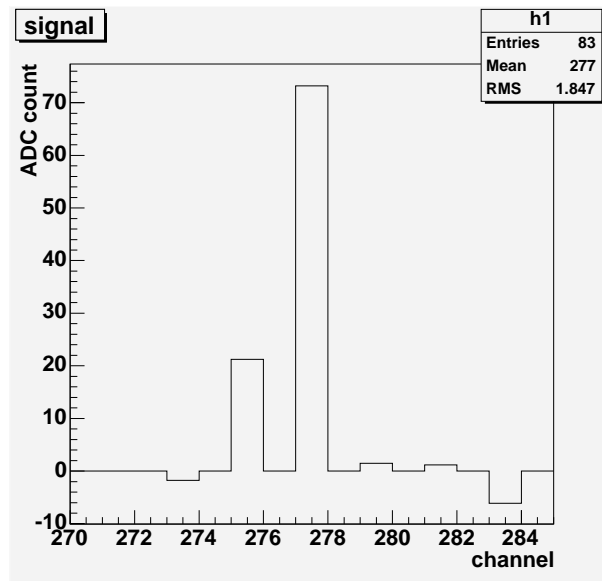

Figure 5.5: The signal plot of laser scan

5.4   Measurement result

5.4.1   Charge sharing of the floating strips

The charge sharing of the floating strips and its charge loss are estimated. The signal yield of each channel at each scan point is measured. Then, a sum of the yield of all the channels is calculated. The charge sharing is studied by comparing the yield between floating strip and readout strip. Figure5.6, 5.7,and 5.8 show charge sharing of the laser scan of S75-2, S75-3, and S75-4 region.

The black line is the sum of the signal yield of all the channels and the other color lines are the yield of each channels. The readout strips are located at the peak position of each curve in the plot. The yield of each channel decreases as the light injection point goes away from the readout strip. There is a position where the curve slope becomes flat at middle of two readout strips. This is the floating strips. The curve was continuous over all the scan region and the charge sharing is found to be smooth.

The shape of one channel is different among the three regions. The curve of the yield of S75-4 is more gradual and the peak width is narrower than S75-2 and S75-3. This is due to the difference of the strip width. For the narrower strip region, the charge sharing occurs more easily than other wide ones.

Because the laser light output is almost steady, the sum of the yield is also stable. However, the yield at the floating strip is obviously smaller compared with those at the readout strips. This is caused by the charge loss. To evaluate the charge loss in each region, the charge collection efficiency at the floating strip is calculated. The sum of the yield signal at the readout and floating strips are compared. Table5.2 shows the charge collection efficiency of floating strips for each region. The charge collection efficiency is more than 85% at all the

Charge collection efficiency	
S75-2	0.89
S75-3	0.85
S75-4	0.86

Table 5.2: Charge collection efficiency at floating strip

regions, and S75-2 region gives slightly higher efficiency than other two regions. Since S75-2 has wider strip width, the charge loss is the smallest. Although the difference between three regions is small, it is necessary to evaluate the charge sharing with charged particles penetrating the SSD.
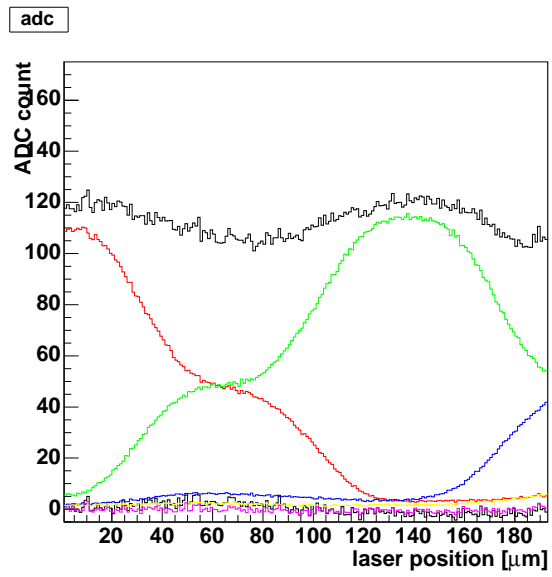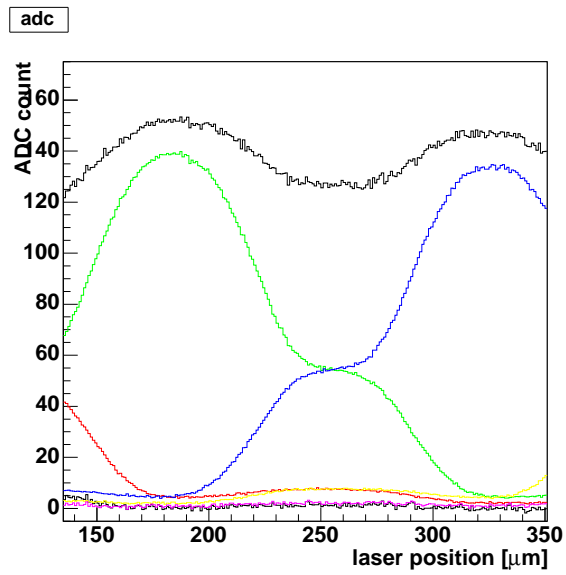
Figure 5.6: The charge sharing of laser of S75-2

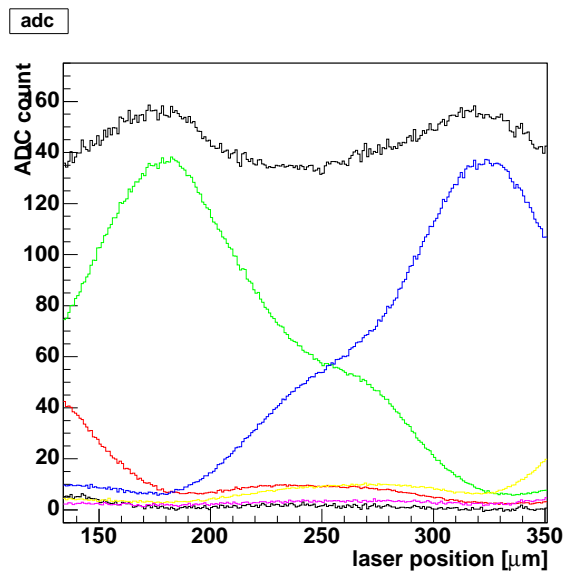Figure 5.7: The charge sharing of laser of S75-3

Figure 5.8: The charge sharing of laser of S75-4

5.4.2 Position resolution estimation with the laser scan

The position resolution is obtained by comparing the position between the light injection position and the weighted scan position of the strip yield. The laser light injection position is arbitrarily varied. At each injection position, the hit strips whose signal-to-noise ratio are greater than 3 is found in one event data. The position is obtained by the center of gravity method.

The correlations of measured position and the true position between two readout strips of S75-2, S75-3, and S75-4 are shown in Figure5.9, 5.10, and 5.11. The horizontal axis is the true position and the vertical axis is the measured position. In all the plots, the readout strips is located at 0 and 150μm, and the floating strip is located at 75μm. The slope of the correlation is gradual around 0, 75, 150μm in all plots. This tendency is especially strong in S75-2. The correlation curve of S75-2 is disconnected at the position $\sim10\mu$m and $\sim140\mu$m. This is because all the created charges are collected by a single strip. The measured position spread in S75-2 is smaller than that of other regions. This is because the charge collection efficiency of the readout strip is the largest.

The position resolution is measured. Figure5.12, 5.13, and 5.14 show the residual distributions of S75-2, S75-3, and S75-4, respectively. S75-2 has double peaks in the residual distribution. This is because the S75-2 has the wider strip width and therefore the charge collection by the floating strip is also large. The RMS values of residual distributions are shown in Table5.3. In all the regions, The RMS is about 10μm. Although the spread of the charge sharing is small in S75-2, the RMS becomes large because of the double peaks in the distribution. The center of gravity method is not useful in S75-2. As a result, the S75-4 has the smallest position resolution in the three regions.

	RMS [μm]
S75-2	8.8
S75-3	10.6
S75-4	8.2

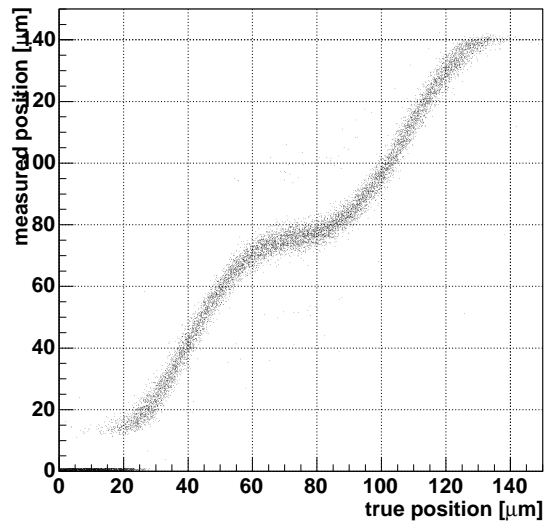Table 5.3: RMS of residual distribution

Figure 5.9: The correlation of position of S75-2
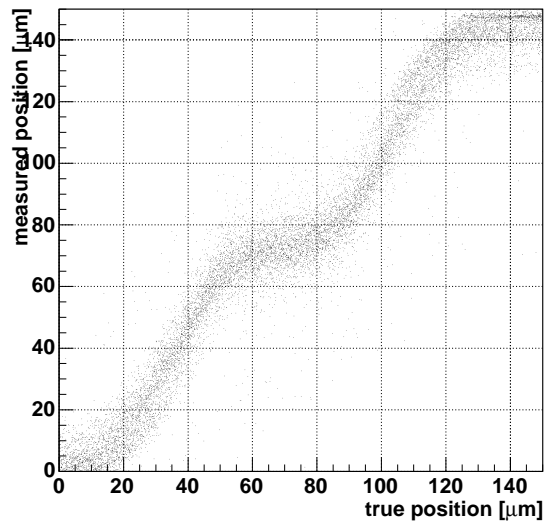

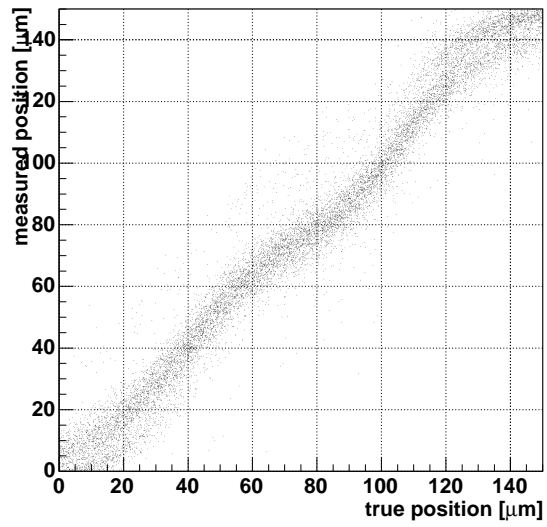Figure 5.10: The correlation of position of S75-3
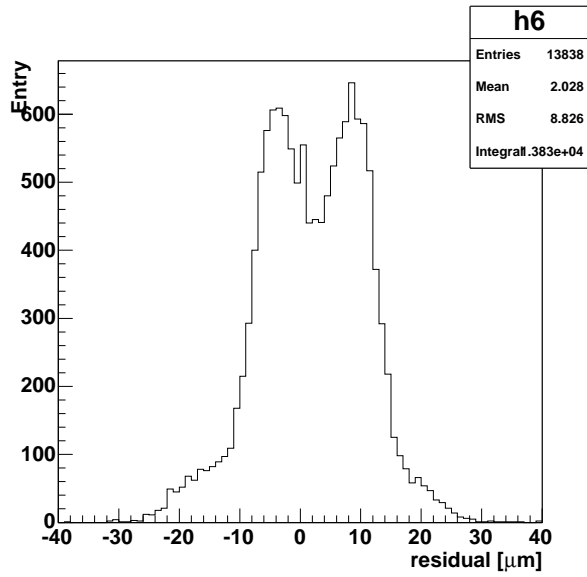
Figure 5.11: The correlation of position of S75-4
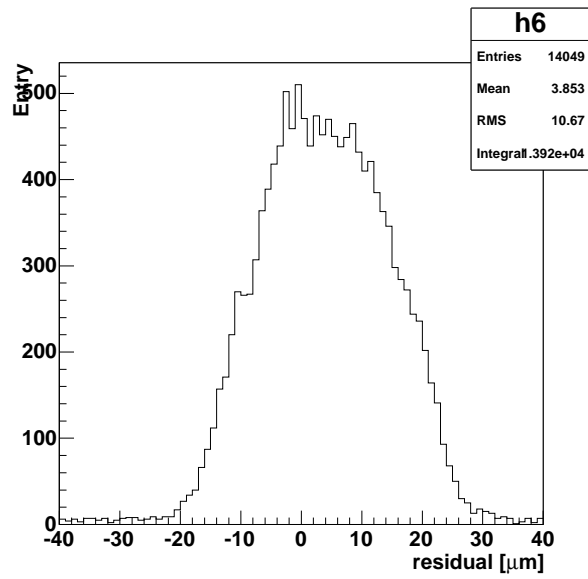

Figure 5.12: The residual distribution of S75-2

Figure 5.13: The residual distribution of S75-3
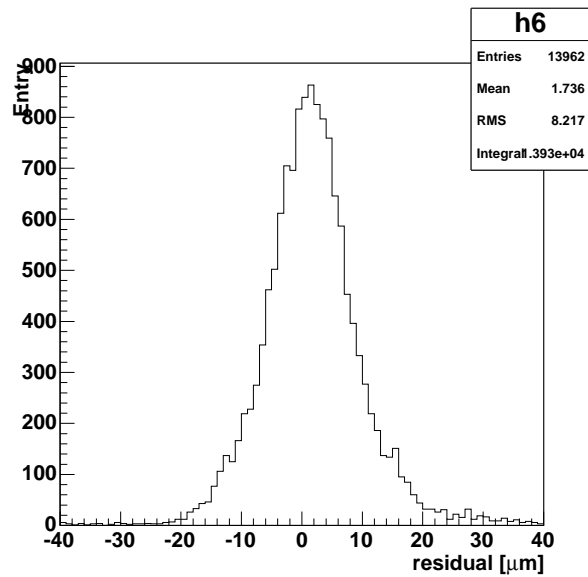
Figure 5.14: The residual distribution of S75-4

Chapter 6

Beam test analysis

In this chapter, I will describe the detail of the beam test which was conducted at KEK in December, 2005. As described before, we need to evaluate the charge sharing with charged particle.

6.1 Outline of the beam test

There are two purposes for this beam test. One is the study of the test sensor with the APV25 readout with the charged particle beams. The other is the investigation of the interference between VA1TA and APV25 when both are operated simultaneously. The beam test was performed at the KEK/PS $\pi 2$ beam line (Figure6.1) in December, 2005.
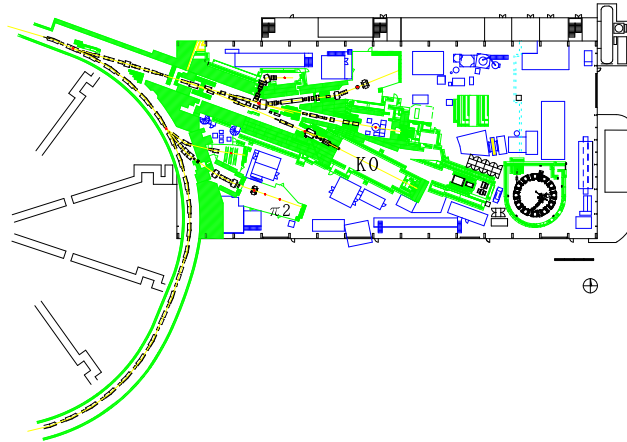
Figure 6.1: The beam line in KEK/PS

In this research, I concentrate the first purpose. In particular, cluster energy and charge sharing are studied in more detail. Since we use a charged pion beam,

we can know the detector response as same as that of the real operation of the SVD. Therefore the analysis result of this beam test data is closely connected to the real operation of the SVD2.5.

6.2   Test detector for beam test

The test detector used at the beam test consists of the test sample (Figure4.4) and three DSSD ladders (Figure6.2). The used ladders are the spare layer-1 ladders of SVD2. This DSSD is slightly different from the SVD2 DSSD currently operated: there is no aluminum electnode pad on the floating strip in P-side.

A layout and a picture of the detector are shown in Figure6.3 and Figure6.4.

Figure 6.2: Test ladder picture

Figure 6.3: Test detector layout

Figure 6.4: Test detector picture

6.3 Detail of the readout system and experiment

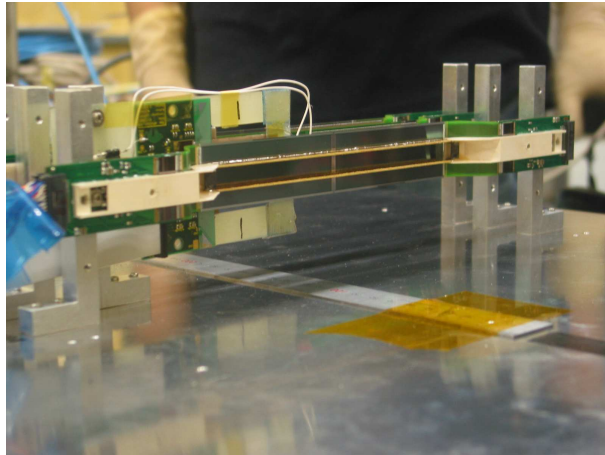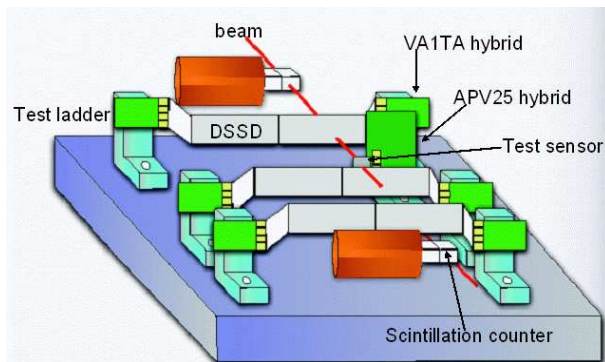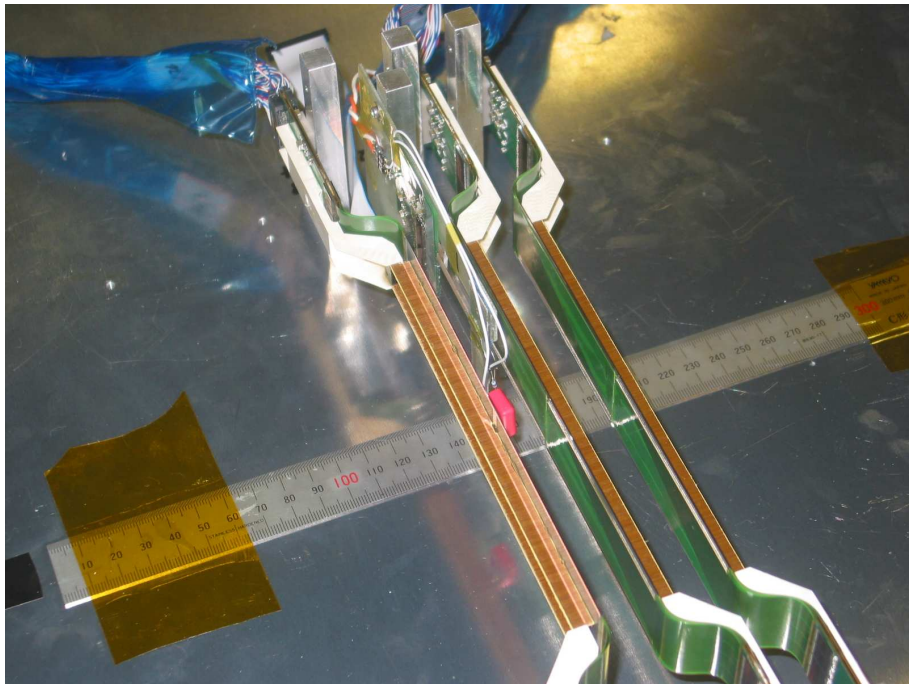I describe the readout system in this section. In SVD2.5, we will operate the APV25 and VA1TA synchronously. For the readout of the APV25, APVDAQ explained in Section 4.3 is used. For the readout of the VA1TA, the same system as the actual SVD readout described in Section 3.4 are used. Total three DSSDs (six hybrids) are read in this beam test. Two REBOs, and one FADC are therefore operated.

The coincidence of the signals of two scintillation counters is used for a generation of trigger signals. The trigger signal is fed to the APVDAQ and TTM. After trigger acceptance, a veto signal is issued from both APVDAQ and TTM. By using the veto signal, we can avoid the event slip between APV25 and VA1TA. In the VA1TA data, there is a 4bit event tag used for event number information. In this beam test, the event tag is sent to the APVDAQ and used to match the event between APV25 and VA1TA data acquisition.

A schematic diagram of the readout system is shown in Figure6.5.
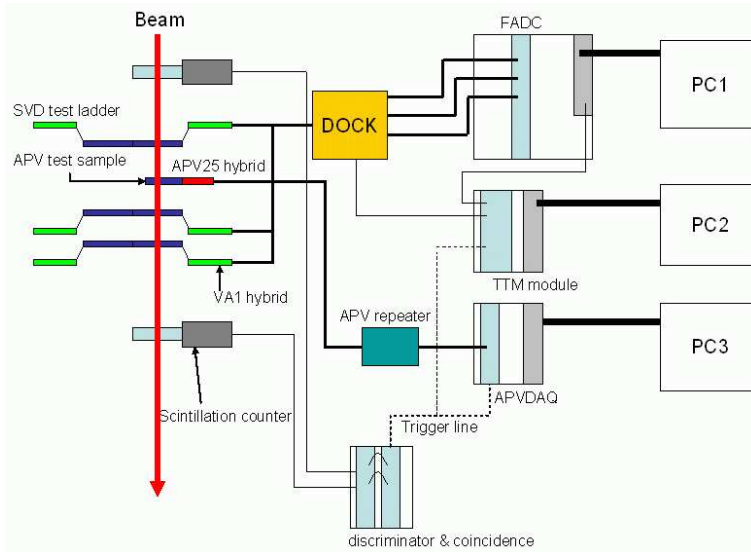
Figure 6.5: A Schematic diagram of readout system at the beam test

In this beam test, the data were taken with various APV25 conditions. The main conditions that we change are the peaking time, number of samples in multi-peak mode, trigger timing, and bias voltage of the sensor. In the VA1TA side, all the data were taken with the same condition. The particle beam energy could also be chosen. In this time, the data were taken with 4GeV/c π^- beam. We collected 100,000 events for each APV25 condition.

6.4   Analysis procedure

In this section, I describe the analysis procedure. We employ the same method as the one described in Section 5.3 for the noise calculation and pedestal and CMS subtraction.

To find hit signals, we reconstruct clusters based on the observed strip charge yield. In many cases, the hit signal consists of two or more adjoined strips. This is called a cluster. To find a signal cluster, we search for a seed strip whose signal-to-noise ratio is greater than the seed strip threshold C_{seed}. Then, if the signal-to-noise ratios of the neighboring strips of the seed strip are greater than the cluster strip threshold C_{strip}, those strips are combined to one cluster. Because the beam is injected to the sensor almost vertical, we expect that the cluster width is a few strips. We accept the cluster width up to 5. Then, a signal-to-noise ratio of each cluster is calculated as follows,

$$S/N_{clust} = \frac{\sum_i S_i}{\sqrt{\sum_i N_i^2}}, \tag{6.1}$$

where S_i and N_i are signal and noise of ith channel. If the cluster signal-to-noise ratio is greater than the threshold C_{clust}, this is considered as a true hit cluster. In this analysis, C_{seed}, C_{strip}, and C_{clust} is set to 5.0, 3.0, and 10.0, respectively. Then, the cluster reconstruction of VA1TA data is also performed with the same manner. We combine the APV25 and VA1TA data based on the event tag information. Then, we select an event that has cluster signals in the all four layers.

The beam hit position is calculated using the center of gravity method using the cluster. Because the SSD is used, only the one dimension position information can be obtained.

6.5 Experiment result

The analysis result of the beam test is described here. The data used for the analysis were taken with 50ns peaking time, 6 sample multi-peak mode, and -80V bias voltage.

6.5.1 Cluster energy

Figure6.6, 6.7, and 6.8 shows the cluster energy distributions of S75-2, S75-3, and S75-4, respectively A Landau-Gaussian function is used to fit the distribution. This function is a convolution of Landau and Gaussian functions. The energy loss of a charged particle in material follows the Landau distribution. However, the electric noise is always superimposed to the hit signals. Therefore the observed hit signal distribution becomes a Landau convolved with a Gaussian components from the noise.

The peak value of the distribution in each region is described in Table6.1. The peak value differs in each region. We suspect that this is due to the difference of the charge loss. Compared with Table4.4, the signal-to-noise ratio are more than 30 in all regions.

	Peak value [electron]
S75-2	25945
S75-3	24868
S75-4	22580

Table 6.1: The peak value of cluster energy distribution
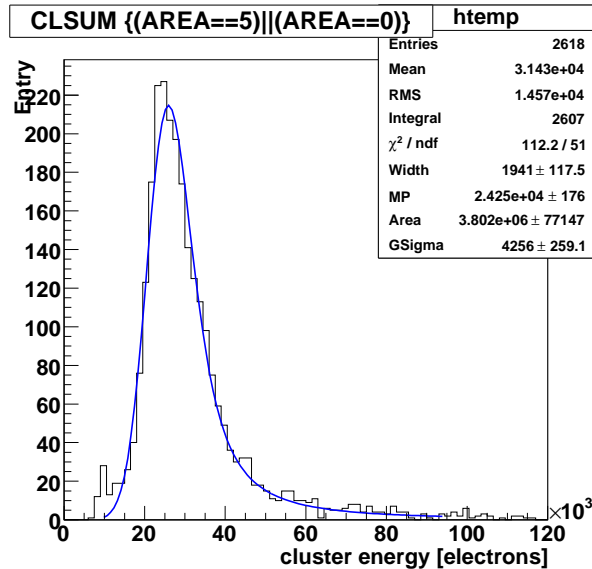
Figure 6.6: The cluster energy distribution of S75-2

48

CLSUM {(AREA==6)||(AREA==1)}	htemp	
Entries		2580
Mean		3.039e+04
RMS		1.328e+04
Integral		2561
χ^2 / ndf		63.38 / 50
Width		1999 ± 109.3
MP		$2.332\text{e+}04 \pm 171$
Area		$3.831\text{e+}06 \pm 77451$
GSigma		3857 ± 201.7
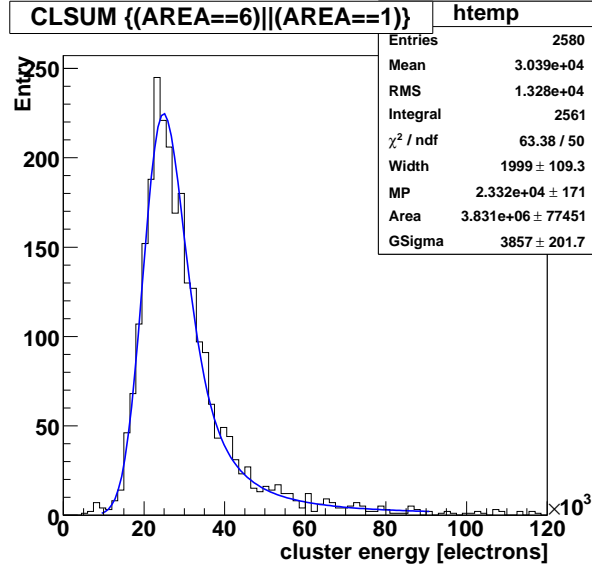
Figure 6.7: The cluster energy distribution of S75-3

CLSUM {(AREA==7)||(AREA==2)}	htemp	
Entries		2806
Mean		2.727e+04
RMS		1.341e+04
Integral		2803
χ^2 / ndf		81.65 / 46
Width		1819 ± 108.0
MP		$2.091\text{e+}04 \pm 165$
Area		$4.114\text{e+}06 \pm 80299$
GSigma		4251 ± 235.4

Figure 6.8: The cluster energy distribution of S75-4

6.5.2 Charge sharing

Figure6.9, 6.10, and 6.11 show plots of cluster energy vs measured incident position of S75-2, S75-3, and S75-4, respectively. The horizontal axis of the plot is the measured cluster position between two strips calculated with center of gravity method. The readout strips is located at 0 and 150μm and the floating strips is located at 75μm. The vertical axis is the cluster energy. In this plot, I divide the two strip interval into 15 regions and calculate the averaged cluster energy in each interval. The mean value with RMS is plotted at each position. The mean value slightly decreases as the strip width reduces. The value around readout or floating strips are extracted and the charge collection efficiency of the floating strip to the readout strip is calculated. Table6.2 shows the charge collection efficiency at each region. The collection efficiency is slightly low compared with laser scan result (Section 5.4). This is because of smearing by the position resolution.

	Charge collection efficiency
S75-2	0.87 ± 0.01
S75-3	0.81 ± 0.01
S75-4	0.84 ± 0.01

Table 6.2: Charge collection efficiency at floating strip
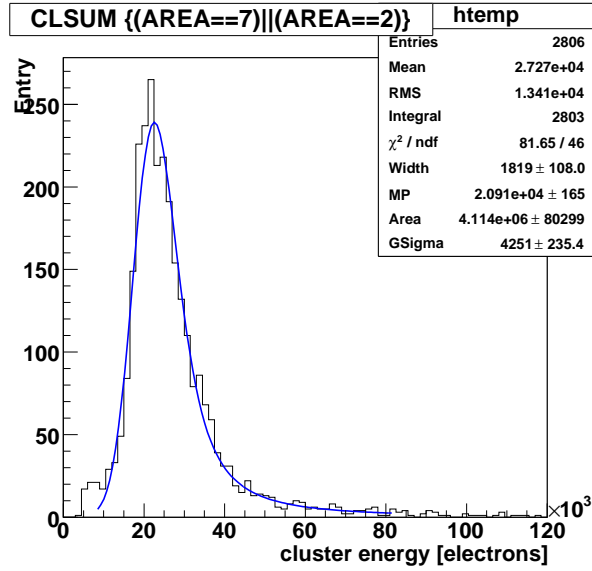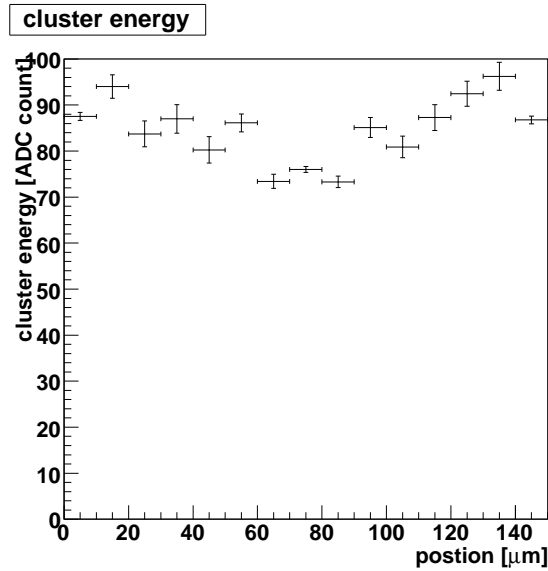

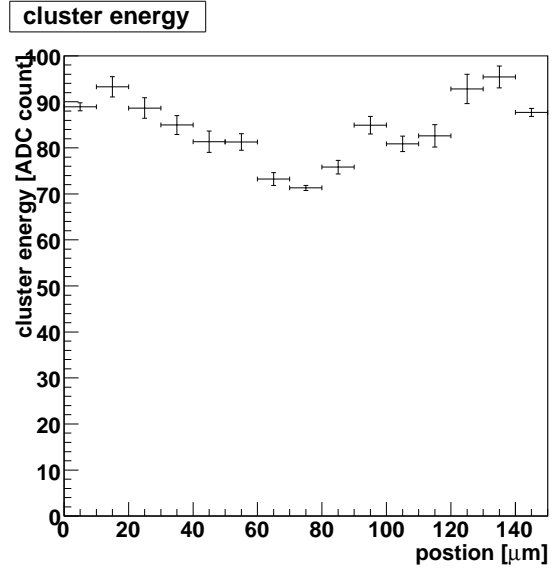Figure 6.9: The cluster energy vs. position in S75-2

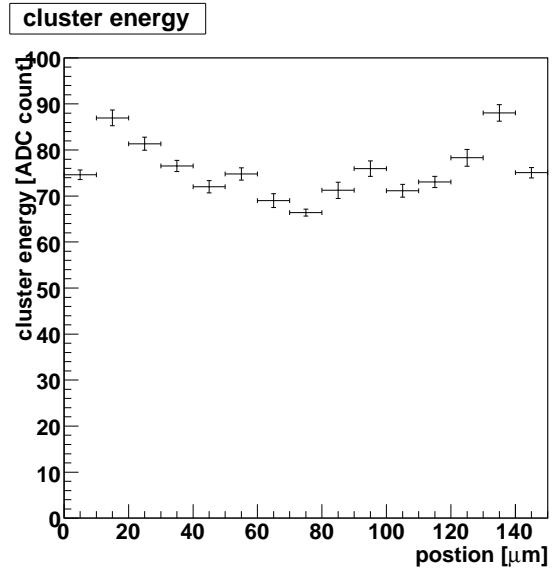Figure 6.10: The cluster energy vs. position in S75-3

Figure 6.11: The cluster energy vs. position in S75-4

6.6 Summary of all the analysis result

Table6.3 shows all the analysis result.

	S75-2	S75-3	S75-4
Intrinsic noise [ENC]	814	737	703
Position resolution [μm]	8.8	10.6	8.2
Cluster energy [electron]	25945	24868	22580
S/N	31.9	33.7	32.1
Charge collection efficiency	0.87$\pm$0.01	0.81$\pm$0.01	0.84$\pm$0.01

Table 6.3: All the analysis result

The intrinsic noise with APV25 readout are less than 1000 ENC and the signal-to-noise ratio for the charged particle are more than 30. The position resolution are estimated to be about 10μm. The charge collection efficiency of the floating strips is more than 80% and the charge loss are small. All the regions can be used at the actual operation without problem. Especially, the S75-4 region has the good position resolution and low noise. Finally, S75-4 parameters are the best in the three from overall result.

Chapter 7

Conclusion

To cope with a further luminosity improvement of KEKB accelerator, a new Silicon Vertex Detector (SVD2.5) is planed to be installed in 2007. The main improvement of the SVD2.5 are the replacement of the readout chip to APV25 which has faster shaping time. The purpose of this thesis is to optimize a new Double-sided Silicon Strip Detector(DSSD) for the APV25 readout. We study the performance of the test sensor which has the different types of strip parameters with APV25 readout.

First, the detector intrinsic noise is evaluated. We find that the detector noise with fast shaping time is less than 1000 ENC for all the types. In the laser scan, the position resolution is estimated to be about $10\mu m$ in all the region. In the beam test, we study the sensor response of the charged particle. The charge collection efficiency is found to be 79~85% in all the types. As a result, we find that all the regions can be used for the actual operation without any problem. We choose S75-4 parameters as the best among the three from the overall result.

As a future task, we will study the influence of the radiation damage. The radiation dose of the SVD is expected to increase greatly by the luminosity improvement. Especially, the leakage current of the sensor increases by γ-ray irradiation and the shot noise become larger. Therefore, it is necessary to evaluate its radiation hardness by irradiating γ-rays to the sensor.

We design a prototype DSSD for the SVD2.5 based on these results. We have adopted the parameters of S75-4 which has the lowest noise in the N-side. The parameter of prototype DSSD is described at Appendix D.

Appendix A

Intrinsic noise of semiconductor detector

The intrinsic noise of a semiconductor detector is mainly caused by the detector leakage current and electric capacitance. The magnitude of these noise sources is evaluated by the detector design. Therefore it is very important to estimate these contribute to the noise for the detector design. The noises caused by the leak current and capacitance are given by the following equations:

$$ENC_{leak} \propto \sqrt{I_{leak} T_{peak}}, \qquad (A.1)$$

$$ENC_{capa} \propto \frac{C}{\sqrt{T_{peak}}}, \qquad (A.2)$$

where I_{leak} and C is the leakage current and the load capacitance of one strip, and T_{peak} is the peaking time of the shaping curve in readout chip. ENC is the noise in equivalent noise charge. Because these noise sources are not correlated, the total noise equals to a square sum of each noises. According to the above two equations, the shot noise caused by the leakage current become dominant if the peaking time is long. On the other hand, the noise caused from detector capacitance become dominant if the peaking time is short.

Appendix B

LEP-SI model

LEP-SI model is used for the estimation of the detector capacitance. the details of this model is describe in [2] and [6].

A DSSD has a finite number of strips with a certain width placed regularly. In this model, the interstrip capacitance C_i is a function of the ratio of strip width W to strip pitch p.

$$C_i = \begin{cases} \frac{\epsilon}{\pi} \ln(2\frac{1+\sqrt{k}}{1-\sqrt{k}})L & 0 \leq k \leq 0.7 \\ \frac{\epsilon \pi}{\ln(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}})}L & 0.7 \leq k \leq 1.0 \end{cases} \qquad (B.1)$$

where $k = W/p$, $k' = \sqrt{1-k^2}$, ϵ is the dielectric constant of silicon, and L is the strip length. FigureB.1 shows the calculated capacitance as a function of k with $L = 30mm$.
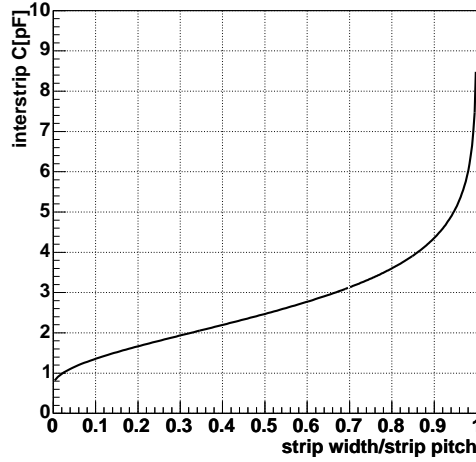

Figure B.1: The plot of interstrip capacitance at LEP-SI model

Appendix C

Evaluation of pedestal and noise

In all the measurements with APV25, 600 events are taken first for pedestal and noise evaluation by the internal trigger. Here, I describe the calculation method of pedestal and noise.

The first 300 events are used for the pedestal calculation. The pedestal is an offset ADC value of each channel. The signal yield from the sensor is obtained by subtracting this pedestal from the raw data. The pedestal of each channel is calculated by averaging 300 events,

$$P_i = \frac{1}{300} \sum_{j=1}^{300} ADC^j{}_i, \qquad (C.1)$$

where $ADC^j{}_i$ is an ADC count of ith channel in jth event. The second 300 events are used for noise calculation. Noise is defined as the RMS of the signal. There are two kinds of noises. The first one is the intrinsic noise caused by the leakage current and the detector capacitance. The intrinsic noise is different in each channel. The second one is the external noise. The external noise influences the entire chip and ADC count changes with the same amount for all channels. This noise is called a common mode shift (CMS). CMS is obtained by averaging pedestal subtracted ADC count for one chip in one event.

$$C^j = \frac{1}{128} \sum_{i=1}^{128} (ADC^j{}_i - P_i) \qquad (C.2)$$

The intrinsic noise is calculated as the RMS of the signal by subtracting both pedestal and noise.

$$N_i = \sqrt{\frac{1}{300} \sum_{j=301}^{600} (ADC^j{}_i - P_i - C^j)} \qquad (C.3)$$

56

Appendix D

The prototype DSSD for SVD2.5

The following table shows the parameters of prototype DSSD.

	P-side	N-side
Chip size[mm]	$79.6 \times 28.4 \times 0.3$	
Active area[mm]	77.6×26.0	
Strip pitch[μm]	25.5	76
Number of readout strips	512	512
Number of floating strips	512	512
Readout pitch[μm]	51	152
Strip width[μm]	10	12

Table D.1: Prototype DSSD specification

Acknowledgment

Bibliography

[1] M.Friedl (Vienna University of Technology) Doctor Thesis (2001)

[2] R.Abe (Niigata University) Master Thesis (2002)

[3] H.Kurashiro (T.I.T) Master Thesis (2005)

[4] F.Ohno (T.I.T) Master Thesis (2002)

[5] J.Kaneko (T.I.T) IEEE Trans. Nucl.Sci., VOL49,NO.4 (2002),1593

[6] D.Hussun IEEE Trans. Nucl.Sci., VOL41,NO.4 (1994),811