Upgrade of the Belle Silicon Vertex Detector

M.Friedl*

(for the Belle SVD Collaboration)

Institute of High Energy Physics, Nikolsdorfergasse 18, A-1050 Vienna, Austria

Abstract

The Belle experiment at KEK (Tsukuba, Japan) was inaugurated in 1999 and has delivered excellent physics results since then, which were, for example, recognized in the Nobel Prize award 2008 to Kobayashi and Masukawa. An overall luminosity of $895\,\mathrm{fb}^{-1}$ has been recorded as of December 2008, and the present system will be running until $1\,\mathrm{ab}^{-1}$ is achieved. After that, a major upgrade is foreseen for both the KEK-B machine and the Belle detector.

Already in 2004, the *Letter of Intent for KEK Super B Factory* was published. Intermediate steps of upgrade were considered for the Silicon Vertex Detector (SVD), which performs very well but already got close to its limit regarding the occupancy in the innermost layer and dead time. Eventually it was decided to keep the existing SVD2 system until $1\,\mathrm{ab}^{-1}$ and completely replace the silicon detector as well as its readout system for Super-Belle.

The future SVD will be composed of double-sided silicon sensors as the present detector, but equipped with faster readout electronics, namely the APV25 chips originally made for CMS at CERN. Moreover, it will be enlarged by two additional layers and equipped with a double layer of DEPFET pixel detectors surrounding the beam pipe. The silicon sensors will be fabricated from 6" wafers (compared to the current 4" types) and the readout chain will be completely replaced, including front-end, repeaters and the back-end electronics in the counting house.

Key words: Silicon Vertex Detector, Belle, KEK, B Factory, APV25, DEPFET

1. Introduction

The KEK-B machine is located at the KEK laboratory in Tsukuba, Japan. It is an asymmetric storage ring colliding beams of electrons and positrons at 8 GeV and 3.5 GeV, respectively, with an unprecedented luminosity of up to $1.7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. So far, about $900\,\mathrm{fb}^{-1}$ of data have been recorded by the Belle experiment, mostly at the $\Upsilon(4S)$ resonance, corresponding to almost a billion $B\bar{B}$ pairs, which are used to study CP violation.

The 2008 Nobel Prize of Physics was partly awarded to Makoto Kobayashi and Toshihide Masukawa for their theoretical work on CP violation and prediction of three generations of quarks. In the official press release, the Royal Swedish Academy explicitly mentioned that the experiments BaBar in Stanford and Belle at KEK [1] verified the hypothesis of Kobayashi and Masukawa. While BaBar is already completed, this honor further motivates the Belle collaboration to continue and improve its work.

The KEK-B will run until early 2010. Afterwards, a major upgrade is intended for both the machine (Super-KEK-B) as well as the detector (tentative name: Super-Belle), with an ultimate luminosity goal of about $5 \ldots 8 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, up to 50 times higher than now. The commissioning of the new machine in foreseen in 2013.

The current Belle Silicon Vertex Detector (SVD2) [2] consists of four layers of double-sided strip detectors made from 4" wafers. It suffers from about 10% occupancy in the innermost layer due the slow shaping time constant of the VA1TA amplifier [3] and a few percent of dead time due to lack of a pipelined readout. It is obvious that this system cannot cope with the conditions of Super-B and thus needs replacement. Already a few years ago, a replacement of the innermost layer (and later of layers one and two) was considered, as a significant luminosity boost was expected after the installation of crab cavities, which would in turn deteriorate the tracking performance because of excessive occupancy. However, this did not come true and consequently, the intermediate upgrade was unnecessary and thus dropped. Instead, the plan is to completely renew and enlarge the vertex detector in the future.

2. Super-Belle Vertex Detector

The future Vertex Detector will cover the same polar angle range ($17° \ldots 150°$) as the current SVD2, but extend to a radius of about 14 cm, compared to less than 9 cm at present. Consequently, it will contain more layers and most importantly, a pixel detector will be introduced in

*Corresponding author, Phone: +43-1-5447328-38, Fax: +43-1-5447328-54

Email addresses: friedl@hephy.at (M.Friedl)

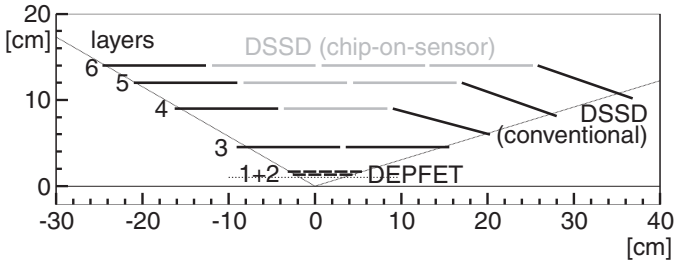

Figure 1: Conceptual design of the Silicon Vertex Detector for Super-Belle, consisting of two pixel layers surrounded by four double-sided silicon strip layers with some slanted sensors in the forward region. The edge detectors will be conventionally read out from the sides, whereas the inner sensors will make use of the Origami chip-on-sensor concept. All silicon strip sensors will be made from 6" wafers.

the innermost part. The new system has to feature a high background tolerance and a pipelined readout in order to avoid the shortcomings of the current detector and enable robust tracking in a high-luminosity environment.

Fig. 1 gives an overview of the tentative Super-Belle SVD layout. The two innermost layers at radii of 1.8 and 2.2 cm will be populated by DEPFET [4] pixel detectors. Their sensing element is the buried gate of a field effect transistor which is essentially switched on by a traversing particle. As the substrate is fully depleted, the charge collection efficiency is excellent and allows thinning down to a thickness of 50 μm while maintaining a comfortable signal-to-noise ratio of 20 . . . 40.

The four double-sided silicon strip layers will be entirely composed of 6" wafers with some slanted sensors in the forward region in order to reduce the number of detectors and readout channels. In the present SVD2, up to three sensors are ganged and the front-end amplifiers are located outside of the acceptance region. Although this is a beautiful concept in terms of material budget, it cannot be maintained in the future system, where every sensor must be read out individually. This necessity arises from the application of the APV25 readout chip with short shaping time in order to reduce the occupancy, which is inherently more susceptible to noise. As the main contribution to the noise figure is load capacitance, it is neither possible to concatenate strips between sensors nor to route individual strips from inner sensors to the edges outside of the acceptance.

3. APV25 Readout Chip

The APV25 chip [5] was originally developed for the CMS Silicon Tracker at CERN. It has an adjustable shaping time of about 50 ns and an analog pipeline of 192 cells which operates at the clock frequency of 40 MHz (default). Its equivalent noise charge (ENC) of $250e^- + 36e^-/pF$ is naturally higher than the slow-shaping VA1TA in the present Belle SVD, yet lowest in its league. These properties make the APV25 an ideal choice for the future Belle Silicon Vertex Detector.

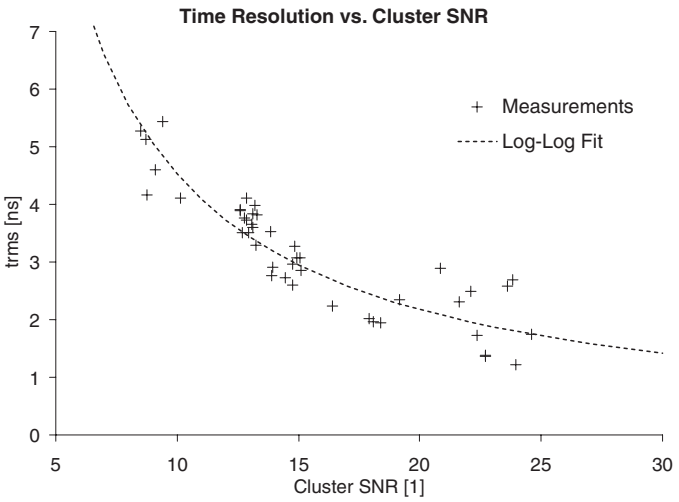

Figure 2: Timing precision of the APV25 obtained with a waveform fit in beam tests using various double-sided prototype sensors for the Belle SVD upgrade. In a double-logarithmic mode, the measured points can be fit by a straight line.

In CMS, the APV25 chip is used in the so called *deconvolution mode* by default, which is an on-chip switched capacitor filter that essentially narrows the resulting (sampled) pulse shape down to a single clock cycle by a weighted sum of three consecutive samples at the cost of increased noise. This feature allows to attribute measured hits to a specific bunch crossing and thus is invaluable to reduce ambiguities. However, it requires a clock-synchronous beam, and thus cannot be used with a quasi-continuous beam at (Super-)KEK-B.

Nevertheless, we can take advantage of a related built-in feature called *multi-peak mode*, where several consecutive samples along the shaped waveform can be read out. Together with an off-chip pulse shape reconstruction, one can determine the peaking time with a precision of 2 . . . 5 ns, depending on the Signal-to-Noise ratio, as measured in various beam tests and shown in fig. 2.

We have shown that the three highest samples of the shaping curve are sufficient to determine the peak with good accuracy. For the future SVD readout, we will implement this functionality into FPGAs (Field Programmable Gate Arrays) which process the digitized APV25 data using look-up tables for online hit time reconstruction. Together with reference timing information obtained from the TOP (Time of Propagation) counter, this feature will allow additional online occupancy reduction. Altogether, we expect up to 100 times lower occupancy than in the current SVD2 system, referring to the same luminosity.

4. Origami Chip-on-Sensor Concept

Sensors at the edge of acceptance can be read out from the side, using proper flex fanout circuits, which will add some capacitance at an acceptable level. The only solution for inner sensors, however, is to put the readout chips directly onto the detectors. Naturally, this raises questions

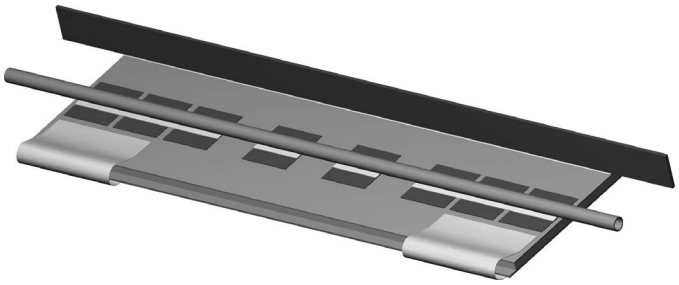

Figure 3: 3D rendering of a double-sided prototype module using the Origami chip-on-sensor concept.

of material budget and cooling. We devised an elegant way to accomplish this chip-on-sensor concept for double-sided sensors while minimizing the material for both readout and cooling, called *Origami*, because it uses short pieces of flex circuit folded around the edge of the sensor.

Fig. 3 shows a graphical representation of the Origami module. This prototype is currently under construction with a 4" double-sided silicon detector read out by four APV25 chips on either side. All chips are aligned on the top side (the face farther away from the interaction point), such that they can be cooled by a single, thin aluminum pipe which also serves as one of two structural elements. The center APV25 chips are fanned out to the short strips on the top face of the sensor, which are mostly covered by an insulation layer of Rohacell styrofoam and the Kapton hybrid. The outer four ASICs read the long strips on the bottom face of the sensor, which are connected by fanout circuits wrapped around the edge of the detector.

In order to reduce the material budget, the APV25 chips were already successfully thinned down to $100\,\mu$m. Although the two groups of four readout ASICs sit on voltage potentials which are separated by the bias voltage of the sensor (typically 80 V) and thus have to be electrically isolated from each other, the Kapton circuit design for the hybrid was accomplished with just three layers. Taking everything into account, we estimate an overall averaged material budget of $0.72\%\,\mathrm{X}_0$ compared to about 0.48% for the conventional construction with long fanout lines (which render an unacceptable noise figure). Thus, the Origami sacrifices some additional material for a significant gain in signal-to-noise.

The chip-on-sensor concept was already tested with the APV25 for single-sided readout. In 2006, the so called *Flex-Module* was constructed, using the same 4" double-sided silicon detector. Only the short strips were read out by chips on top of the sensor, while the long strips were connected from the side in a conventional way. This module yielded excellent results in beam tests [6].

5. Readout Chain

A VME-based readout system was developed for an intermediate upgrade, where only the innermost two layers of the SVD2 should have been replaced with APV25 readout. It consists of a single controller module which sends clock, trigger and slow control information to the front-end, together with FADC+Processor modules which digitize and process the received APV25 data before they are passed on to standardized COPPER DAQ modules [7].

About 30 m of cable length towards the front-end, repeater boards are located which buffer signals in both directions and perform the voltage level translation between ground (VME side) and bias voltage levels (detector side) by means of capacitive coupling for clock, trigger and analog signals as well as optocouplers for slow controls. The detector modules are connected to the repeater boards by about 2 m of cable.

It is doubtful whether this system can be scaled up to the full Super-Belle SVD size, as there is limited space in various locations. Consequently, several parts, especially the repeaters close to the front-end, must become much more dense than in the prototype system. R&D is ongoing and various possible solutions are under study.

6. Summary

The Silicon Vertex Detector of the future Super-Belle experiment will have to cope with up to 50 times higher luminosity than present. It will be equipped with two layers of DEPFET pixel sensors surrounded by four silicon strip layers, extending to a radius of about 14 cm. With its fast shaping, the APV25 readout chip is able to handle the expected hit rates at low occupancy. The effective sensitive time window can be further cut down through online hit time reconstruction, using multiple samples along the shaped waveform. This feature will be implemented in FPGA hardware. As noise strongly depends on the capacitance and hence the length of fanout lines, each sensor must be read out individually with short connections. This is accomplished by the Origami chip-on-sensor concept, where thinned APV25 chips sit on top of the inner sensors with minimum amount of material yet including cooling. Large R&D effort is now being put into the future Silicon Vertex Detector, which shall become operational in 2013.

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