Heavy Photon Search
Electronics, DAQ, & Software

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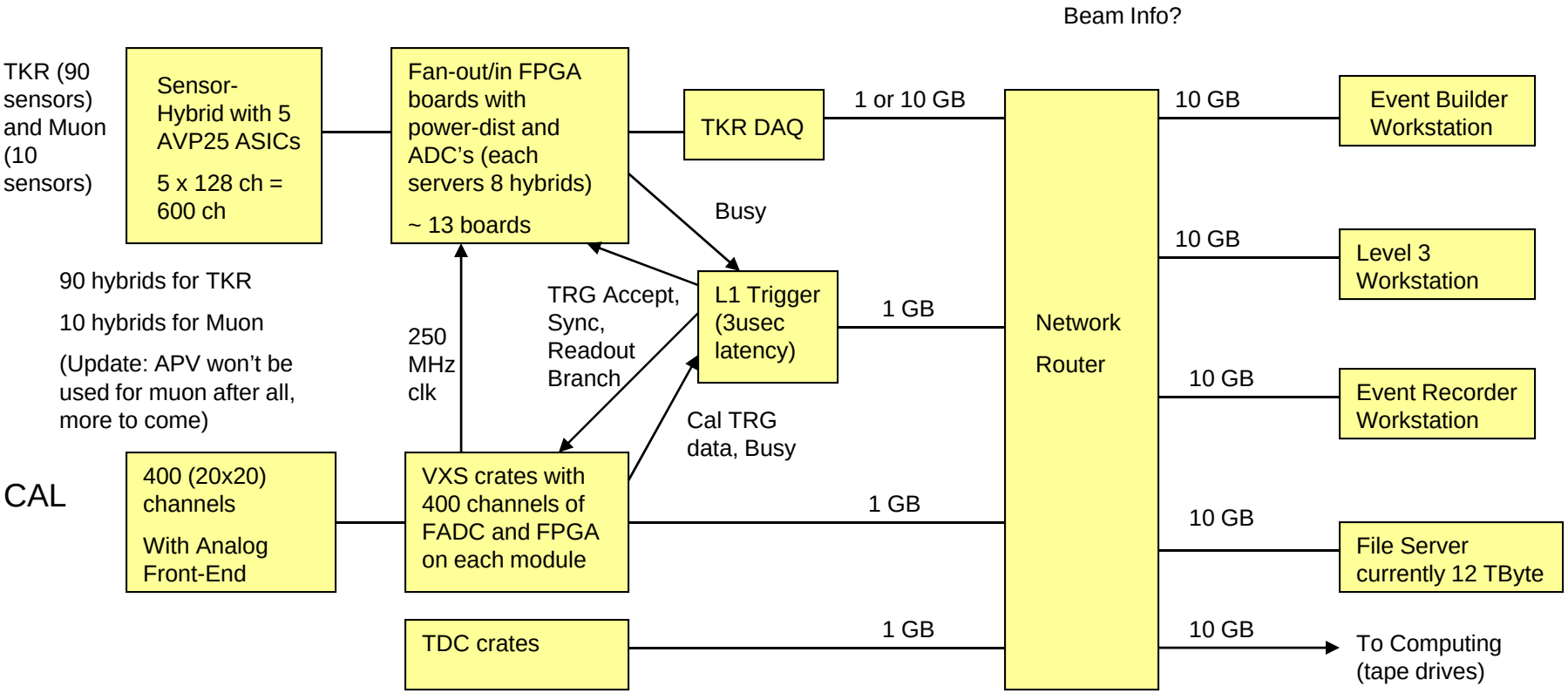
Top Level Block Diagram



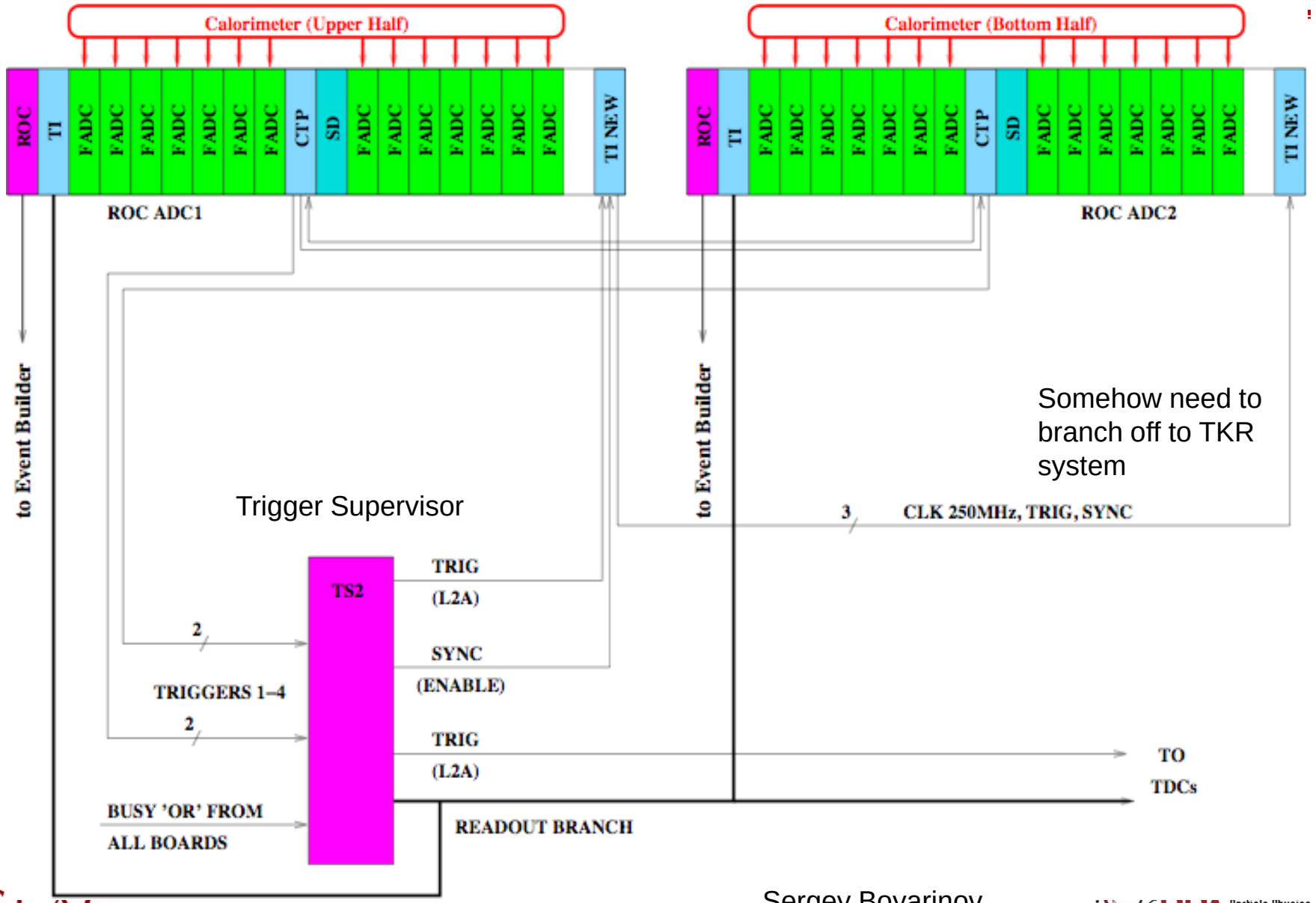
Calorimeter ADC & TDC & Trigger

* Sergey Boyarinov (JLAB)
  - > 400 channels of 12-bit 250 MHz Flash ADCs (planned)
  - > 400 channels of 85 psec resolution pipeline TDC's with discriminator (exist)
  - Trigger boards
* Can all be provided by JLAB
  - Question is timing, JLAB might only need production in 1 year or later, but we need it earlier
  - Question to JLAB electronics dep head whether there is any cost to our project or not (JLAB needs there anyways for other experiments, our project only need for 1 month)
    - Chris answered that maybe they can find funds to make a small production earlier (25 boards)
  - Assume preamps used for APD's can be used for our project (in process of investigating how amps can be removed from current system)

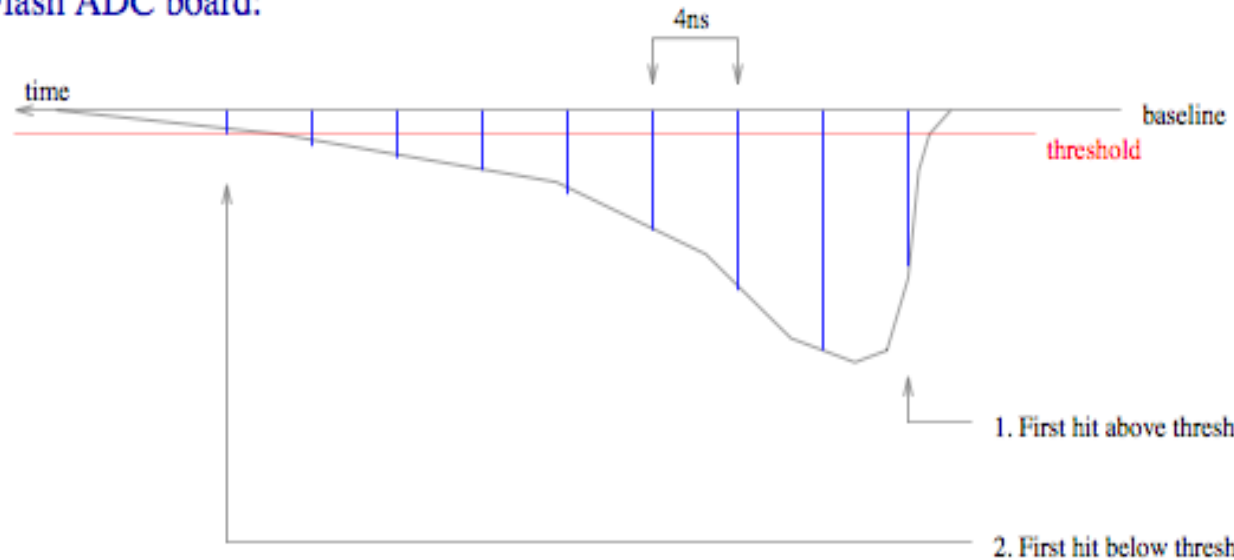
Calorimeter ADC & TDC & Trigger

* To be done:
  - Above boards to be fabricated/tested (time-scale). JLAB might be able to get small production of 25 boards but needs to find funding at JLAB for that
  - FPGA code for ADC's to be written for trigger (assume JLAB will provide)
    - Each one has 16 inputs, select hits above threshold, produces list of 8-bit ADC values, is transferred to next stage)
  - Trigger (Trig accept, sync, Readout Branch) needs to interface to TKR
    - Several options are under investigation, looks doable, like fiber split, etc
  - Also provides CLK, 250 MHz, need to decide how above system will provide CLK to TKR
    - Are there additional outputs which can be used for TKR?
    - Fiber fan-out?

Flash ADC and Trigger Subsystem (JLAB)



Flash ADC board:



1. First hit above threshold: start sum window, add previous hit to it

2. First hit below threshold: add that hit to the window, close window; we have now ADC value and WINDOW_SIZE

3. Wait DELAY ns and send ADC valie to the Cluster Finder board (DELAY = DELAY0 – WINDOW_SIZE, where DELAY0 is delay constant for all channels, order of 128ns; this way sending time will be related to the beginning of the window)

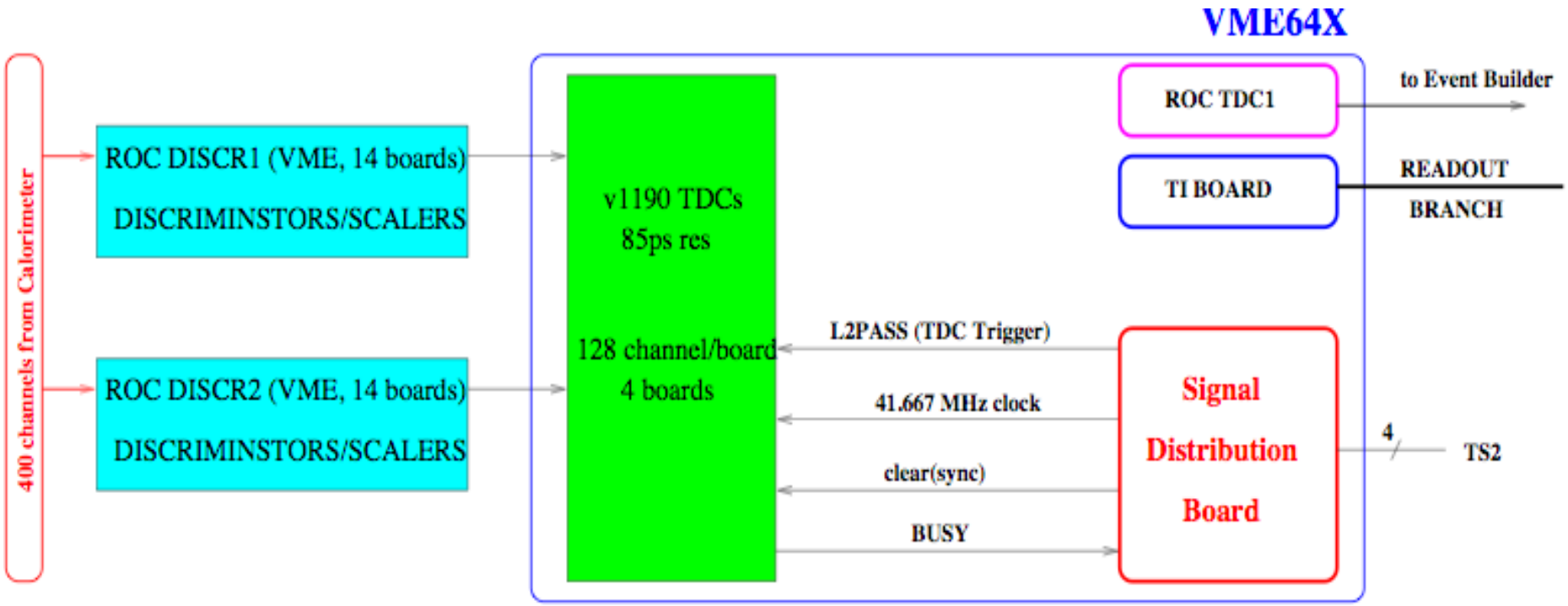
4. Based on bandwidth 8GBit/s we can send 8bits per channel every 16ns including channels without info, or 16bits per channel every 32ns including channels without info

Cluster Finder board:

1. Does not have information about original sum window width

2. Expands every window up to the value big enough to enforce coincidence between different channels

Pipeline TDC Subsystem (JLAB)



TKR Data rate and volume

* Number of channels
  - 500 x 128-ch ASICs = 64,000 channels

* Occupancy
  - If run at 3*noise threshold: from noise: 0.135% -> 86 channels over threshold
  - Each channel-over-threshold results in 6 digitized values: 556 samples
  - Hits: 10 x 2(strips) x2 (H&V) = 40 channels; x 6 samples = 240 samples
  - Total 126 hits x 6 samples = 756 samples for each trigger

* Amount of data for 40 MHz clock, 50 KHz rate (APV25)
  - Structure
    - Each chip 12-bit header (3 start, 8-bit address, 1 error) plus 10 bits/channel if 10-bit ADC is used
    - For each ASIC need additional 9 bit chip address
  - Number of bits for each hit
    - 9-bit chip address (16-bit)
    - 12-bit header (16-bit)
    - 6 times 10-bit ADC value (72-bit) (assume 10-bit ADC for now since need bare minimum 8 bits)
    - 13 bytes (104 bits) (81 bit minimum)
  - Data volume and rate
    - 126 ASICs x 2 bytes chip address: 252 bytes
    - 126 hits x 2 bytes header: 252 bytes
    - 126 hits x 6 samples x 1.5 bytes: 1,134 bytes
    - 1,638 bytes x 50 KHz = 81.9 Mbytes/sec
  - Raw storage
    - For 1 month running: 30x24x3600x81 Mbytes/s -> 210 Terra-bytes.
    - $500 / Terabyte
    - Store all (no L3) is $105,000
    - Data rate into storage is 150 MB/sec per node (scales with nodes)
    - if one allocates $20k for storage, that is 40 Terabytes, need 45:1 reduction in L3 processing
    - Increase of reduction from 5 to factor of 100 saves max $20k
  - Alternate
    - Calculate time and pulse height for each hit
    - 126 ASICs x 2 bytes chip address: 252 bytes
    - 126 hits x 2 bytes header: 252 bytes
    - 126 hits x 3 ?? bytes time/amplitude 378 bytes
    - 882 bytes x 50 KHz = 44 Mbytes/sec
    - Factor of 2 less than above?

Backend IO for each ASIC

* Common
  - Diff: trig, clk
  - Single-ended input: Rst , sdain, sclk,
* Each ASIC
  - Single-ended output: oute, sdout, muxout
  - Diff output: anaout
* Power
  - About 5 sets of + and – 1.25V (check what can be bussed)
* Lets assume to each hybrid 5 ASICs (which would require 100 hybrids)
  - 7 common input lines
  - 3 outputs if logic on hybrid?
  - A few power lines if filtering on hybrid

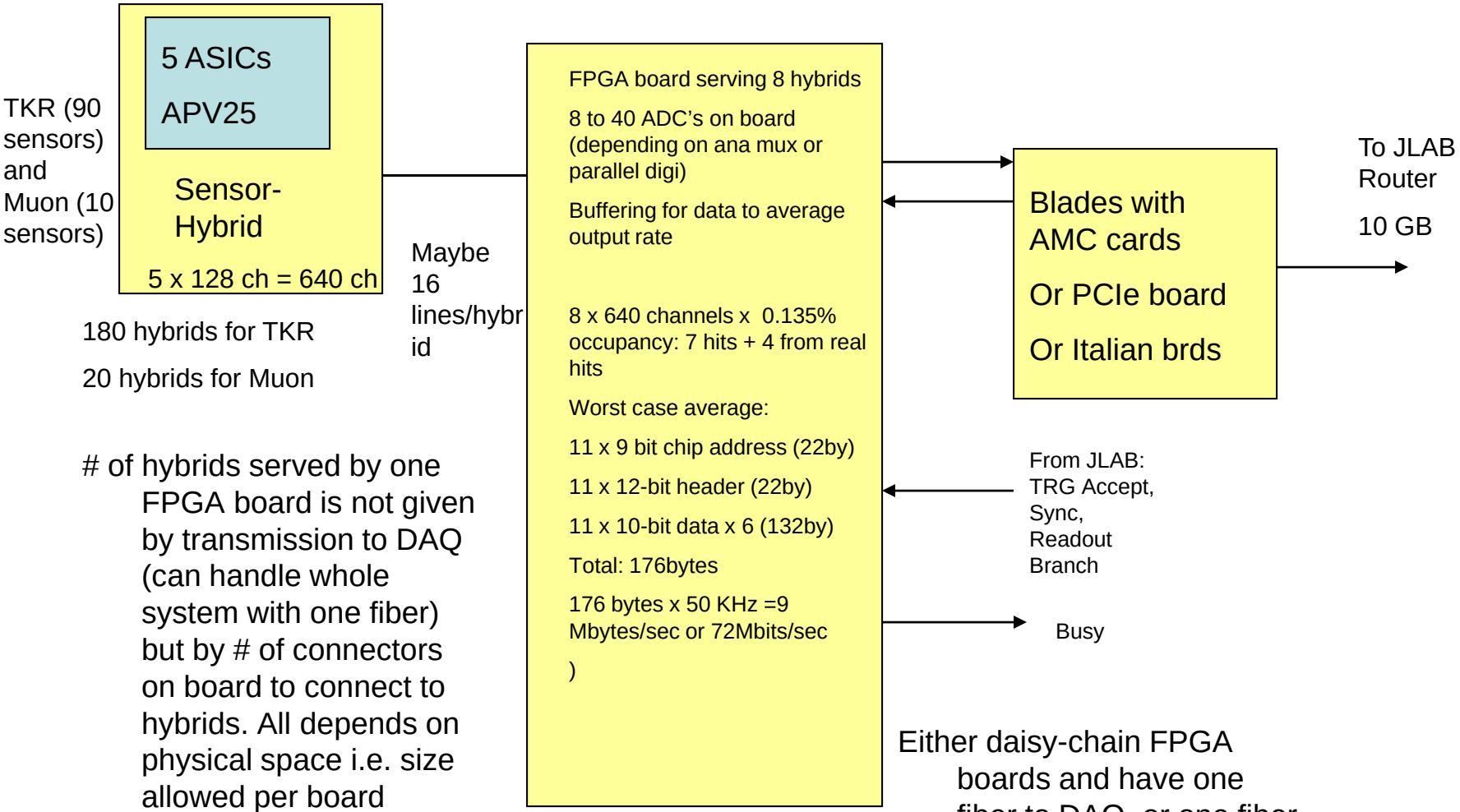
Hybrid locations/partitioning

* From Tim: At the moment, we are planning five measurement stations along the beamline. Each of these stations measures a combination of three different views: x, y and s, where x-y are an orthogonal pair and s is small-angle stereo. Some stations may measure only one of these, while others may possibly measure three. However, there are major advantages (mechanically) in having a measurement pair at each station. So... for the moment... let's assume that.
*
* Because the lateral coverage needed in each layer depends upon the depth in the tracker, the first layers can be smaller without sacrificing acceptance. So, in each layer, the number of sensors in the two views of the five stations would be:
*
* 4+6 = 10 sensors/hybrids = 6400 channels
* 8+8 = 16 sensors/hybrids = 10240 channels
* 10+12 = 22 sensors/hybrids = 14080 channels
* 10+12 = 22 sensors/hybrids = 14080 channels
* 10+12 = 22 sensors/hybrids = 14080 channels
* ==========
* = 92 sensors/hybrids = 58880 channels (and 460 chips total)

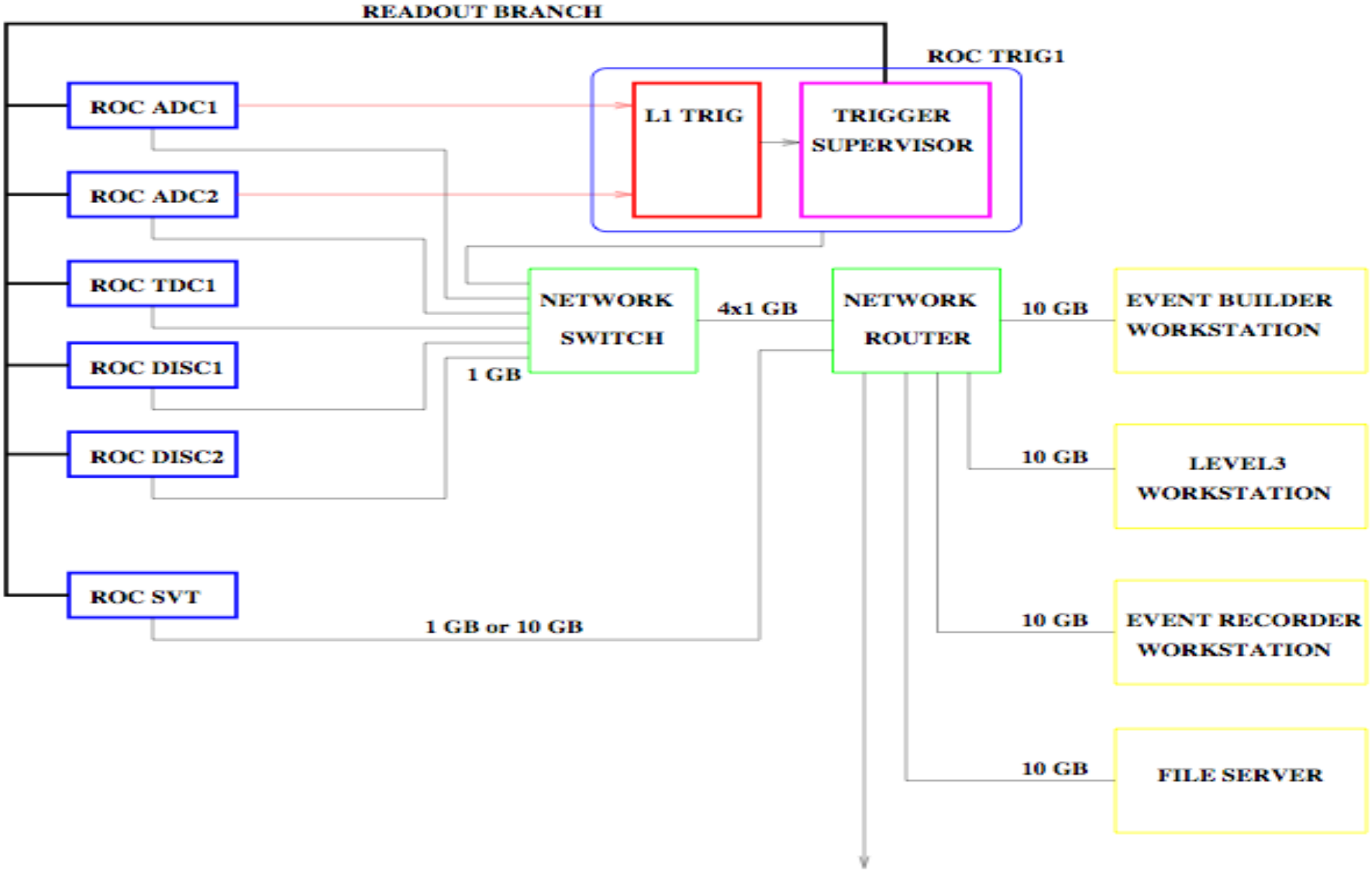
* About 20 cm in between stations

* # of FPGA boards assuming one FPGA board serves 8 hybrids
  - 2
  - 2
  - 3
  - 3
  - 3
  - Total of 13 boards

Block Diagram



DAQ (JLAB, Sergey)



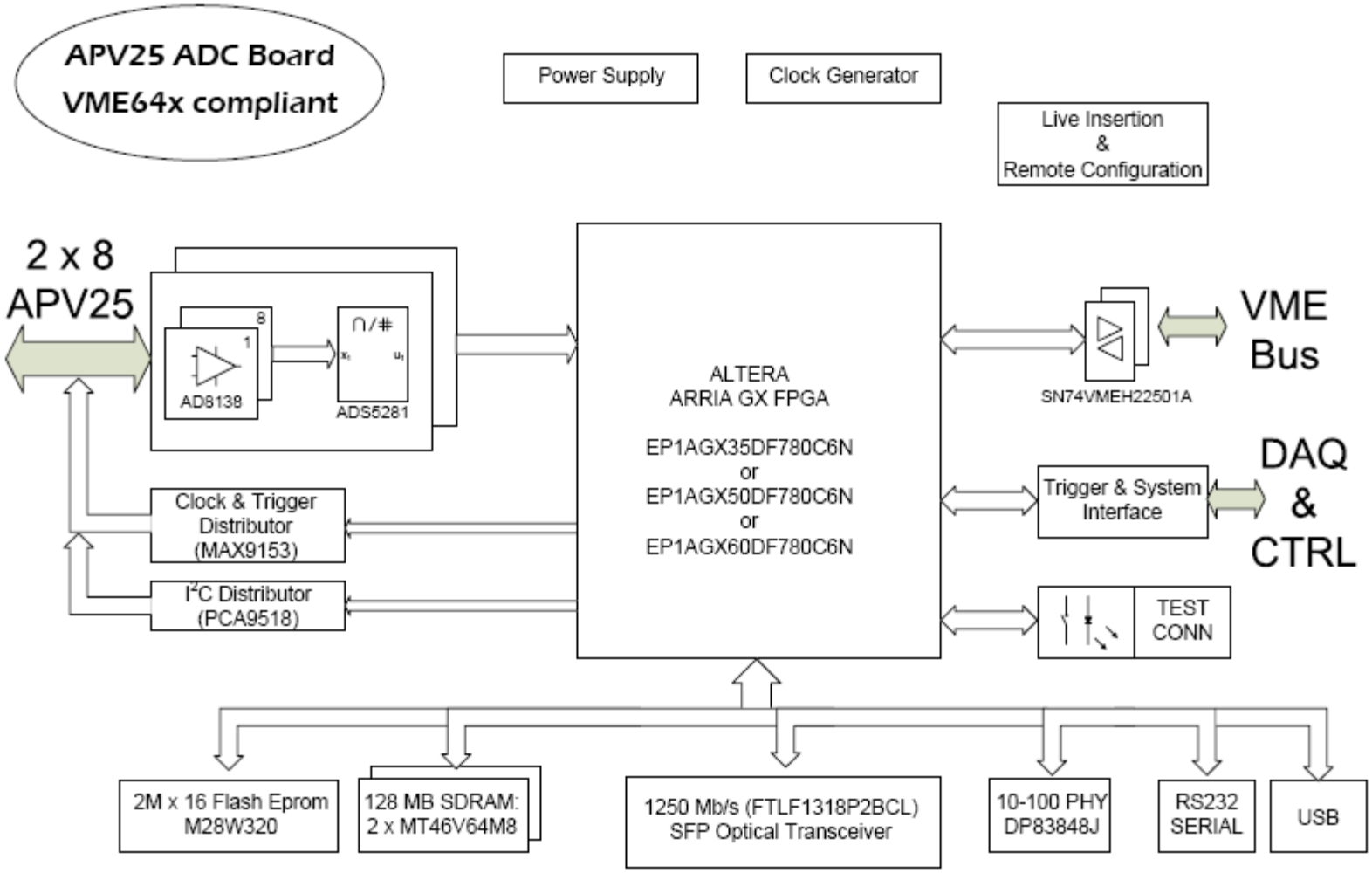
Notes

* Determine how TKR gets trigger signals, sync, readout branch, and how to send Busy back to JLAB system
  - SLAC could use TI (trigger Interface) board from JLAB, but would need to be in VXS, VME, or PCI format
  - Or SLAC could use trigger branch signals directly
  - Sergey will get SLAC TI code
  - Not a show-stopper but needs to be figured out
* Might be able to use another PCI card (DLINK plus daugtherboards for ALICE) to interface to TKR FPGAs
  - SLAC will investigate, Sergey will send more info about above to SLAC.
  - They have 4 boards, 2 fiber IO's each
* Might be able to use Genova system in development
  - Paolo Musico/Evaristo Cisbani)
  - Have prototype board
  - System targeted to interface to JLAB DAQ

From Genova:

* We are developing a new VME64x module with VXS extension which can control/readout up to 16 APV25 chips.
* Chris gave us the hardware details to make it Jlab compatible.
* The module is essentially a 16 channels ADC (12 bit, 40 MHz) controlled by an ALTERA FPGA which can decode the APV serial data streams, store data in a local buffer and trasmit them to DAQ.
* The FPGA can be programmed to implement a variety of interfaces: VME, optical, ethernet, USB.
* We have received the first 2 prototypes a couple of weeks ago and now we are starting the bench testing.
* FPGA coding is in progress.

APV25 ADC board (Genova)



More from Genova

* We are planning to have a first revision working (on actual prototypes) before august to make a test beam. This should be a very preliminary code to be optimized in the near future.
* We still do not have details on data format as specified from Jlab: this will go in the optimization phase, after summer vacation.
* No plan for integration with software yet, although it should be relatively straightforward into the new official CODA system.
* We expect a trigger rate of 5 kHz and a corresponding event rate up to 100 MB/s.
* I try to propose a possible collaboration plan:
* - Once we have debugged our actual prototype we'll build a second version by September/October.
* - We can produce few additional pieces of the new board for you and provide also a "level 0" FPGA code.
* - Then we can go in parallel and find a way to collaborate in the FPGA optimization.
* The code core will be substantially the same, but perhaps some refinements can be different (i.e. baseline correction algorithm, data reduction, ...).
* - Once the hardware is well debugged we can provide you all the cards you
* need: you'll pay directly the firm for your batch

* Note from Gunther: we need to see how much work above is for SLAC to get familiar and get involved in a non-SLAC APV readout system versus implementing a PCI based system
  – Will be investigated over the next few weeks

Notes

* TKR
  - SLAC provides APV25 hybrids, cables to TKR FGPA boards, FPGA board, DAQ CPU
  - Need to make sure APV25 work at 41.666 MHz, (250 MHz/6 system clock)
* Power
  - Power supplies needed to connected to FPGA boards (power to APV25 is provided by FPGA boards)
  - Needs more discussions but not an issue
* Trigger only from CAL?
  - Or maybe add scintillator plates, small, maybe 4 to 12
* How is beam info transported?
  - Analog, digital, protocol?
* Muon system is being changed, more later

Notes (con't)

* CAL
  - Assume JLAB provides all calorimeter, trigger, and TDC boards for use by us, no cost to project (needs to be checked with Electronics head)
  - Assume JLAB takes care of CAL including
    - FADC FPGA trigger VHDL
    - CTP FLGA code
    - List of cluster code running in Level 3 workstation
    - Again needs to be confirmed what he costing model is if any

Notes

* DAQ
  - JLAB provides complete system (shown in earlier slide)
  - Use JLAB CODA DAQ software
  - For configuration, readout SLAC provides command list, data format, etc. (Transport is Ethernet)
  - JLAB woul d need to add GUI's in their system to interface to TKR
  - JLAB provides List of clusters for CAL ((Level 3 work station)
  - Question whether TKR data reduction takes place
    - in TKR DAQ crate (track finding)
    - Or send all data (640 Mbit/sec) to Level 3 workstation and process there
      - Probably better solution
      - Also have CAL data available
      - Question whether workstation is powerful enough, but worst case can buy more powerful server
  - DAQ stops every e.g. 1000 events and makes sure everybody is in sync. If not send Sync signal

Notes (con't)

* Input to Level 3 workstation
  - From TKR: 80 Mbytes/s plus margin
* Output of Level 3 workstation to tape
  - < 50 Mbytes/sec
* Need reduction in Level 3 filter by factor of 4 at least?
* Best to filter as little as possible since don't have much time optimizing or checking filter performance
  - Have several filters available and when know real data-rate make as loose as possible while still sending < 50 Mbytes/sec to tape

Notes (con't)

* Trigger only from CAL?
  – Or maybe add scintillator plates, small, maybe 4 to 12
* How is beam info transported?
  – Analog, digital, protocol?

Items (may change in case of JLAB system)

* Software
  - Configuration (Front-end ASICs)
  - Calibration * Analysis
  - L1 trigger configuration (possibly just enable map for front-end OR in CAL)
  - L3 filter to reduce data amount
  - Online event –data quallity monitoring
  - User Interface, GUI for above
* Power supply and distribution
  - Distribution/monitoring via FPGA board
  - Use bench supplies for power
* Minimal T/V/I monitoring (tbd)