Heavy Photon Search
Electronics, DAQ, & Software

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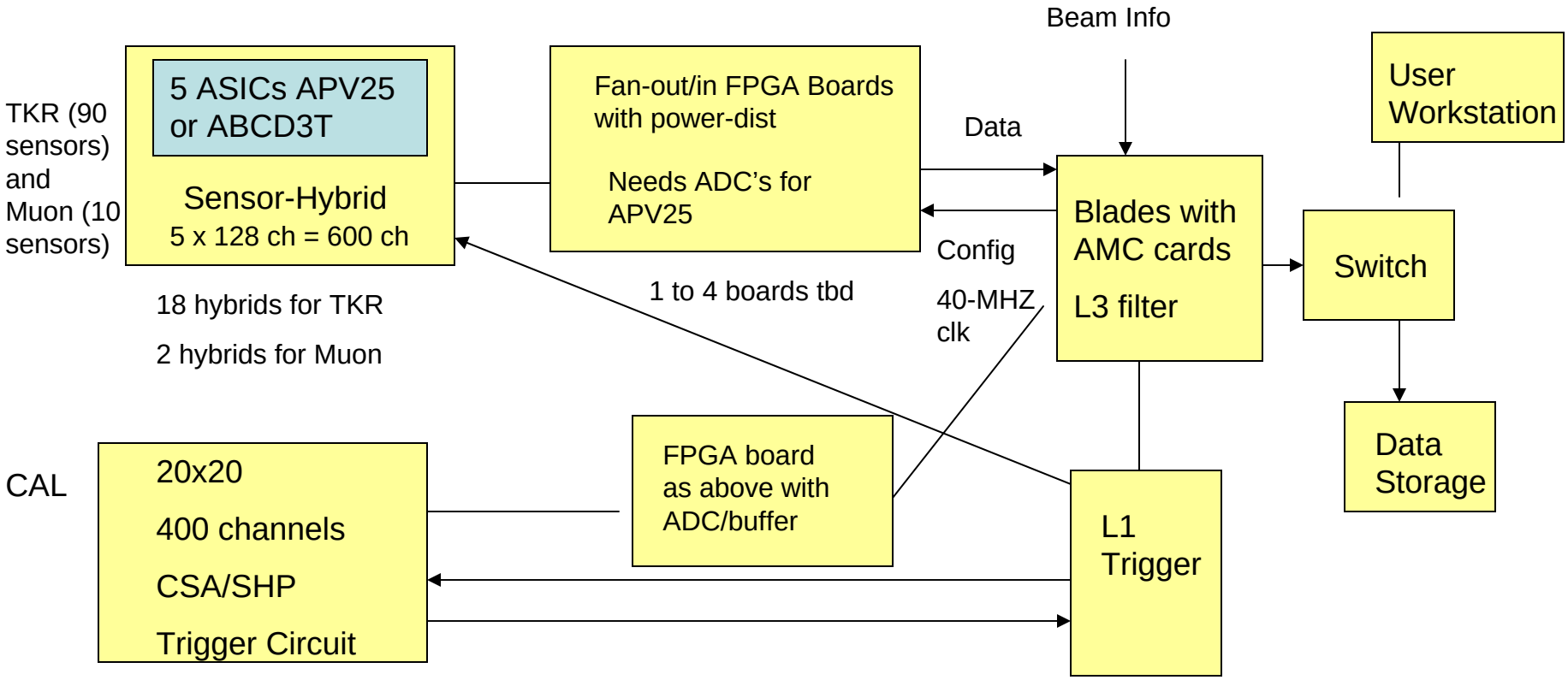
SLAC PPA REG-E

January 7, 2010

Block Diagram



Items

* Control and Timing system
  - Same blades as used for DAQ
* Software
  - Configuration (Front-end ASICs)
  - Calibration * Analysis
  - L1 trigger configuration (possibly just enable map for front-end OR in CAL)
  - L3 filter to reduce data amount
  - Online event –data quallity monitoring
  - User Interface, GUI for above
* Power supply and distribution
  - Distribution/monitoring via FPGA board
  - Use bench supplies for power
* Minimal T/V/I monitoring (tbd)

Processing versus Storage

* Number of channels
  - 500 x 128-ch ASICs = 64,000 channels
  - Occupancy: 3% -> 2,000 channels
* Amount of data for 40 MHz clock, 50 KHz rate
  - APV25
    - Each chip 12-bit header plus n bits/channel
    - 7 bits for channel encoding
    - N depends on ADC used
    - If 8 bit ADC then total of 2 bytes/channel hit
    - For each ASIC need additional 9 bit address
    - Total is about 4 bytes/chip overhead plus 2 bytes/channel hit
    - 2,000 channels -> 4 Kbytes, ~times two overhead -> 8 Kbytes
    - 8 kbytes at 50 KHz -> 400 Mbytes/sec
    - For 1 month running: 30x24x3600x400 Mbytes/s -> 400 Tera bytes
  - ABCD3T
    - Less than above but not even factor of 2, so choice of ASIC is not driven by DAQ/storage
* Cost
  - $500 / Terabyte
  - Store all (no L3) is $200,000
  - Data rate into storage is 150 MB/sec per node (scales with nodes)
  - if one allocates $20k for storage, that is 40 Terabytes, need 10:1 reduction in L3 processing
  - Increase of reduction from 10 to factor of 100 saves max $20k

More items

* CAL Dynamic Range?
  - If range from 1 to 6 GeV and want 1GeV to 5% -> only 8 bit required?
* Trigger only from CAL?
  - Or maybe add scintillator plates, small, maybe 4 to 12
* How is beam info transported?
  - Analog, digital, protocol?
* Boards do be designed
  - Strip-ASIC hybrid
  - FPGA board with ADC and power distribution (simple)
  - Trigger board (probably can use same FPGA board)
  - CAL board