Deciding Upon Readout Option for MaDPhoX

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MaDPhoX Tracking Meeting

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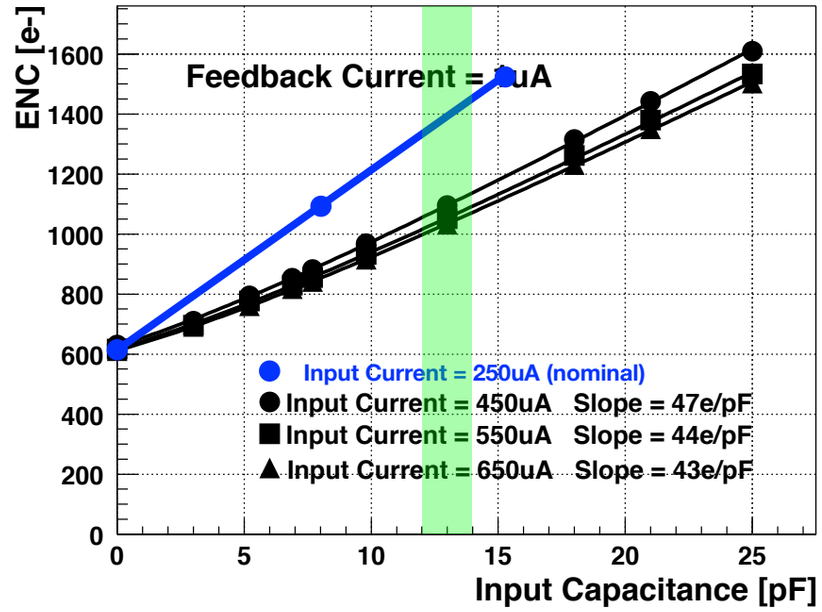
Comparing Readout Chips

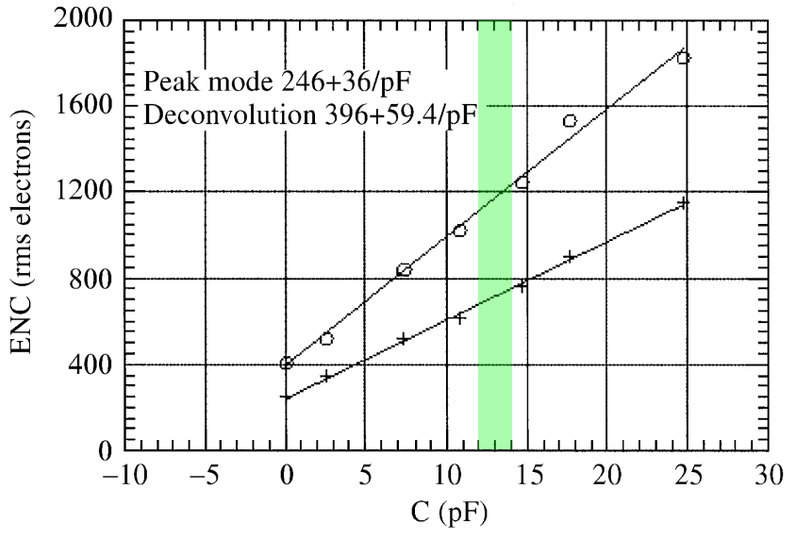
Before irradiation it is simple:

- noise characteristics of chips
- digital vs. analog readout

ABCD3TA

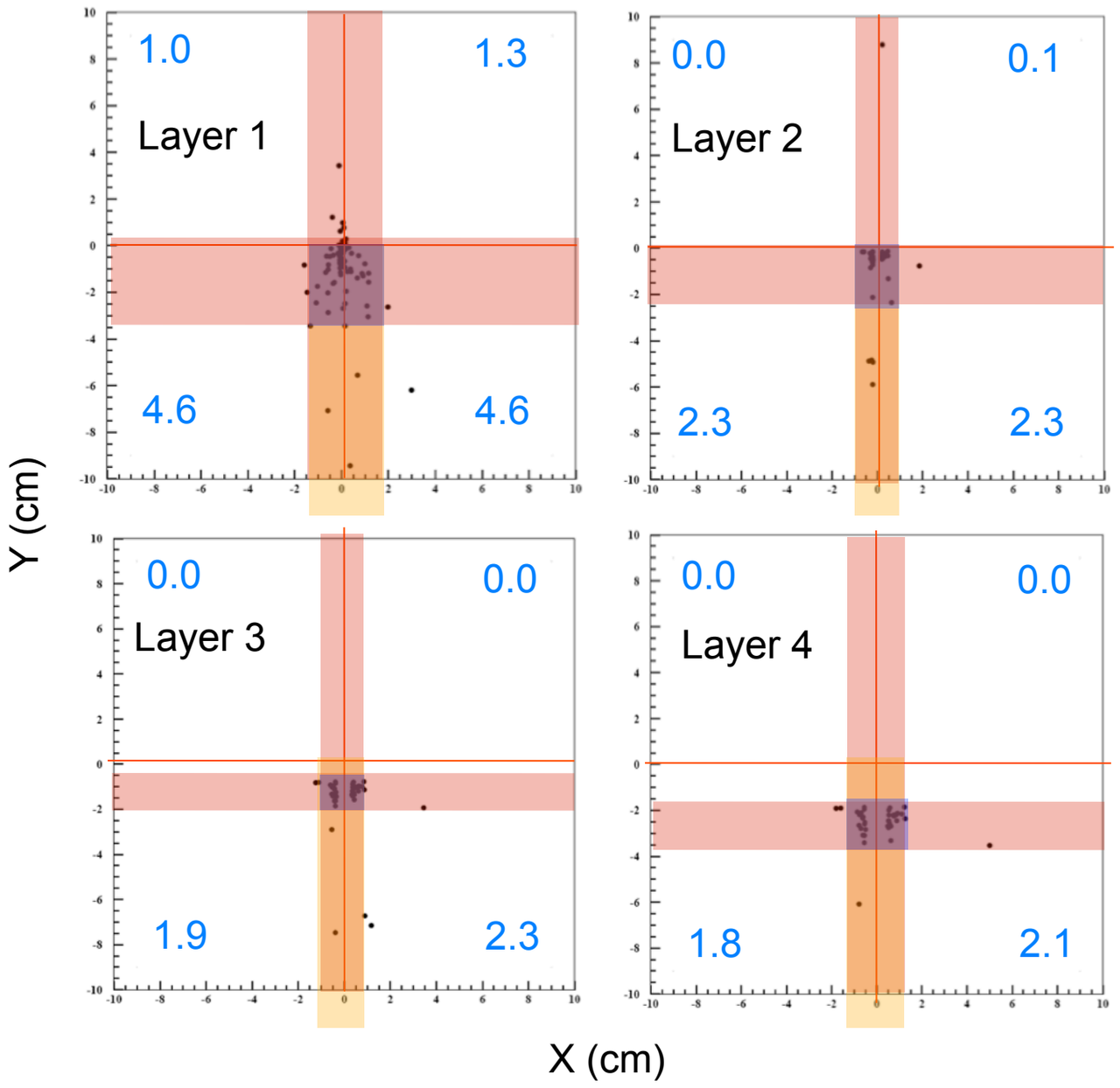


APV25



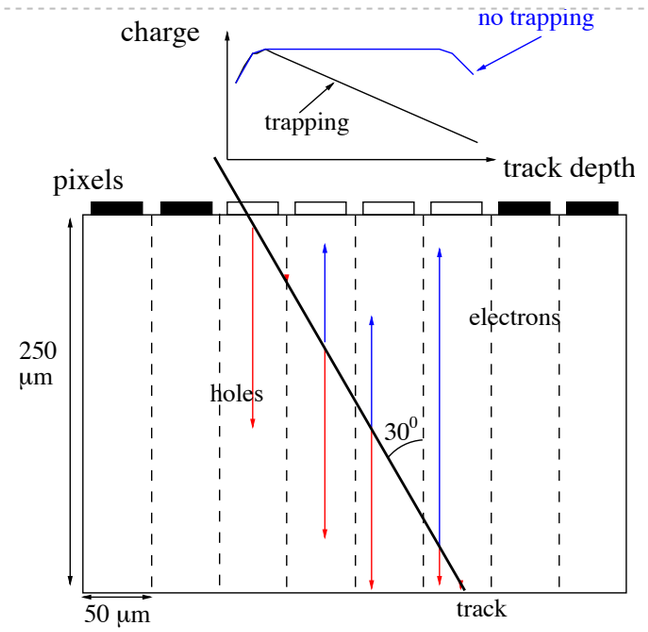
Performance after Irradiation

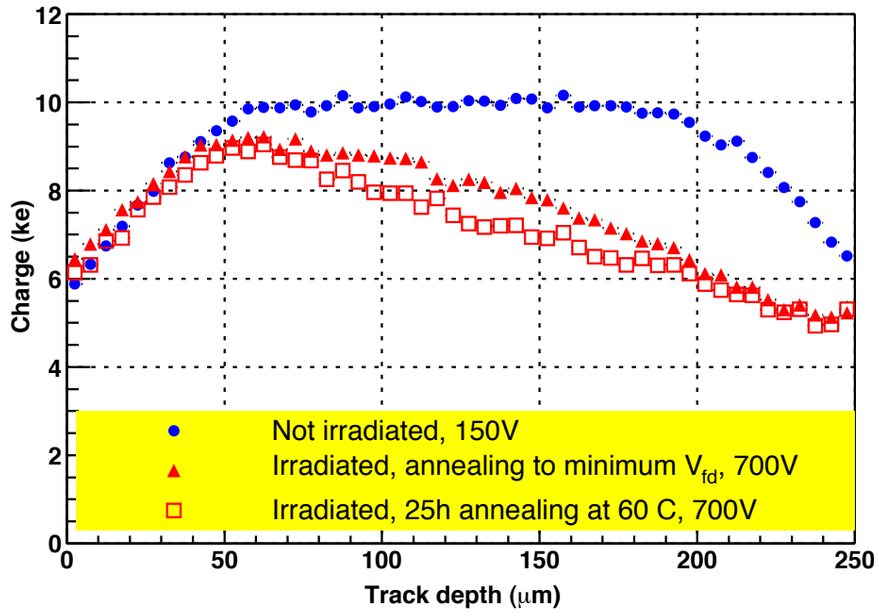
- Silicon damage is the primary concern
  - Some effects are local and impact only part of a strip, others impact the entire strip
- Some readout chips may receive significant radiation doses



Radiation Effects in Silicon

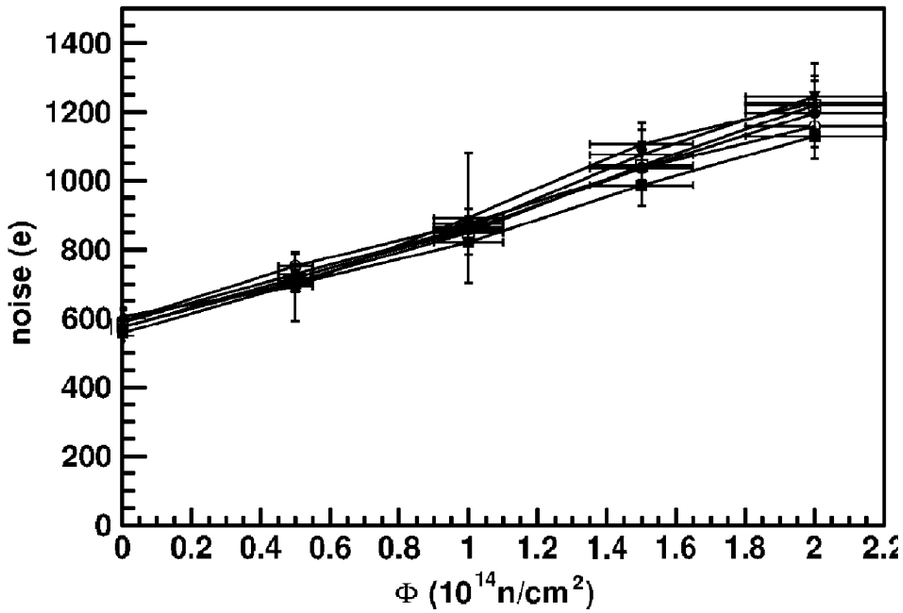
- Increased interstrip capacitance
  - before: 1.2 pf/cm
  - @2E14 NEQ: 1.6 pf/cm (looking for 1E15)
- Trapping decreases charge collection
  - before: no charge loss
  - @1E15 NEQ: ~20% loss per 100um drift
- Charge loss from underdepletion
  - before: fully depleted
  - after: covered in detail in previous talk.

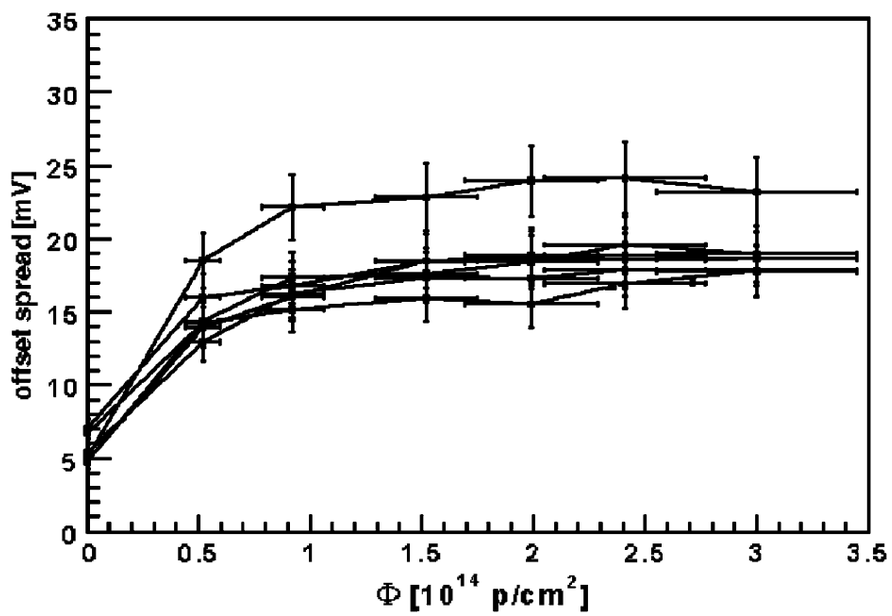




Radiation Effects in Readout Chip

- ABCD (0.8 um DMILL)
  - Increase in noise:
    - before: 600+65C e- ENC
    - @2E14: 1100+65 e- ENC
  - Increase in pedestal fluctuations (can be periodically trimmed out)
    - before: ~700 e-
    - >5E13: ~1500 e-
- APV25 (0.25 um CMOS)
  - no significant degradation





Simulation

Changes to org.lcsim

- New readout chip BasicReadoutChip
  - thresholds as multiples of RMS noise: easy to simulate optimized readout
  - simulates generic ADC via two settable parameters:
    - nbits (number of bits resolution)
    - dynamic_range (in fC)
  - binary readout (1 bit) is handled as a special case
- Change to CDFSiSim to simulate charge trapping
  - Can set fraction of charge loss per 100 microns drift
  - Depth dependent trapping is fully simulated

Suggested Test Points

- Before irradiation
  - Silicon: 1.2 pf/cm, full charge collection
  - ABCD3TA: 600+65*C e- ENC
  - APV25: 400+60*C e- ENC (deconvolution mode)
- Irradiated silicon @1E15 NEQ, fully depleted
  - Silicon: 1.6 pf/cm, 20% / 100um drift charge trapping
  - ABCD3TA: 600+65*C e- ENC
  - APV25: 400+60*C e- ENC (deconvolution mode)
- Irradiated silicon @1E15 NEQ, fully depleted, irradiated chip @2E14
  - Silicon: 1.6 pf/cm, 20% / 100um drift charge trapping
  - ABCD3TA: 1100+65*C e- ENC
  - APV25: 400+60*C e- ENC (deconvolution mode)

Summary

- By testing a few cases we can get an idea where we stand.
- The code is there. The amount of new code is very small so I don't believe there will be a long debugging cycle.
- Once we have checked these scenarios, we can decide how hard we need to look at these issues.
- Beyond these, we should probably look at what happens with thinner silicon.
- I will be in touch with Matt to get him up and running.