Effects at chip boundaries Mark Raymond – 24/6/08

In certain circumstances excess noise has been observed at chip boundaries, where one sensor channel is read out by one chip and the neighbour is read out by another. This note is an attempt to explore a possible origin of this behaviour.

The schematic shows a simple model of the sensor capacitance network connected to the charge preamplifier inputs in the boundary region between two chips. Only four channels of each chip are shown; the bottom four (1 -4) of chip1, and the top four (125-128) of chip 2.

The capacitors C_{BP} represent the sensor strip capacitance to the bias line V_{BIAS}, but these play no part in the effect to be described here.

The preamplifiers of each chip are shown referenced to a supply reference on the chip (gnd_1 for chip 1, gnd_2 for chip 2). In an ideal system these two voltages would be identical, but it is interesting to explore what happens if they are not, because this can give rise to behaviour similar to that which has been observed. Although I have called the preamp references **gnd**, this is somewhat arbitrary. For example in the APV the input FET sources connect to V125, so this would be the reference voltage.

The quiescent voltages at the preamplifier inputs (sometimes called virtual grounds – but actually DC levels) are at a fixed DC offset with respect to the supply reference level. For example if gnd_1 were to change by a voltage ΔV, then all the preamplifier input and output quiescent voltages would change by the same amount. The green waveforms in the schematic show the effect of a step change in gnd_1 on the input and outputs of the preamplifiers in chip 1, which will all show the same step change. For all the channels, with the exception of the edge channels, this is a common mode effect which can be removed.

For the edge channels the effect is different, but only if the preamplifier reference voltage of the neighbouring chip (gnd_2 for chip 2) does not see the same disturbance. If gnd_2 remains unchanged then the preamplifier input voltages V_{IN128}, V_{IN127}, V_{IN126}, ..., are also unchanged which leads to a transient current through the interstrip capacitance $C_{1\text{-}128}$ coupling the edge channels between the two chips. This current is represented by the red arrows in the figure.

For the polarity of the voltage step on gnd_1, the current will flow out of chip1/channel 1 into chip2/channel 128 and the outputs of the preamplifiers connected to those channel will show the step responses shown in blue; positive for chip 1, negative for chip 2. (Note that V_{O1} would also have a small contribution from the original disturbance on gnd_1, which is present on all the other channels on chip 1.)

This effect could only happen for edge channels. For channels within a chip the input voltages either side of the interstrip capacitance change by the same amount (in response to a change in the preamp reference voltage), so there is no current flow.

A typical value for the interstrip capacitance might be ~ 15 pF. A step voltage disturbance of just 1mV on gnd_1 with respect to gnd_2 would cause a positive charge injection of 15 fC into channel 128 of chip 2, and a correlated negative charge injection of -15 fC into channel 1 of chip 1. These are huge signals, but on the other hand gnd_1 and gnd_2 are connected together on the hybrid by a very low impedance (~ mΩ ?) so a difference of as much as 1 mV is unlikely.

To conclude at this point, I am starting to believe that the interstrip coupling described here probably gives rise to the observed effects. It is still not clear to me how the supply differences

between chips on the same hybrid can arise, but the magnitudes of the voltage differences need only be small to give rise to significant disturbances in these edge channels, because of the relatively large interstrip capacitances.