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NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

A novel technique for fast pulse-shaping using a slow amplifier at LHC

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We describe a new technique for front end signal processing for LHC type applications, where a shaping amplifier with a time constant of several beam crossing intervals is used. The method is based on discrete time filtering of data extracted from an analog pipeline after a first level trigger. A finite impulse response type filter deconvolutes the sampled voltages of the shaped pulse to retrieve the original impulse signal with high precision. Measurements showing the performance of the technique and its implication for signal to noise are presented. The method is well matched to CMOS front ends, where low power consumption and low noise is achieved for silicon strip readout by utilizing pulse shapes with time constants ~ 50 ns. A CMOS circuit emulating the filter has been built. It has been implemented with very low power consumption (< 0.1 mW) in a small silicon area to be utilized on every channel in the system.

1. Introduction

The detection of events generated in proton–proton collisions at the Large Hadron Collider will require the observation of interactions at intervals of 15 ns. It will be essential to identify the time origin of a signal with the precision of a single beam crossing interval. However it is extremely demanding, in terms of power consumption, to process signals from detectors with low noise using very short amplifier shaping times. In addition, pulse shapes employed in most amplifiers have tails which have durations several times longer than the rise time. These contribute to pileup so that the presence of a pulse height above a given threshold may not alone constitute evidence of a detected particle.

For the readout of silicon microstrip detectors for tracking applications at LHC, low power and low noise are major considerations. Detector systems will contain several million channels of densely packed readout electronics in quite small volumes and the heat dissipated creates serious problems for the mechanical design. Therefore it is of the utmost important to design an adequately low noise readout system with minimum power dissipation. A front end system based on a charge sensitive preamplifier and shaper to be implemented using CMOS technology is under study for LHC applications [1]. To achieve low power the shaping amplifier uses a relatively long shaping time of 45 ns. A novel technique is then used for processing the signals to achieve the aim of fast pulse shaping. This is referred to as deconvolution, since the operation performed is equivalent to retrieving the initial signal impulse from the shaped amplifier pulse. An important feature of its use is the fact that it relies on the regular sampling of amplifier output voltages at the beam crossing rate of the LHC machine (67 MHz). This introduces the possibility of applying techniques more familiar in digital signal processing applications.

2. The deconvolution method

In a linear amplifying system with an impulse response $h(t)$, the output $v(t)$ from an initial signal $s(t)$ can be written as a convolution integral:

$$v(t) = \int_{-\infty}^{t} h(t-t')s(t')\,\mathrm{d}t'.$$

In a system where the amplifier output voltage is

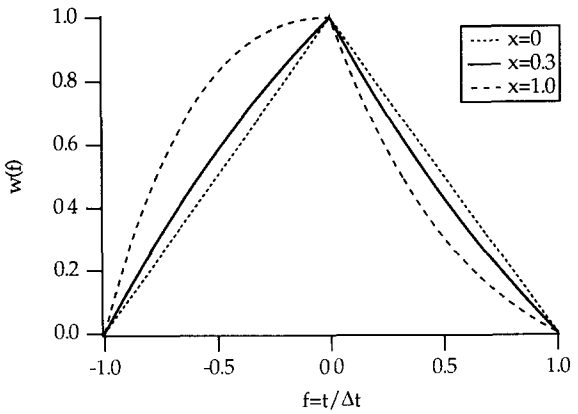

Fig. 1. the weighting function for the CR–RC shaper and deconvolution system.

sampled at regular intervals, so that the measurements of $v(t)$, for example, are $(v_1, v_2, v_3, v_4, v_5, \ldots)$, it is convenient to write the equation in a matrix form as

$$V_i = \sum_j H_{ij} S_j \quad \text{or} \quad \boldsymbol{V} = \boldsymbol{H} \cdot \boldsymbol{S}.$$

The original signal impulse can be recovered by performing the inverse operation

$$\boldsymbol{S} = \boldsymbol{W} \cdot \boldsymbol{V} = \boldsymbol{H}^{-1} \cdot \boldsymbol{H} \cdot \boldsymbol{S}$$

and the elements of the weight matrix $\boldsymbol{W}$ can be found by numerical matrix inversion of $\boldsymbol{H}$. It can be shown [2] that for the CR–RC filter which is commonly used in amplifier systems the equations above reduce to a particularly simple form. If the system response is described by

$$v(t) = e^1(t/\tau)\, e^{-t/\tau},$$

there are only three nonzero weights necessary and

$$s_k = w_1 v_k + w_2 v_{k-1} + w_3 v_{k-2},$$

with values

$$w_1 = e^{x-1}/x, \quad w_2 = -2\, e^{-1}/x, \quad w_3 = e^{-x-1}/x,$$

where $x = \Delta t/\tau$ and Δt is the sample interval. This means that a filter performing this operation can be constructed by forming the weighted sum of three consecutive voltage samples in time. The same result can be derived in another way using z-transform theory [3–5].

Estimates of noise in such a system can be made in a number of ways [2]. One method is to use the weighting function [6] which can be calculated by answering the question "What output is produced at

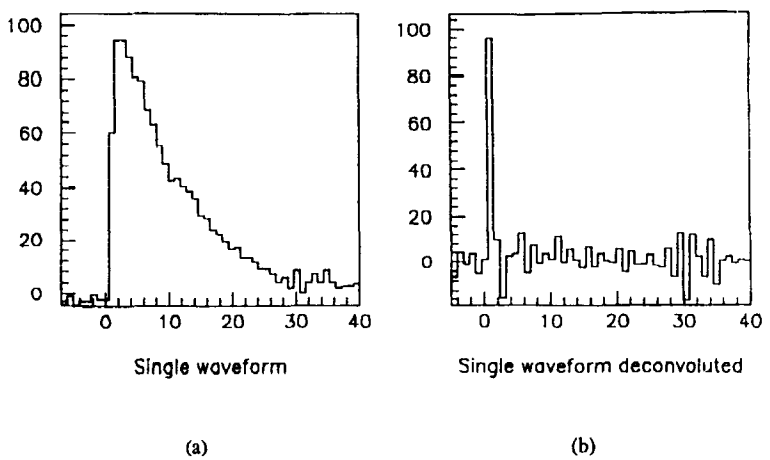

Fig. 2. (a) The measured impulse response of the CMOS amplifier. (b) The result of deconvoluting the signal measured in (a).

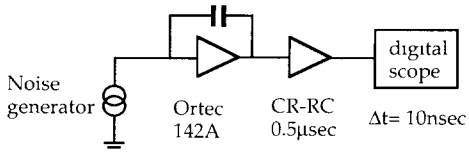

Fig. 3. The system used to verify the noise calculations.

some observation time T_m by an impulse which occurs at time t?" For the CR–RC pulse shape and the weighted sum above the weighting function can be written as

$$w(t) = \begin{cases} (1+f)\,e^{-fx}, & -1 < f < 0, \\ (1-f)\,e^{-fx}, & 0 < f < 1, \\ 0, & \text{elsewhere}, \end{cases}$$

where $f = t/\Delta t$ and t = arrival time of impulse with respect to the sample time. Thus $f > 0$ corresponds to an early impulse and $f < 0$ to a late impulse. $f = 0$ corresponds to an impulse coincident in time with the signal delta pulse being measured; as required, $w(0) = 1$. The function is plotted in fig. 1.

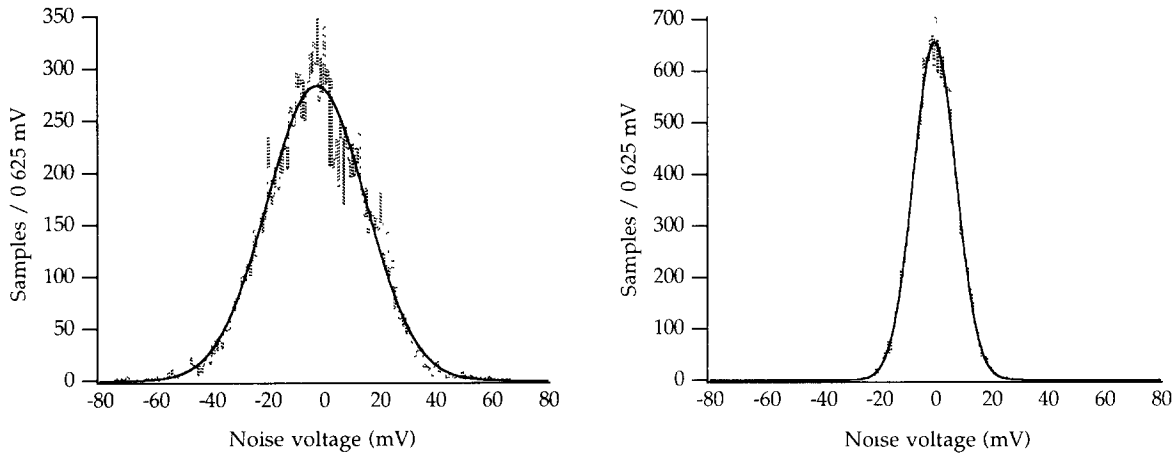

Fig. 4. Noise distributions before and after deconvolution.

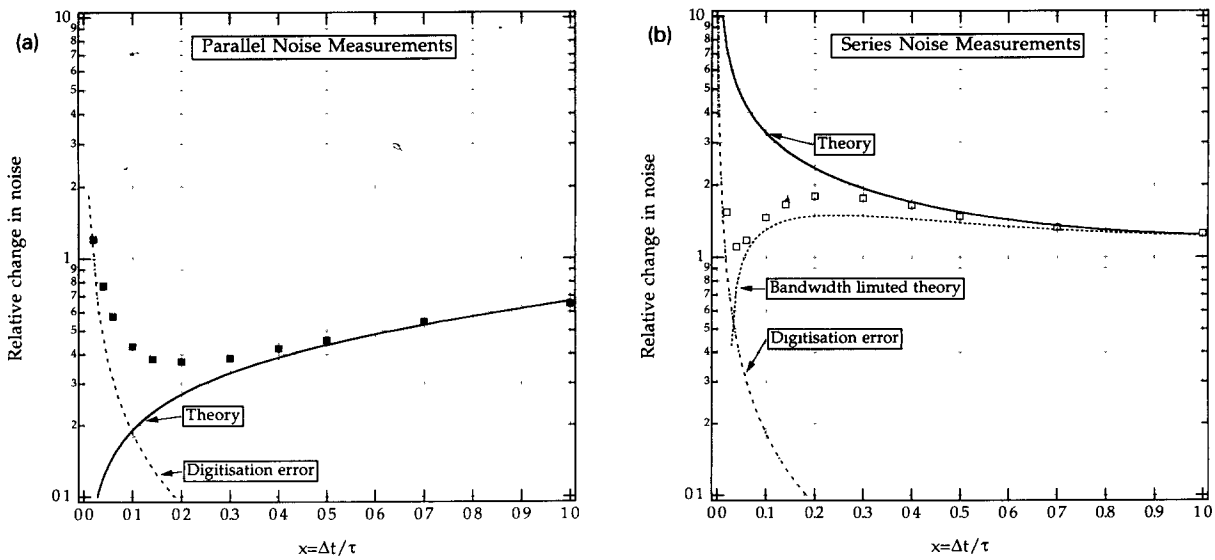

Fig. 5. (a) Parallel noise measurements compared with the theory. (b) Series noise measurements compared with the theory

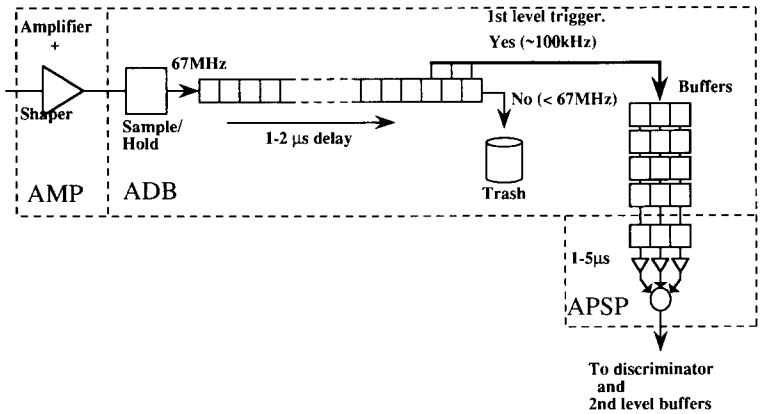

Fig. 6. A schematic diagram of the system proposed to implement the deconvolution method.

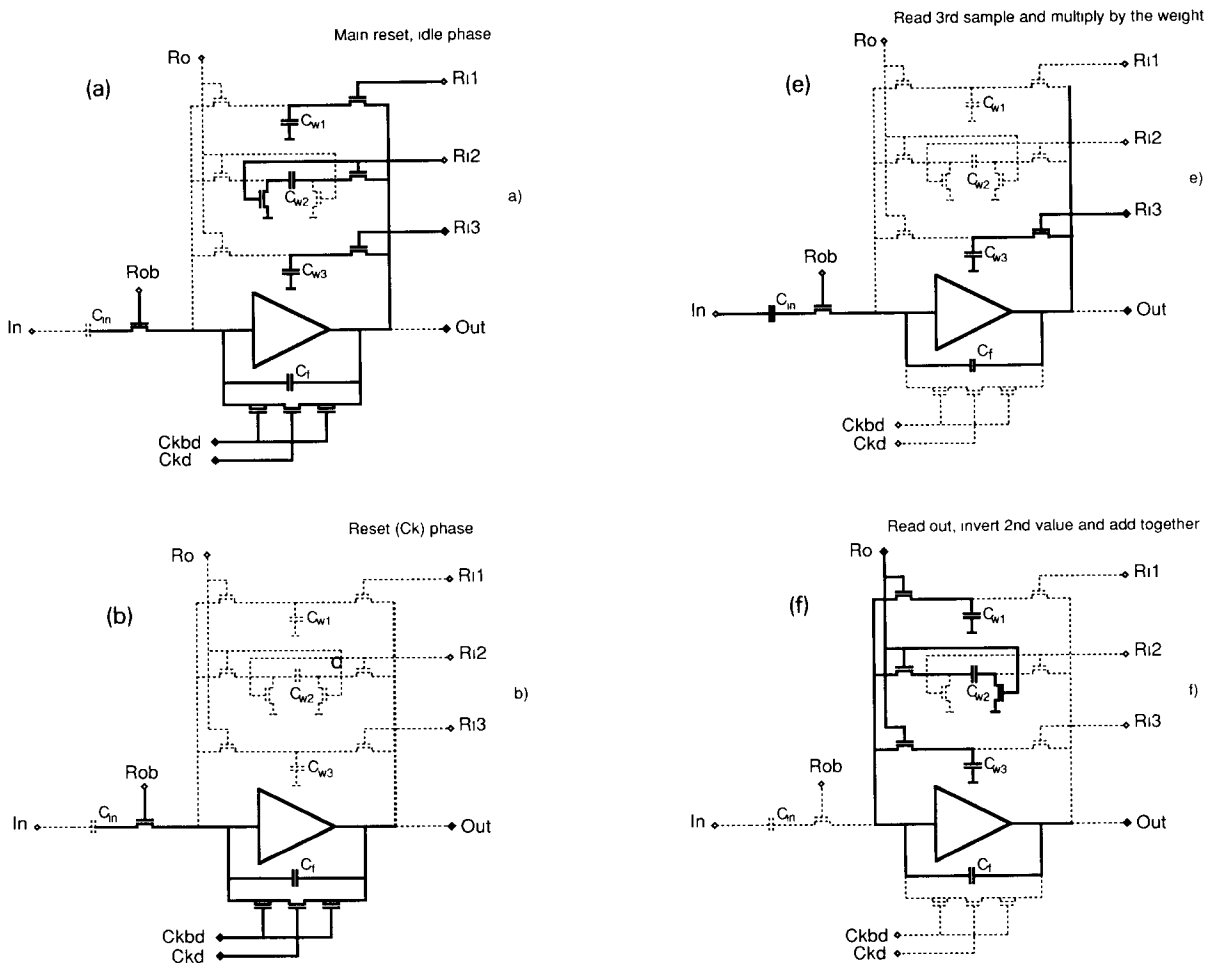

Fig. 7. The APSP circuit and the operating sequence.

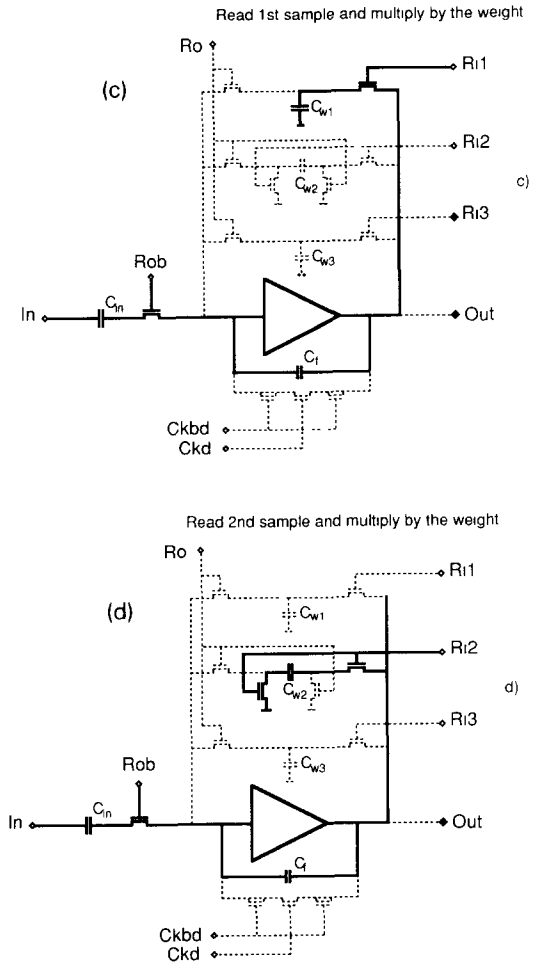

Fig. 7 (continued)

The noise in the system can be calculated by computing two integrals:

$\int_{-\infty}^{\infty} [w(t)]^2 \, dt$ for the parallel noise,

and

$\int_{-\infty}^{\infty} [w'(t)]^2 \, dt$ for the series noise.

The results are given in ref. [2], normalized to the same integrals for the CR–RC filter. They show that parallel noise is reduced following the filter and series noise is increased, as the operation is effectively equivalent to reshaping the output pulse with a shorter time constant.

3. Demonstration of the deconvolution method

Using an amplifier constructed as a prototype for silicon strip readout at LHC [1] we have verified the principle by digitizing output waveforms using a sampling oscilloscope. The amplifier is a CMOS circuit with a charge sensitive preamplifier and shaping filter closely approximating an CR–RC pulse shape with $\tau = 45$ ns. Fig. 2a shows the digitized output produced by a fast test pulse at the amplifier input and fig. 2b shows the consequence of forming a weighted sum of the samples using the weights calculated above for a value $x = 1/3$. This corresponds to the proposed ratio of sampling time ($\Delta t = 15$ ns) to τ.

It was considered of great importance to verify the general validity of the noise calculations [2]. To achieve this another charge sensitive amplifier (Ortec 142A) was used with a pulse shaping filter with a time constant of approximately 500 ns. The scheme is shown in fig. 3. Low value resistors were placed at the system input as a means of generating parallel noise in the system which would dominate over other noise sources. Data were digitized at intervals of 10 ns and transferred to an offline computer for analysis where they were processed by selecting samples at different intervals so that a wide range of x, 0.02–1, could be covered. The noise fluctuations were histogrammed and rms values extracted before and after the deconvolution operation (fig. 4) from a fit to a gaussian line shape. In a similar way data were also acquired using a large capacitor at the amplifier input to ensure that series noise dominated and the noise before and after deconvolution compared. The results are summarized in fig. 5.

To compare the calculations to measurements it is important to be aware of additional experimental factors which enter [7]. In a digital system quantization of the measured samples with the resolution of the ADC

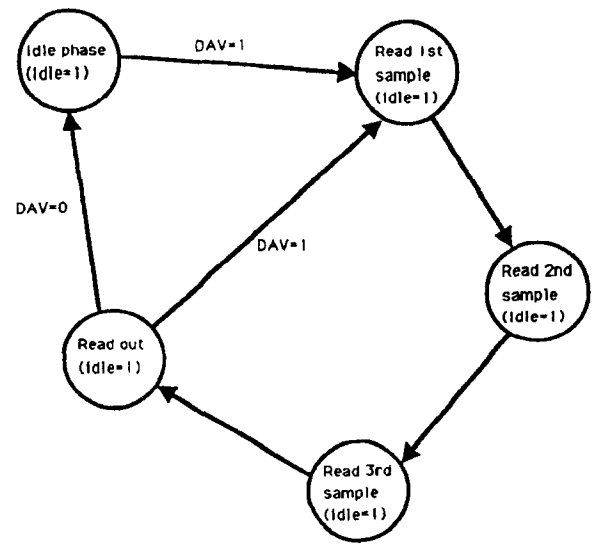

Fig. 8. A finite state flow chart of the APSP

(8 bits) occurs, which makes an additional contribution to the measured error. For measurements of series noise the bandwidth of the system, which is modified by the large input capacitance, needs to be taken into account since this increases the preamplifier rise time in a well-known way [8]. Once these effects are taken into account the data agree well with the calculations.

4. A brief system description

A system has been built which realizes the scheme. It is shown in fig. 6 and consists presently of three separate chips: the preamplifier with CR–RC shaper (AMP), an analog delay and buffer (ADB) and an FIR (finite impulse response) filter denoted as analog pulse

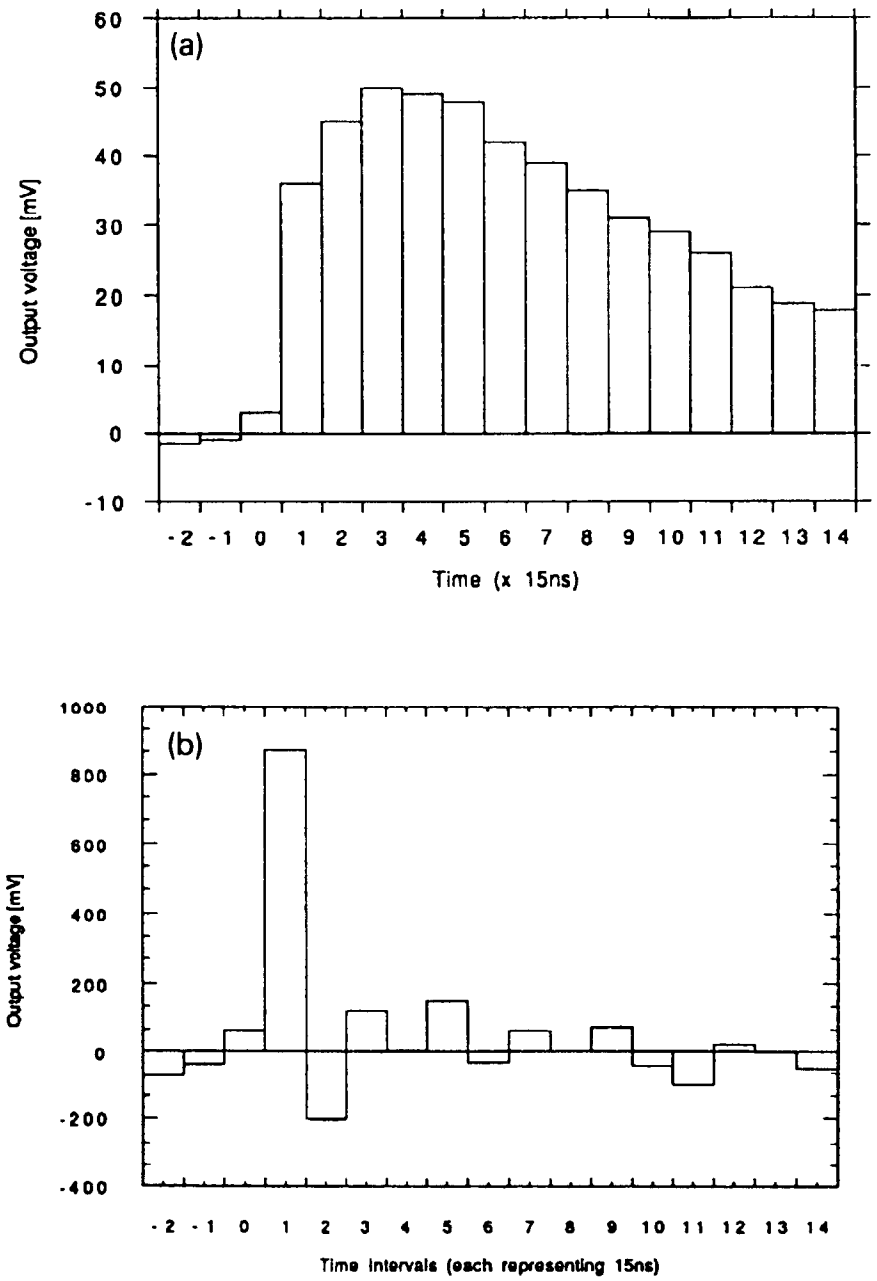

Fig. 9. Measurements on the APSP circuit: (a) shows the input sequence which is a measured output sweep from the CR–RC shaper; (b) shows the response of the APSP.

shape processor (APSP). The ADB is an analog pipeline running at 67 MHz and includes the digital logic necessary to control the flow of data to interface with the APSP.

The output of AMP is sampled every 15 ns. Each sample is stored exactly for the same time as the 1st level trigger delay. During the period in which no 1st level trigger occurs ("no"), which is more than 99% of the time, samples are discarded and overwritten by new samples. However, when a 1st level trigger does occur ("yes"), three samples are transferred to the APSP, which calculates the convolution sum. The average time between each positive 1st level trigger is expected to be ~ 10 μs. Consequently, if the APSP spends less time than this on each calculation, the system will be dead time free, providing buffers (which are included in the ADB) are provided to store data from 1st level triggers occurring close together.

Because the APSP only operates on data selected by the 1st level trigger the filter operation can be accomplished consuming very little power. This configuration is possible due to the fact that the impulse response of the deconvolution filter is finite and with only a small number of weights.

5. The APSP circuit

A CMOS circuit has been made to implement the FIR filter. Fig. 7 shows the analog circuit schematic and illustrates the method of operation. The clock runs continuously and has a duty cycle of $\sim 20\%$. When the circuit is idle or the clock is high, the indicated elements in (a) and (b) are reset. The operation is sequential and takes 4 clock periods.

The principle is simple. In the first clock period the

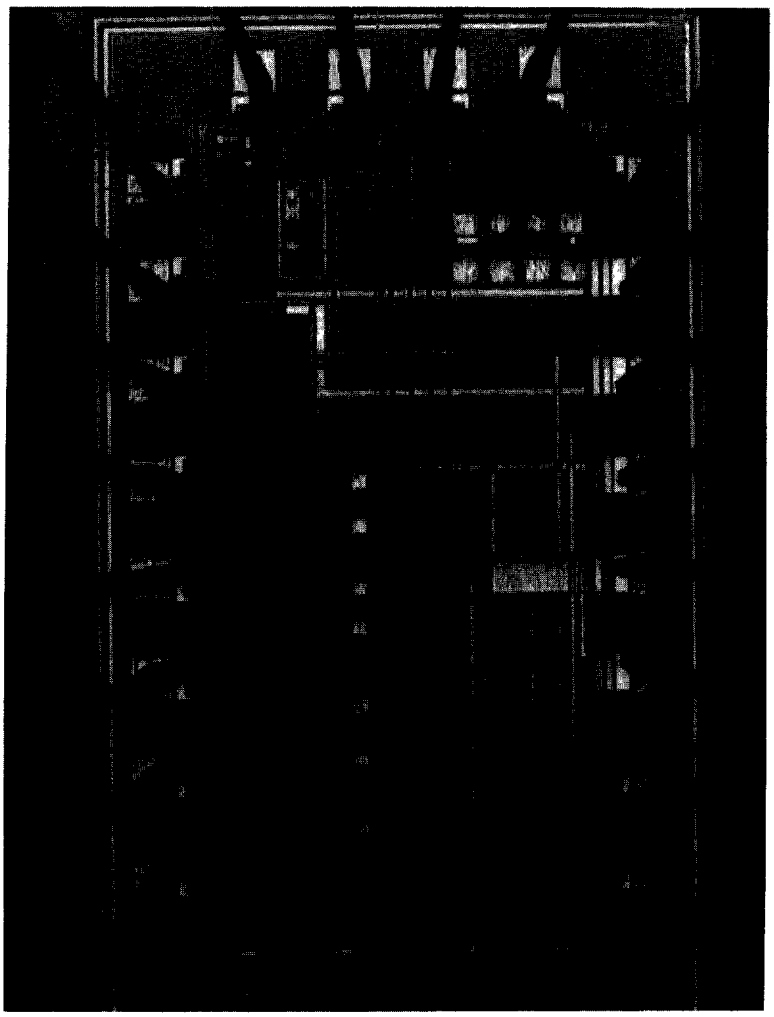

Fig. 10. A photograph of the prototype APSP chip

first analog value is read in, amplified by the ratio C_{in}/C_f and stored on the uppermost capacitor as shown in (c). In the next two periods the same happens with the two subsequent analog values except now the results are stored on the middle and lowermost capacitors, respectively, as shown in (d) and (e). In the fourth clock period the charges from the three capacitors are added together and integrated on the feedback capacitor and the final results appears on the output. In this scheme, the size of the storage capacitors controls the magnitude of the weight and the flipping of the middle capacitor accomplishes the change of polarity.

A digital control circuit has been put on the chip to generate all the necessary clock signals and to communicate with the ADB from which the input data comes. The latter is accomplished by the DAV and IDLE signals. The data available (DAV) signal is generated by the ADB immediately after a 1st level trigger and remains until all the required samples from this event have been read out. If new events appear during the readout of a previous event, DAV will remain until the samples from these are read out. The IDLE signal is generated by the APSP and its main purpose is to make sure that the readout of the ADB is fully synchronized with the read-in of the APSP. The circuit is implemented as a classical finite state machine and the control flow chart is shown in fig. 8.

In fig. 9 a measured output sequence of the circuit is shown for an input signal observed using the amplifier described above. The circuit accomplishes satisfactorily the required function of the FIR filter. The clock frequency used in the measurements was 1 MHz, and the total power consumption for the circuit is less than 100 μW. A chip photograph is shown in fig. 10.

Acknowledgements

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