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Nuclear Instruments and Methods in Physics Research A 466 (2001) 359–365

**NUCLEAR  
INSTRUMENTS  
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RESEARCH**  
Section A

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# Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker

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## Abstract

The APV25 is a 128-channel analogue pipeline chip for the readout of silicon microstrip detectors in the CMS tracker at the LHC. Each channel comprises a low noise amplifier, a 192-cell analogue pipeline and a deconvolution readout circuit. Output data are transmitted on a single differential current output via an analogue multiplexer. The chip is fabricated in a standard 0.25  $\mu\text{m}$  CMOS process to take advantage of the radiation tolerance, lower noise and power, and high circuit density. Experimental characterisation of this circuit shows full functionality and good performance both in pre- and post-irradiation (20 Mrad) conditions. The measured noise is significantly reduced compared to earlier APV versions. A description of the design and results from measurements prior to irradiation are presented. © 2001 Elsevier Science B.V. All rights reserved.

PACS: 85.40.e; 81.40.X; 29.40.G

Keywords: Deep submicron; Low noise; CMOS; Front end; CMS; Tracker; LHC

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## 1. Introduction

Recently, the CMS experiment at the CERN Large Hadron Collider (LHC) decided in favour of an ‘all-silicon’ solution for the tracker [1]. While the internal part consists of two layers of pixel detectors, the remainder of the tracker will be

made of silicon microstrip detectors. The total area of the tracker is about 230 m<sup>2</sup> for a total of about 10<sup>7</sup> readout channels.

Several years ago, the CMS tracker adopted a readout architecture based on the deconvolution method [2] for all-analogue readout. Based on these guidelines, the APV (Analogue Pipeline Voltage mode) integrated circuits were developed in qualified radiation-hard technologies: the APV6 [3] in Harris 1.2  $\mu\text{m}$  AVLSIRA process and the APVD-DC [4] in Temic 0.8  $\mu\text{m}$  DMILL process.

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These technologies use special processes which reduce the effects of radiation on the circuits.

The scaling of standard technologies towards deep submicron technology (Minimum Feature Size MFS smaller than  $0.5\ \mu\text{m}$ ) is beneficial to the radiation resistance of MOS transistors. With the oxide thickness being only a few nanometres, tunneling through the oxide can occur, causing a self-annealing of radiation-induced defects in the oxide. The threshold shift, one of the most important parameters which characterise radiation effects, decreases faster than expected by simple calculations which do not take into account tunnelling. For standard CMOS technologies with MFS of  $0.25\ \mu\text{m}$ , the threshold shift has been measured to be as low as a few tens mV after 30 Mrad of irradiation [5]. Another major effect affecting the performance of CMOS circuits under irradiation is the creation of paths for surface currents which show up as an increase in leakage current in the transistors. These can be eliminated by classical layout techniques, namely the use of an enclosed geometry for the transistor channels and of guard-rings between transistors [6].

Based on these assumptions, the CMS front-end readout circuits were translated into a standard quarter micron CMOS technology. The selected process features a minimum  $L_{\text{eff}}$  of  $0.18\ \mu\text{m}$ , up to six metal layers for compact routing and a low

operating voltage (2.5 V) for low power applications. It also provides capacitances and resistances for analogue circuits, and noise performance is good. These characteristics motivated the decision to design a new version of the APV circuit (the APV25) in this technology.

In the following sections, the design of the circuit (Section 2) is briefly reviewed. A more complete description of the design can be found in Ref. [7]. The core of the paper describes the experimental results obtained on the chip before irradiation (Section 3). One chip has been irradiated up to 20 Mrad and shows no degradation of the performances. A range of individual transistors has been irradiated to 50 Mrad. Single Event Effect tests have also been performed and the rate of Single Event Upset found to be small. Complete results on radiation tests will be presented elsewhere.

## 2. Design overview

The APV25 is a 128-channel VLSI circuit for the readout of the CMS tracker. Its architecture is based on the previous APV circuits. In this section the design is briefly reviewed, highlighting the main differences with respect to previous versions.

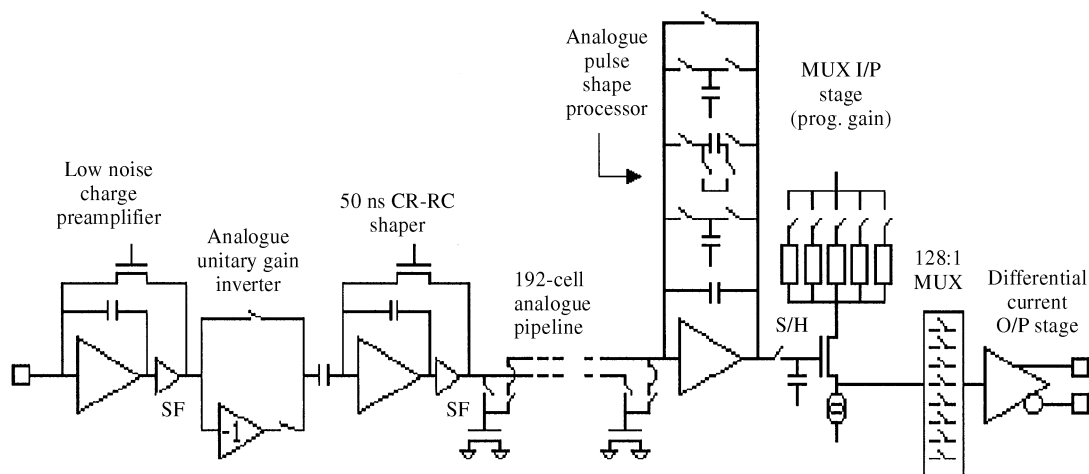


Fig. 1. Block diagram of one channel of the APV25.

The schematic of one channel is shown in Fig. 1. A Minimum Ionising Particle (MIP) generates about 25 000 electron–hole pairs in 300  $\mu\text{m}$  of silicon. This charge signal is transformed into a voltage step by a charge preamplifier. Depending on which side of the detector junction is read, opposite signal polarities can arrive at the input of the charge preamplifier. In order to cope with the reduction in power supply range while maintaining the capability to handle both signal polarities, a selectable unity gain inverter has been added at the output of the charge preamplifier. In this way, the voltage step on the coupling capacitance to the shaper is always positive. The following block is a CR-RC shaper with a peaking time of 50 ns. The equivalent noise charge obtained with HSPICE simulations is in a good agreement with the one calculated on the basis of the spectral density measured on a single transistor test structure and is equal to  $246 + 36 \cdot C_d [\text{pF}] e^- \text{rms}$ . The total gain of the charge preamplifier with the shaper is about 100 mV/MIP with a total power consumption of 1.15 mW/channel.

The output of the shaper is sampled at 40 MHz and stored in an analogue pipeline. The length of the pipeline has been increased to 192 cells, to accommodate for latencies up to 4  $\mu\text{s}$ , while handling up to 32 or 10 triggers, respectively, in peak and deconvolution mode. The pipeline is DC-coupled to the Analogue Pulse Shape Processor (APSP), which works in either *Peak* or *Deconvolution* mode [2]. The APSP adds a power consumption of 0.2 mW/channel and it has been designed so to keep an equal gain of 100 mV/MIP in both peak and deconvolution mode.

The voltage at the output of the APSP is sampled and the 128 samples are converted into current and multiplexed by a 3-level multiplexer [8]. The nominal gain at the output of this block is 100  $\mu\text{A}$ /MIP and five programmable settings (nominal,  $\pm 10\%$ ,  $\pm 20\%$ ) have been implemented in the APV25. The power consumption of the multiplexer is 0.17 mW/channel. A current output buffer has been added, too. It provides additional gain (current multiplied by 10) as well as single to double ended conversion for improved common mode rejection, with a power consumption of 20 mW, corresponding to 0.16 mW/channel.

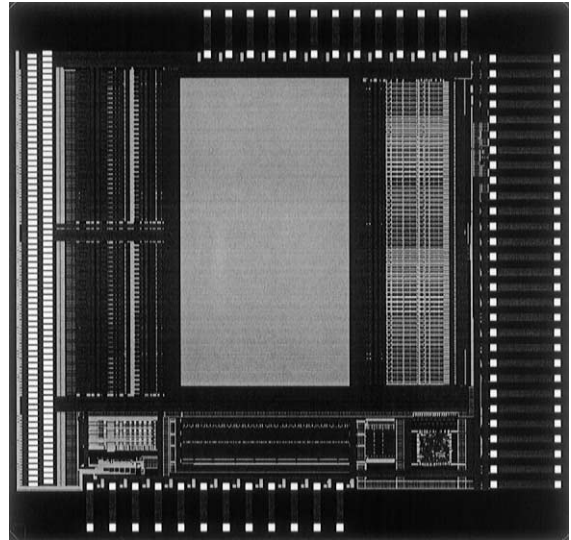


Fig. 2. Floorplan of the APV25.

The output data format (Fig. 3) is same as in the previous APV circuits, with 12 bits of digital header (3 start bits, followed by an 8-bit pipeline column address and one error bit) and the 128 analogue data samples. A tick mark is output every 1.75  $\mu\text{s}$  if no data is present in order to keep the synchronisation with the data acquisition system. In the APV25 the digital levels are  $\pm 4 \text{ mA}$  on each line of the differential output. A new fast 40 MHz mode has been added so that data can be read out either at this speed or at the standard 20 MHz frequency.

With respect to the APV6, power has been saved in the analogue part (1.35 against 1.89 mW/channel) and in the digital part (0.41 against 0.55 mW/channel). The power added by the additional output buffer is compensated by the savings in the following off-chip multiplexing stage.

The floorplan of the APV25 is shown in Fig. 2.

### 3. Electrical characterisation

#### 3.1. Test with a bare chip

An example of a measured data frame is shown in Fig. 3. The levels are as expected and the 1 MIP

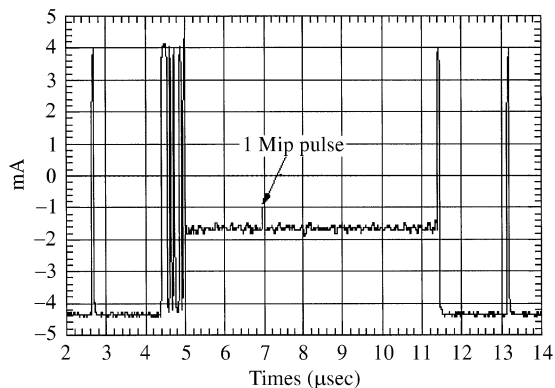


Fig. 3. Example of an output frame on one line of the differential output.

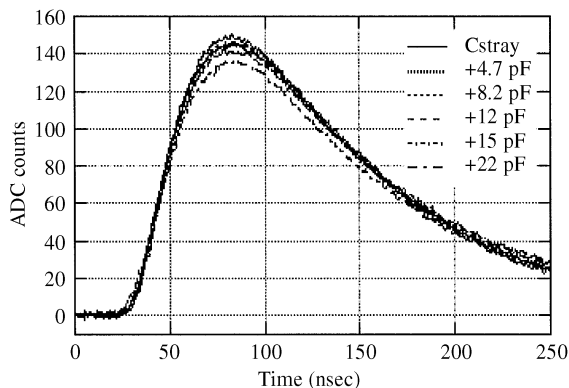
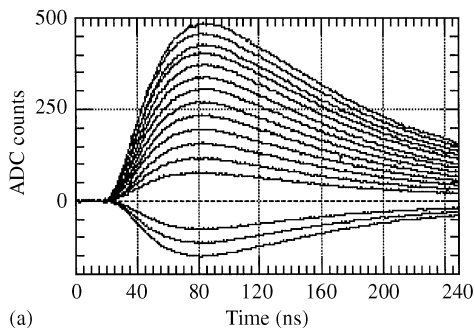
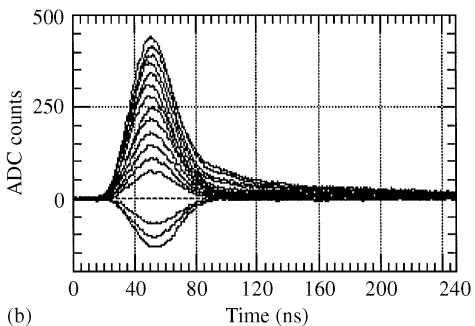


Fig. 4. Response of the APV25 as a function of the input capacitance (peak mode).

pulse on one channel is clearly visible. As in previous versions, the APV25 has no direct output from the shaper. The analogue waveform can be reconstructed by reading out the analogue output from a single channel while changing the phase of the calibration pulse with respect to the 40 MHz clock. This measurement can be done for both peak and deconvolution modes. In the curves shown in Fig. 4, the measurements have been repeated for values of the input load capacitance, varying from the bare stray capacitance up to 22 pF, i.e. higher than the capacitance of an irradiated CMS detector. Loading the input does not change the shape significantly. The output in peak mode fits well to a 50 ns CR-RC with no (or very little) undershoot.



(a)



(b)

Fig. 5. Response curve of the APV25 as a function of the input signal. (a) Peak mode, (b) deconvolution mode.

In order to test the linearity of the circuit, signals ranging from  $-2$  to  $-1$  and from  $+1$  to  $+7$  MIPs in 0.5 MIP steps have been fed to the input. The results are shown in Figs. 5 and 6. The linearity is very good up to 3 MIPs and remains better than 5% up to 5 MIPs. The results for the deconvolution mode are similar.

The equivalent noise charge has been measured as a function of the input capacitance. Typical curves are shown in Fig. 7 for a particular channel, and for both peak and deconvolution mode. The noise at 0 pF is  $246$  and  $396e^-$  rms with the slope being  $36$  and  $59.4e^-$  rms/pF in peak and deconvolution mode, respectively. The noise in deconvolution is higher than the one measured in peak mode as expected from the theory. For an input capacitance  $C_d$  of 18 pF, the noise is slightly less than 900 and about  $1500e^-$  rms in peak and deconvolution mode, respectively. These values represent a significant improvement with respect to previous versions of the APV [3, 9]. The noise (in ADC counts rms) as a function of the channel number is shown in Fig. 8. Apart from three

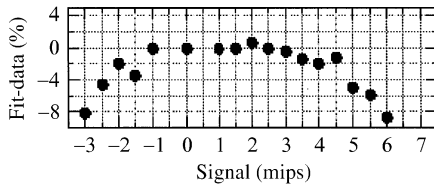
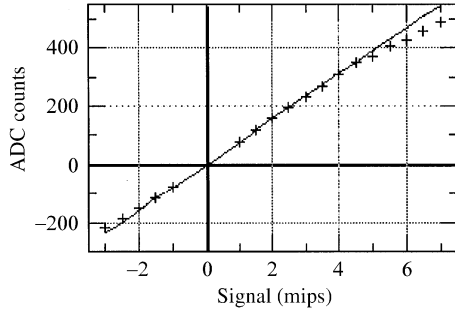


Fig. 6. Calibration curve and linearity in peak mode.

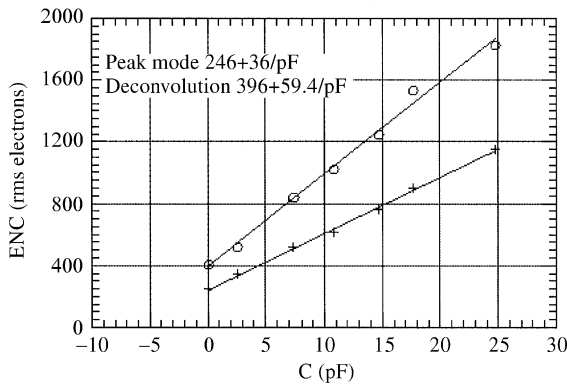


Fig. 7. Equivalent noise charge as a function of the input load capacitance in peak and deconvolution mode. Measurement done on channel 109 (see Fig. 8).

groups of bonded channels showing higher noise as expected, there is a clear slope across the chip. The observed slope can be explained by the different length of the tracks from the input pad to the input FET (Fig. 2). At room temperature and with the given shaping, a series input resistance  $R_{series}$  gives a contribution to the noise equal to  $ENC_{series} = 3.5C_d[pF] \sqrt{R(\Omega)}$ . The estimated variation in  $R_{series}$  from 13 to 70  $\Omega$  across the chip matches well with the measured values of ENC. The layout of the input tracks has been

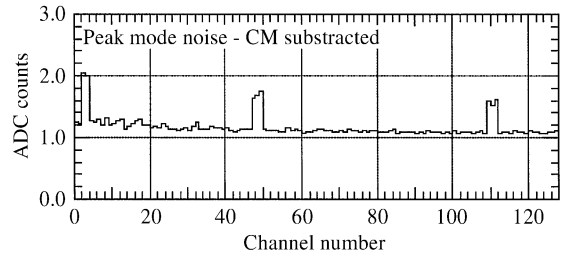
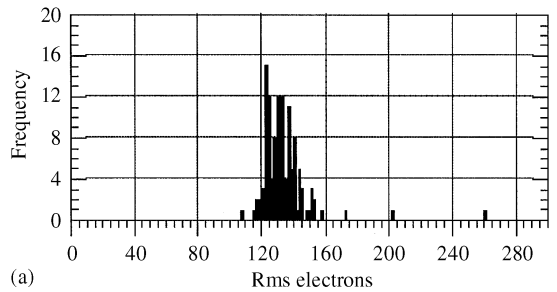
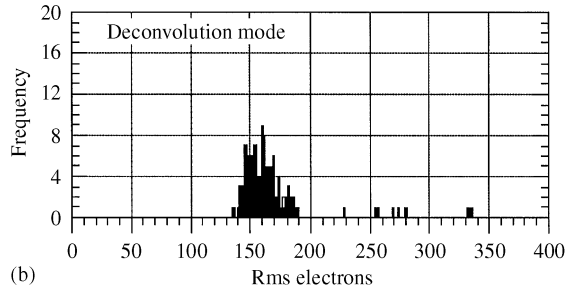


Fig. 8. Noise as a function of channel number.



(a)



(b)

Fig. 9. Distribution of the standard deviation of the single channel pipeline pedestal for one chip. (a) Peak mode, (b) deconvolution mode.

improved following this observation and the second version of the chip will cure this problem (see Section 4).

The uniformity of the pipeline is of great concern for this circuit. For every channel and every location, the pedestal and the gain have been measured. For every channel, a rms pedestal has been obtained over all the locations. The distributions (Fig. 9) of the rms for both the peak and the deconvolution mode are well confined and centred around 130 and 160  $e^-$  rms, respectively. The gain distribution for a single channel has a standard

deviation of 0.4%, i.e. of  $100e^-$  rms in peak mode. Both contributions to the total noise (pedestal and gain) can be considered negligible.

The logic has been tested at different operating voltages: it works at nominal speed down to 1.5 V supply.

The 40 MHz mode has also been tested and no significant difference has been found with respect to the standard 20 MHz mode.

### 3.2. Tests with a silicon detector

The results from the chip without a detector as load have been confirmed by preliminary measurements of the performances of an APV25 connected to a silicon detector. The tests were done with an APV25 connected to a 5 cm silicon microstrip detector, with 50  $\mu\text{m}$  pitch and 350  $\mu\text{m}$  thickness, biased at 100 V. A  $\text{Sr}^{90}$   $\beta$  source was used. In the tests, triggers were accepted if they occurred within 7 ns of the APV clock rising edge. Only single-strip clusters were selected. The pulse-height distribution for both peak and deconvolution mode is shown in Fig. 10. The signal-over-noise ratios quoted correspond quite closely to those expected from bare chip measurements.

## 4. Conclusions

The results shown in the previous sections demonstrate the excellent performance of the APV25, the front-end VLSI circuit for the CMS silicon tracker designed in a standard quarter micron CMOS technology. The characteristics of the circuit correspond to the expected values and to the requirements of the CMS tracker. Probe station tests on a sample of 250 chips randomly selected from four wafers show more than 85% of them are fully functional with no faulty pipeline location (24,576 cells per chip). Large quantity tests are currently under preparation and will take place during this year (2000).

The problem mentioned above (Section 3) of excess series resistance noise has been cured by changing the layout of the tracks from the front-end pads to the input FET. In this new iteration, the resistance of the input track will be lower than

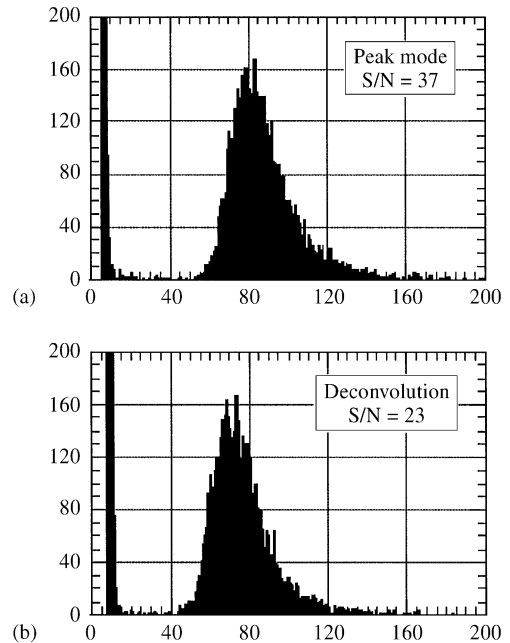


Fig. 10. Pulse-height distribution for an APV25 connected to a silicon microstrip detector and irradiated with a  $\text{Sr}^{90}$   $\beta$  source. (a) Peak mode, (b) deconvolution mode.

$5\ \Omega$  for every channel. The new version has been submitted in April 2000 and will be tested during this summer.

## Acknowledgements

We would like to acknowledge technical support provided by CERN. Particular thanks are due to Sandro Marchioro and Kostas Kloukinas.

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