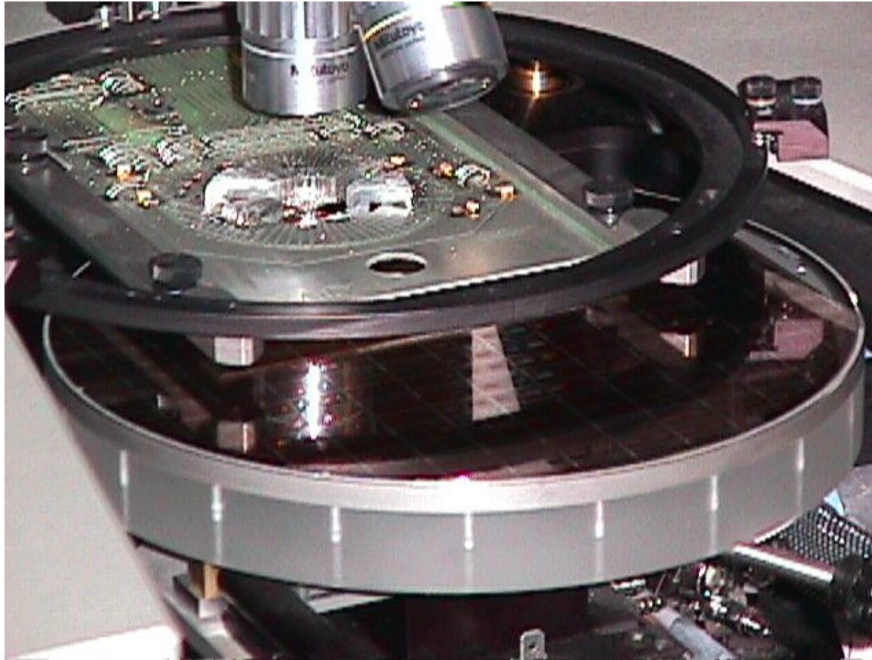
Results from APV25 wafer testing



- Wafer Probing Set-Up
- Test Summary
- Current Status
- Results
- Summary

Wafer Probing

- Set-Up:
  - PC running LabVIEW software
  - VME Crate containing:
    - SEQSI sequencer
    - VI^{2}C card
    - 8-bit FADC
  - RS232 interface b/w PC and Micromanipulator probe station
- Wafer probing:
  - 396 complete APV25 sites per wafer
  - ~10 hours testing time per wafer
  - Results archived on local database
  - 'Wafer map' summary and cutting template

Test Summary

- Basic digital functionality
  - Read & write to all registers
  - Check for stuck bits
  - Chip addressing
  - Correct data frame header/address
  - Random triggers
- Power supply currents
  - Check I_{DD} & I_{SS} during operation
- Channel pedestals and calibration
  - Adjustable analogue baseline
  - Check channel pedestals
  - Pulse shape and gain for all channels
- Pipeline
  - Check pipeline pedestals
  - Correct pipeline column address
- Voltage Stressing
  - Reduces infant mortality rate
  - Dynamic Voltage Stress:
    - APV operation @ 1.5 x V_{DD}
    - Stress duration ~5 s
  - Enhanced Voltage Stress:
    - Additional bump to 2.0 x V_{DD}
    - Stress duration = 1000 ms
  - (Burn-in not recommended)
- Multi mode
  - Measure pulse shape whilst operating APV in multi mode
- FIFO
  - Check all 30 FIFO locations for stuck bits
- Muxgain
  - Check gain adjustment at multiplexer stage

Current Status

- ‘Final system’ now in place
  - Software modifications:
    - Probe station control
    - New tests
  - Hardware modifications:
    - New probe card
    - Voltage stress testing
  - Outstanding modifications:
    - Temperature measurement

- 9 wafers probed (3564 die)
  - **2667 die passed Þ yield = 75%**
    (70, 77, 79, 75, 76, 73, 77, 80, 66%)

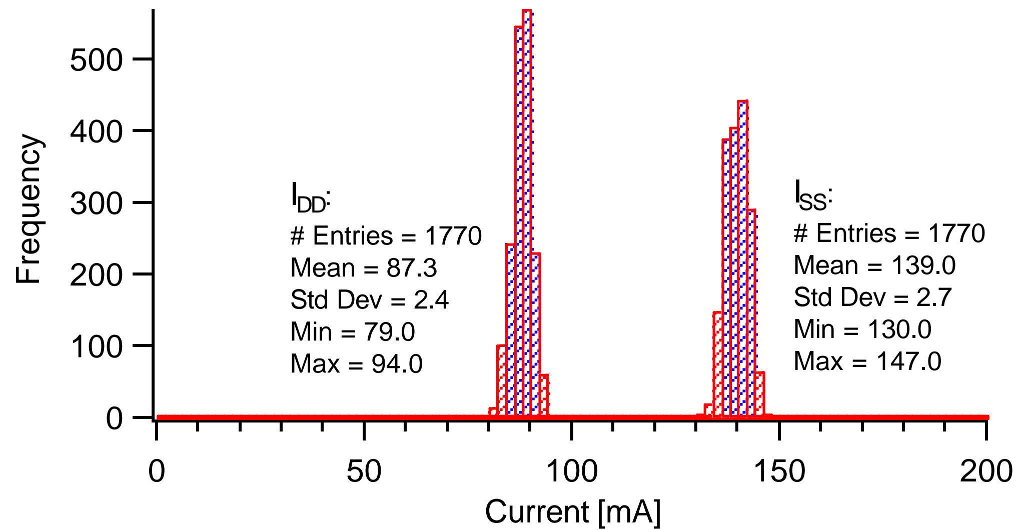
  - 1 wafer showed surface damage (scratching) on delivery
  - ‘Final system’ used to probe last 6 wafers. Results from KGD to follow…

- Wafer cutting
  - 4 wafers cut (MinTech)
  - KGD from 1st cut wafer reprobed
    - 3 failures from 271 KGD
    - Failures are due to cutting damage

- Wafer reprobing
  - Check on reproducibility of results
  - 1 wafer reprobed
    - 9 discrepancies from 396 sites
    - Due to poor contact → reprobe on-wafer

  - **Screening is effective!**
    - Bad die not escaping net

Supply Currents



- Operational chip configuration
  - Deconvolution mode
  - Raised baseline
  - Default I^2C bias values
- Cuts on supply currents:

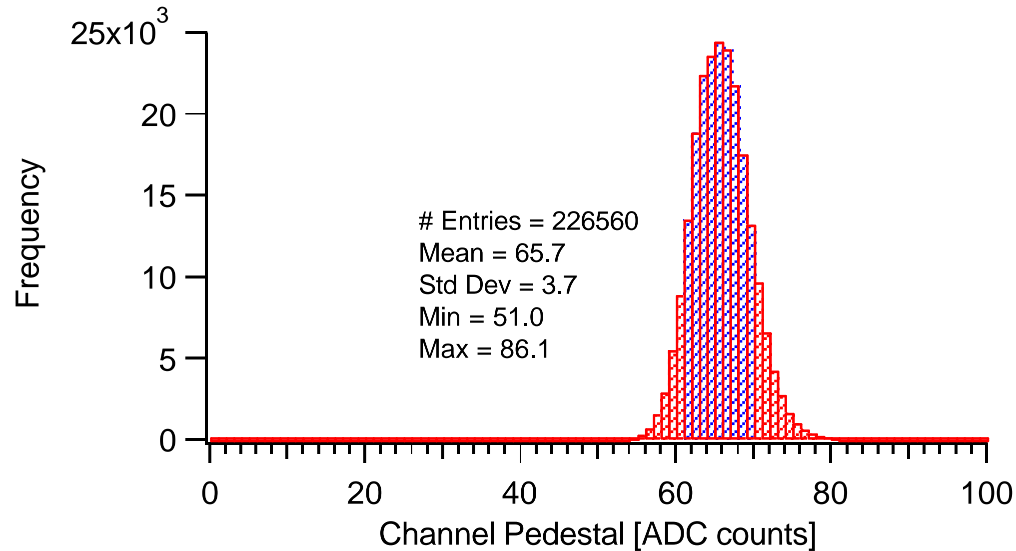
  $70 < I_{DD} < 100$ mA

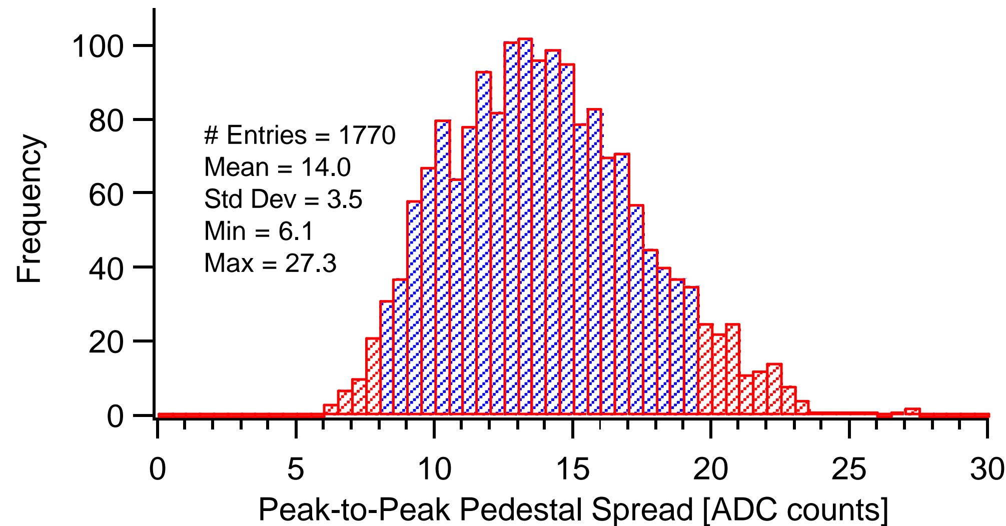
  $120 < I_{SS} < 170$ mA
- Measured supply currents:

  $I_{DD} = 87.3 \pm 2.4$ mA

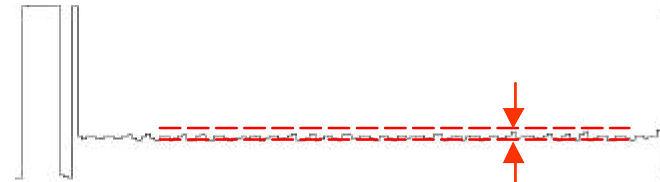
  $I_{SS} = 139.0 \pm 2.7$ mA

Channel Pedestals



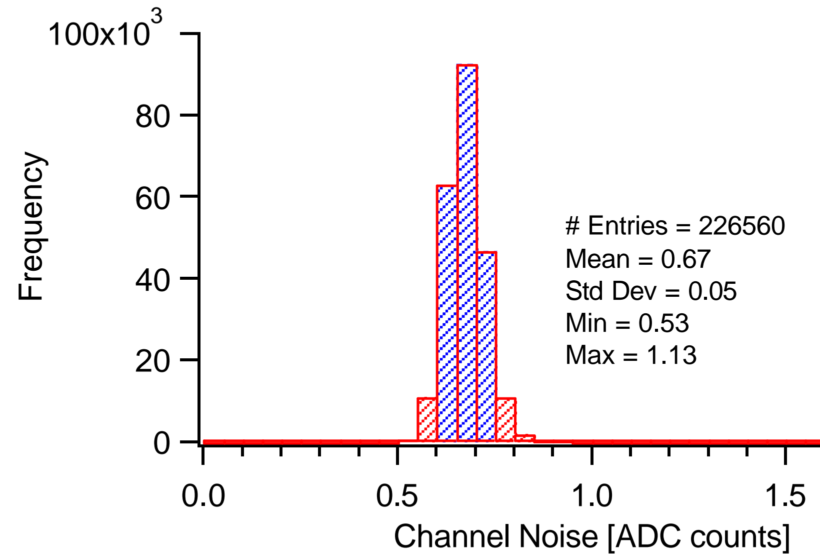


- Cuts on channel pedestals:
  - 50 < Pedestal < 90 [ADC counts]
  - (Raised baseline)
- Measured channel pedestals:
  - (Decon) 65.7 ± 3.7 [ADC counts]
  - (Peak) 67.1 ± 3.8 [ADC counts]



- Pedestal spread ≈ 0.5 mips
  - Worst case ≈ 0.9 mips
  - (1 mip ≈ 30 ADC counts)

Channel Noise



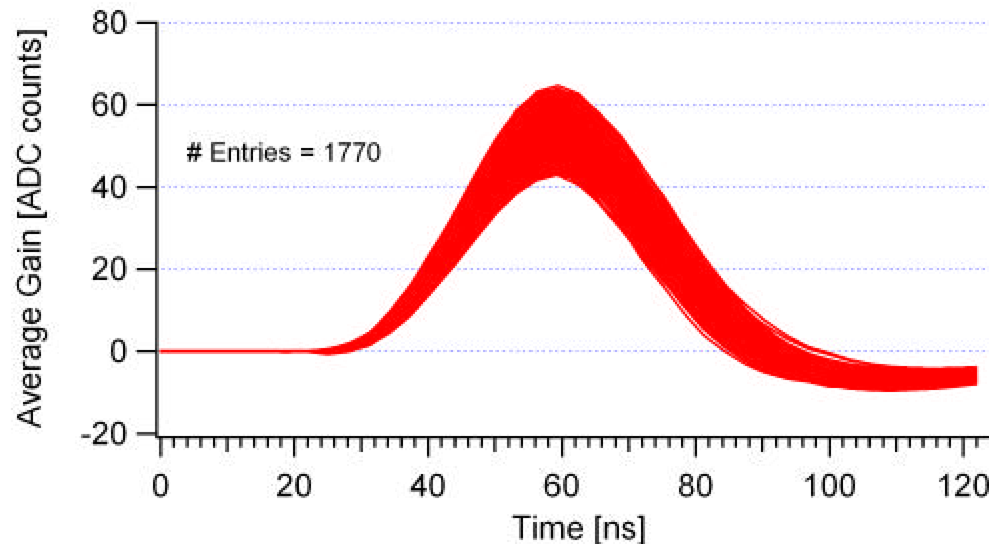
- ENC conversion
  - No external signal generation for calibration, can only approximate…
  - Digital header range ≈ 8 mips (± 20%)
≈ 240 bits (± 5%)
  - 1 mip ≈ 25000e

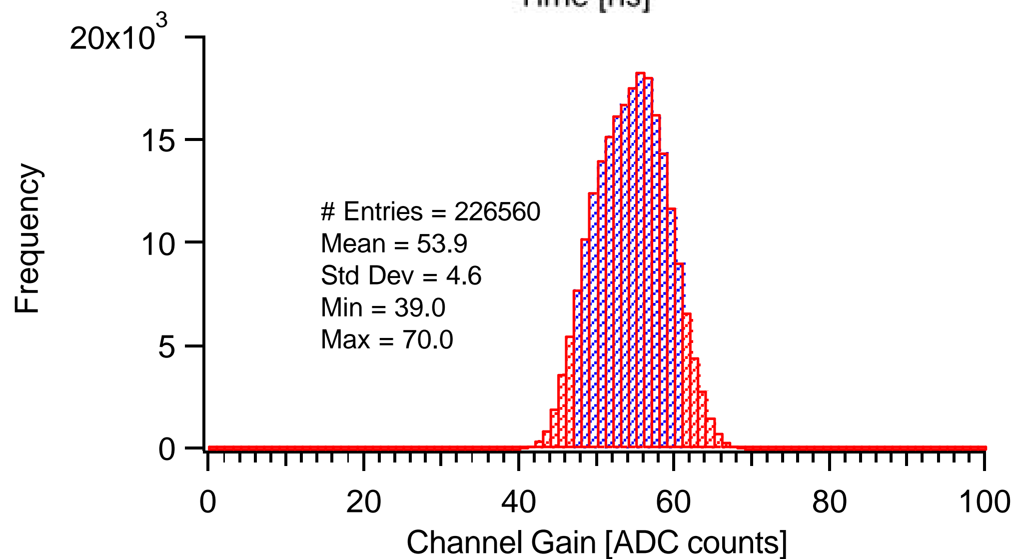
    ⇒ 1 mip ≈ 30 ADC counts
⇒ 1 ADC count ≈ 830e

- Channel noise (deconvolution mode):

  = 0.67 ± 0.05 [ADC counts]
≈ 560e
(cf. 430e measured with calibrated set-up)

Pulse Shapes and Gain

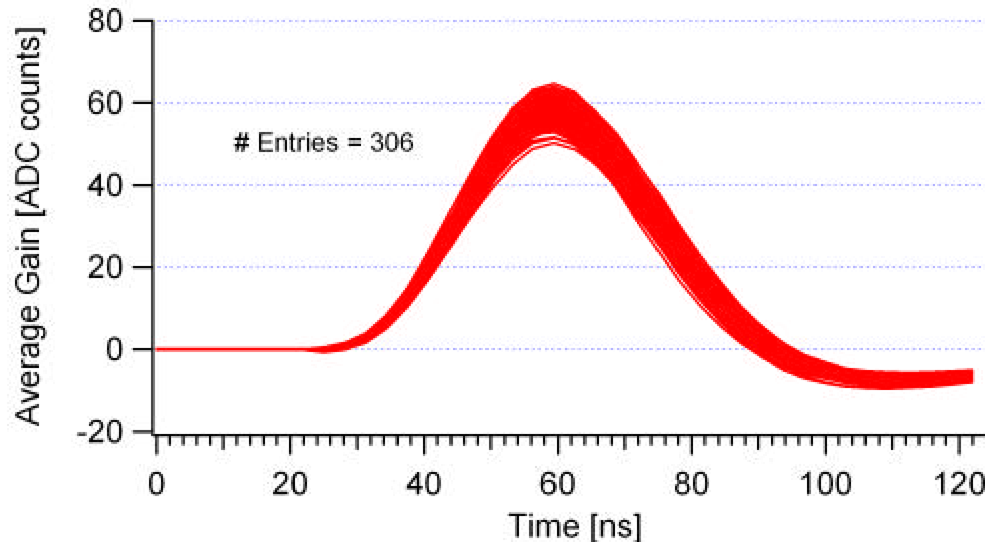


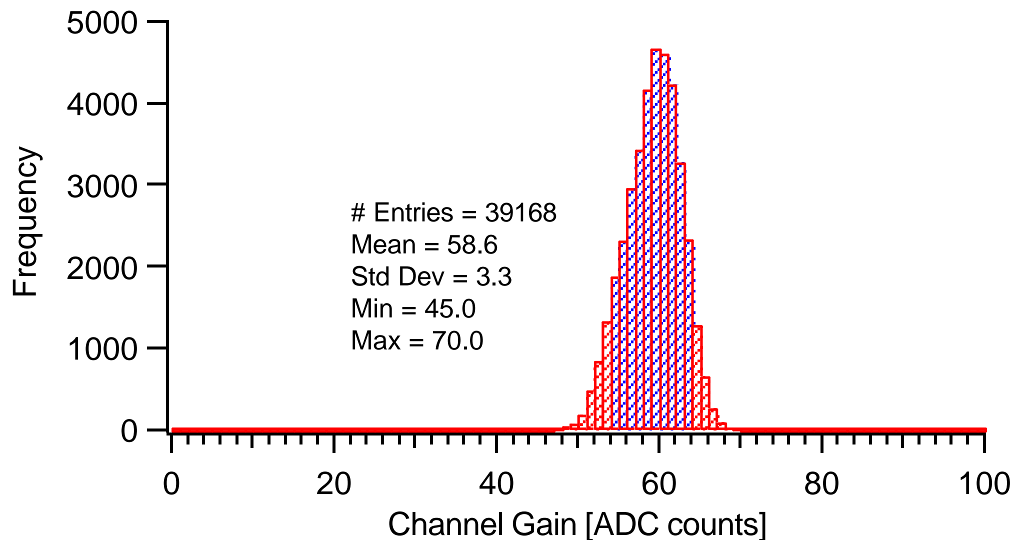


- Data from 6 wafers (1770 KGD)
  - Deconvolution mode
  - ICAL = 50 (~2 mips)
- Cuts on channel gain (G):
  - $G_{abs} > 20$ [ADC counts]
  - $| G_{abs} - G_{ave} | < 15$ [ADC counts]
- Measured channel gain:

  $G = 53.9 \pm 4.6$ [ADC counts]

Pulse Shapes and Gain (2)



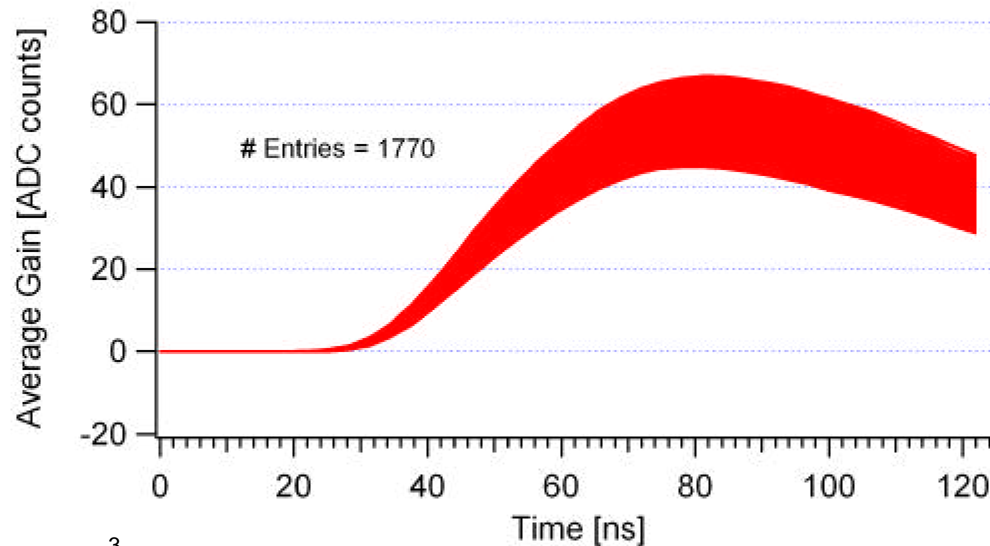


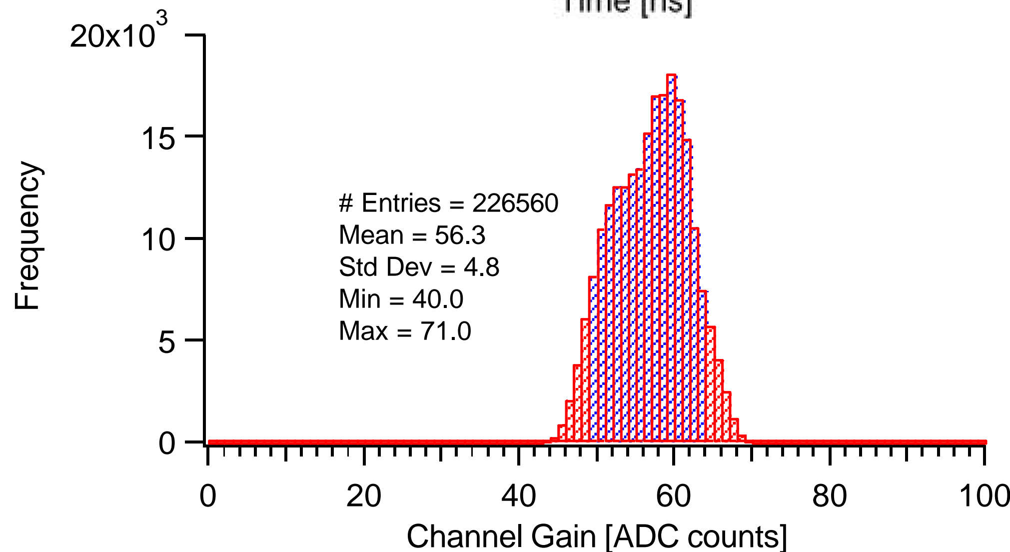
- Data from 1 wafer (306 KGD)
  - Deconvolution mode
  - ICAL = 50 (~2 mips)
- Cuts on channel gain (G):
  - $G_{abs} > 20$ [ADC counts]
  - $| G_{abs} - G_{ave} | < 15$ [ADC counts]
- Measured channel gain:
  $G = 58.6 \pm 3.3$ [ADC counts]
- Maximum deviation in gain
  Across 6 wafers = $^{+29.9\ \%}_{-27.6\ \%}$
  Across 1 wafer = $^{+19.5\ \%}_{-23.2\ \%}$
  - Due to non-linearity in calibration cct capacitors and/or multiplexer resistors

Summary

- 'Final' probing set-up in place – ready for 50 wafer order
- **Excellent yield: 75%** (2667 KGD)
  - APV25S1 performs excellently
  - Good uniformity between chips and wafers
- Results 'black or white' – no 'grey area'
  - Die either good or not
  - Loose cuts appear to screen effectively
  - ~ 50% of failures are digital
- Wafer cutting
  - ~ 1% die failed due to cutting damage (3/271)
- Wafer reprobing
  - Reproducible results
  - Screening is effective

Pulse Shapes and Gain (Peak)





- Data from 6 wafers (1770 KGD)
  - Peak mode
  - ICAL = 50 (~2 mips)
- Cuts on channel gain (G):
  - $G_{abs} > 20$ [ADC counts]
  - $|G_{abs} - G_{ave}| < 15$ [ADC counts]
- Measured channel gain:

  $G = 56.3 \pm 4.8$ [ADC counts]