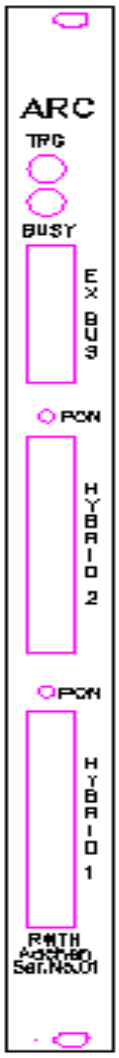
# ARC

A SUPER SIMPLE
TO USE

# APV READOUT CONTROLLER

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# Contents

**FEATURES**

| | | |
|---|---|---|
| # of Channels | : | 6 |
| Memory | : | 8K x 8Bit per Channel |
| Resolution | : | 8 Bit |
| Sampling Rate | : | Up To 40 MHz |
| Bus System | : | SRDISA |

**SPECIFICATIONS**

| | | | |
|---|---|---|---|
| Clock | : | Internal 40 MHz | |
| | | or | Software Selectable |
| | | External Clock Input | LVDS up to 40 MHz |
| | | Clock Output | LVDS |

Trigger :

| | | |
|---|---|---|
| Input | : | Internal (Software) or External (NIM or LVDS) |
| Output | : | LVDS |

| | | | | |
|---|---|---|---|---|
| Hybrid I / O | : | Analogue Input's | : | 6 Differential Voltage |
| | | Resistance | : | 50 Ohm |
| | | Slow Control | : | 3 Standard Buffered I2C Links |
| | | Clock/Trigger | : | 2 LVDS Clock Lines |
| | | | | 2 LVDS Trigger Lines |

| | | | |
|---|---|---|---|
| Expansions Port : | Input or Output : | Clock | LVDS |
| | | Trigger | LVDS |
| | | Synchronised Trigger | LVDS |
| | | APV Trigger | LVDS |

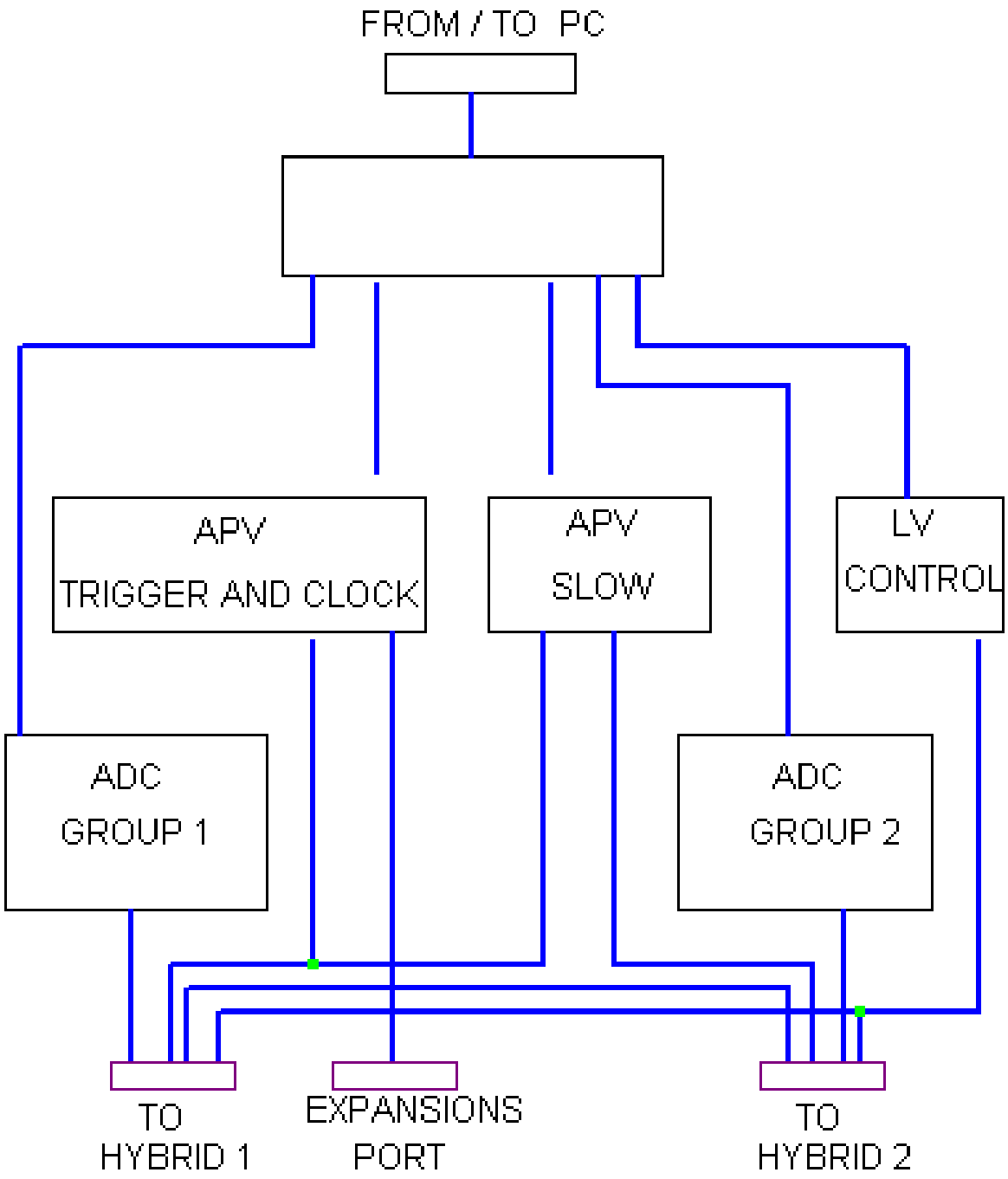
POWER REQUIREMENTS:

1.4 A @ + 5V
60mA @ - 5V

DIMENSIONS : Double Euro Format

# APV READOUT CONTROLLER

## BLOCK DIAGRAM



# Circuit Description

The ARC Module is a standard double Euro Format PCB. For larger setups it can be placed into a 19 " crate, for small set-ups it can be used as a single board device. A standard PC acts as control computer. The module is connected to this computer via a 50 pin flat cable and a PCMIO interface. The PCMIO Module fits into a IBM XT slot and serves as interface between the ISA bus and the ARC module.

The ARC board combines all functions needed for running and testing of two APV front end hybrids.

## CLOCK AND TRIGGER

One of it's function blocks is the clock and trigger controller which generates the clock and trigger signals for both hybrids. The clock is primary generated by a local crystal oscillator. A software or an external ( NIM ) generated asynchron trigger is latched and then synchronised with the system clock. Awaked by this synchronised trigger an APV trigger pattern is sent to each front end hybrid. The trigger pattern has to be loaded into a local 16 bit data register. The MSB will be send first to the APV's. Any possible APV trigger pattern ( RESET, CAL REQUEST, EVENT TRIGGER ) has to be generated via this way. The trigger signal is distributed by a separate trigger link or if selected ( status register D7 ) as clock missing pulses.

## DATA SAMPLING

Two groups of three eight bit FADC's (one group for each hybrid ) sample the analogue data with a synchronised 40 or 20 MHz clock (selected by status register D8 ). For correct sample timing the FADC clock phase should be tuned, in ten steps of ~ 1.7 ns (ADC Clock Delay register ). The digitised data are stored in an 8 Kbyte RAM for each channel. The sample record length is determined by the stop address. Sampling starts at address 0 and stops at the defined stop address ( stop address register ). The stop address may be set to any value between 0 and 8 Kbyte. A record complete is flagged in bit D1 of status register. A PC program may read this flag in polling mode and read the data after this bit is set. Before data read, the memory address counter should be set to the favorite start address ( memory address register ), a read cycle increments the address counter automatically.

## SLOW CONTROL

To handle the hybrid slow control function one I2C controller for each hybrid is applied on the board.

## LV CONTROLL

The hybrids are powered by the ARC module via the front end adapter board. The LV regulators are applied on the front end adapter board and can be switched on or off from the ARC module (status register D9). A separate I2C link controls a serial 8 bit ADC for measuring the LV hybrid currents.

**ADDRESS LAYOUT:**

| ADDRESS | Function | Data | DIR | NOTE | ACCESS |
|---|---|---|---|---|---|
| | | | | | Note 16 |
| XX0 H | Status | D15..D10 Sub Address | R/W | 11 | B |
| | | D9 SHDN Hybrid Power on / off | R/W | 12 | G |
| | | D8 Sample Rate 20 / 40 MHz | R/W | 13 | B |
| | | D7 APV Trigger Mode Select | R/W | 14 | B |
| | | D6 TUP Trigger Under Process | R | 2 | B |
| | | D5 EN / Disable Master Driver | R/W | | B |
| | | D4 EN / Disable Slave Mode | R/W | | B |
| | | D3 DAC / RAM / I2C select | R/W | | B |
| | | D2 DAC / RAM / I2C select | R/W | | B |
| | | D1 DAV | R | | B |
| | | D0 EN / Disable external Trigger | R/W | | B |
| XX2 H | Write DAC / Read RAM | [ D7 .. D0 ] / [ D15 .. D0 ] Write DAC / Read RAM | R/W | | G |
| XX4 H | Write Memory Address / Read Access Generates A Software Trigger | [ D12 ... D0 ] | R/W | 1 | G/B |
| XX6 H | Write APV Trigger Data And Reset Busy State | [ D15 ... D0 ] | W | | B |
| XX8 H | I2C Register A0 = 0 | [ D7 ... D0 ] | R/W | 15 | G |
| XXA H | I2C Register S1 | [ D7 ... D0 ] | R/W | 15 | G |
| XXC H | Write ADC Clock Delay | [ D3 ... D0 ] | W | | G |
| XXE H | Write RAM and Write StopAddress | | W | 10 | G |

Note 11: Status Register [ D15 ... D10 ]
The sub address can be written every time the board address is valid, the other status bits are only accepted if the subaddress matches with the board subaddress switches. A valid subaddress enables all other board accesses.

Note 12: Status Register [ D9 ]
PON Hybrid Power on / off => 1 / 0.

Note 13: Status Register [ D8 ]
Sample Rate 0 / 1 = 20 / 40 MHz. The 20 MHz ADC clock is synchronised with the APV reset 101.

Note 14: Status Register [ D7 ]
APV Trigger Mode Select. 1 / 0 = PLL trigger ( missing clock pulses ) / APV trigger on the separate trigger line.

Note 15:
The two I2C controllers on the same address must be selected via the bit [ D2 ] in the status register.
[ D2 ] 1 / 0 = selects the adapter board control bus / selects the hybrid slow control bus.

Note 16:
B => Board access.
G => ADC group or hybrid sensitive access, dependent on the LSB ( status register [ D10 ] ) in the subaddress register.

**ADDRESSING**

For the ISA address selection refer to the PCMIO Interface description.

Only the six lowest ISA bus addresses, A6.....A1 are fed through and decoded on the module. The module address is selected by means of SW1, an 8-way DIL switch ( the only one on the board ). The switches S8... S6* correspond to A6 ... A4 and define the base address. A compare match enables a write access to the status register to set a valid sub address pattern. The switches S5... S1* correspond to status register bits D15 ... D11 and define the sub address and enables an access only if the compare match.
The sub address bit D10 selects the hybrid group sensitive access like ADC control, APV slow control and memory access. For board sensitive access, like trigger control, D10 is irrelevant.
A3...A1 are on board used addresses, see table below.

| Address Bit | A6 | A5 | A4 |
|---|---|---|---|
| Select Switch | S8 | S7 | S6 |

| Sub Address Bit | D15 | D14 | D13 | D12 | D11 | D10 |
|---|---|---|---|---|---|---|
| Select Switch | S5 | S4 | S3 | S2 | S1 | Hybrid Group Select<br>0 ^= Hybrid 1<br>1 ^= Hybrid 2 |

* Sx ON ^= Address Bit = 1

**STATUS REGISTER**

**Address H x0**
**Data** D15 ... D0

This register, which may be read or written at any time, contains the sub address, status and mode flags.

| | | | |
|---|---|---|---|
| D15 ... D10 | Sub Address | | Refer to chapter addressing |
| D9 | 1 / 0 | PON | Hybrid Power On / Off |
| D8 | 1 / 0 | 40 / 20 MHz | ADC clock |
| D7 | 1 / 0 | PLL APV Trigger Mode / Separate | |
| D6 | 1 / 0 | TUP | Device under Process |
| D5 | 1 / 0 | En- / Disable | Master Clock and Trigger Driver |
| D4 | 1 / 0 | En- / Disable | Slave Clock and Trigger Mode |
| D3 | Select 1 | | |
| D2 | Select 0 | | |
| D1 | DAV | data available | |
| D0 | 1 / 0 | En- / Disable | External Trigger |

**Write DAC / Read RAM**

**Address H x2**

This register is used to adjust the analogue offset or read out the memory.

The analogue offset is channel selective adjustable in a range of 0% to 70 % ADC full scale, with a resolution of 8 bit. The ADC channel selection is done by the select 0 and select 1 bits in the status register.

**Write DAC** D7 ... D0

| sel 1 | sel 0 | offset DAC |
|---|---|---|
| 0 | 0 | channel 1 |
| 0 | 1 | channel 2 |
| 1 | 0 | channel 3 |

**Read RAM Data** D15 ... D0

| sel 1 | sel 0 | D15 ... D8 | D7 ... D0 |
|---|---|---|---|
| 0 | 0 | channel 2 data | channel 1 data |
| 1 | 0 | 00000000 | channel 3 data |

The memories are addressed by the address counter. This counter register can be written in order to read data from a special memory location. Each read memory access increments the memory address counter automatically.

**Write Memory Address / Read Software Trigger**

**Address H x4**

**Data** D12 ... D0 / 0

This register is used to configure the address counter or generate a software trigger.
The address counter has a length of 13 bit corresponding to the memory depth of 8 KB. The memory address can be written to read out data from this memory location. Every read memory access increments the memory address counter automatically.
A read access at this address generates a software trigger. This asynchronous trigger is latched and then synchronised with the system clock after sending the trigger pattern to the connected hybrids. The data sampling starts at memory address 0 and stops at the address which is set in the address stop register (at address H xE).

**Write APV Trigger Data**

**Address H x6**
**Data** D15 ... D0 select 0 =0; select 1 =0

This is used to configure the APV trigger pattern register.
Awaked by the synchronised trigger a APV trigger pattern is sent to each front end hybrid. The trigger pattern has to be loaded to trigger data register and may contain up to 16 bits. The MSB will be send as the first to the APV's. Any possible APV trigger pattern ( RESET, CAL REQUEST, EVENT TRIGGER ) has to be generated via this way. The trigger signal is distributed by a separate trigger link or if selected (status register D7) as clock missing pulses.

For generate longer trigger sequences the 16 bit trigger pattern register is spliced into two 8 bit parts spaced by a 8 bit programmable spacer counter. So are trigger pattern up to 255 + 16 clock cycles are possible.

**Slow control**

**Address H x8 and H xA**

**Data** D7 ... D0

This register is used to configure the I2C controller.

Three identically I2C controller are applied on the board. One for each hybrid selected by the sub address bit D10 and one additional for the LV control of both hybrids. Address H x8 selects the PCF8584 controller register S0 and address H xA selects the register S1.
The hybrid- and the LV- controller are selected with the sel 0 and sel 1 bits in the status register.

| sel 1 | sel 0 | I2C controller |
|---|---|---|
| 0 | 0 | Hybrid |
| 1 | 0 | LV |

For more information about the I2C Bus protocol refer to the Philips PCF8584 manual

For more information about the APV slow control refer to the APV 25 manual
For more information about the LV Control ADC refer to the Philips PCF 8591 manual

**ADC Clock Delay**

**Address H xC**

**Data** D3 ... D0

This register is used to configure the ADC clock adjustment.
For a correct sample timing the FADC clock phase should be tuned up. This can be done in ten steps of ~1.7 ns.

**Write Stop Address**

**Address H xE**

**Data** D12 ... D0

This register is used to set the stop address register or to write data into the RAM.

The sample record length should be preselected by the stop address. The sampling starts at address 0 and stops at the defined stop address. The stop address may be set to any value between 0 and 8 Kbyte.

**Write RAM Data**

**Address H xE**

Data D15 ... D0

For better testability , the memories are written with the same data like the stop address register.
The memories are addressed by the address counter. This counter register can be written to read or write data from or to a special memory location. Every read or write memory access increments the memory address counter automatically. The channel selection is done in the same way as for the read RAM function.

**Write RAM Data** D15 ... D0

| sel 1 | sel 0 | D15 ... D8 | D7 ... D0 |
|---|---|---|---|
| 0 | 0 | channel 2 data | channel 1 data |
| 1 | 0 | xxxxxxxx | channel 3 data |

# Appendix

## FE 6 Hybrid Slow Control Addresses

I2C controller at ARC addresses
S0 xx8 H
S1 xxA H
Sel 1 ... Sel 0 Status Register D3 ... D2 = 00

**APV's** H 40; H42; H48; H4A; Broadcast H7E

**MUX** Address H86

**PLL** H88; H8A; H8C; H8E

**LV Control** Address Selectable space H90 ... H9E Actual H90

ARC I2C controller Sel 1 ... Sel 0 Status Register D3 ... D2 = 01