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# Experience with ARC System in Pisa

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Pisa Module Test Group

## Outline

- ✍ Goals and tested samples
- ✍ Results of measurements
- ✍ Comparison ARC CMS-like measurements
- ✍ Conclusions

## Goal of tests

- ✍ test of our ARC system
- ✍ not full characterisation of modules

## Tested samples

- ✍ TIB001 and TIB002
- ✍ no HV bias on sensors

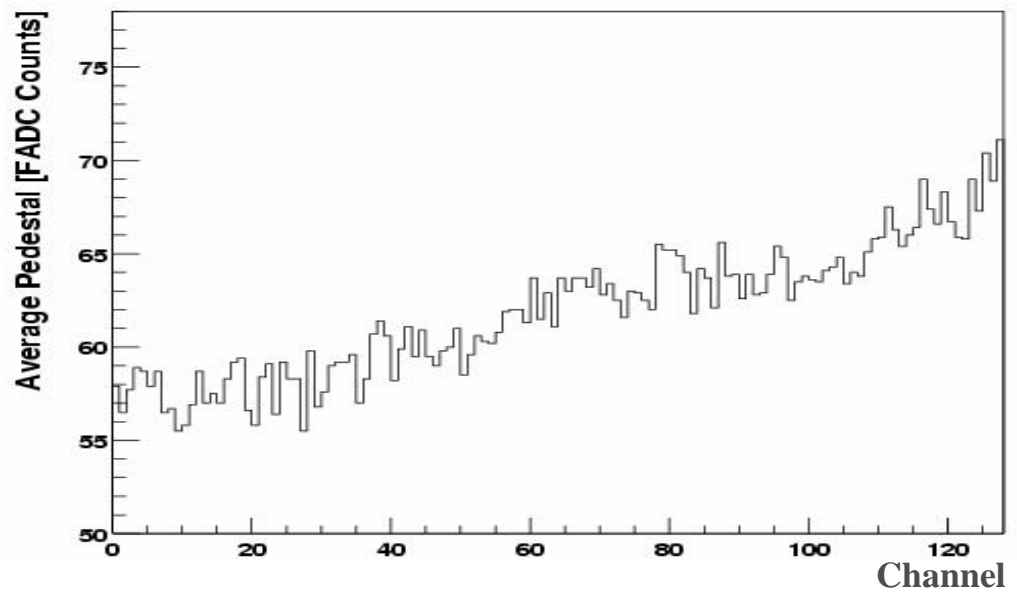
# Pedestal - TIB001, APV1

## ARC – no HV

```

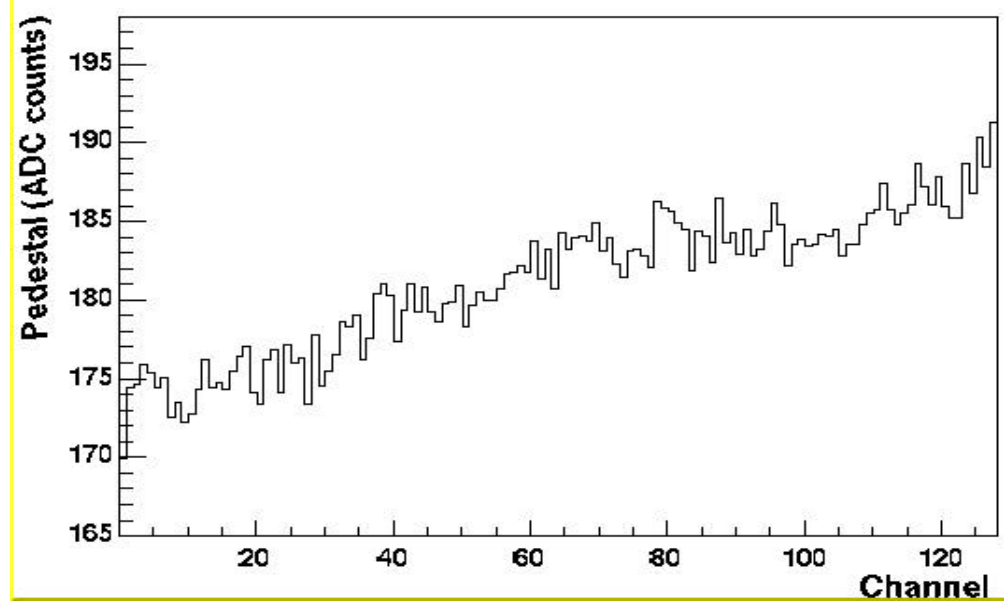
Chip Settings:
I2C.Address= 64
Mode= 43
Latency= 4
IPRE= 98
IPCASC= 52
IPSF= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VPSF= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Error= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```

Average Pedestal



## CMS – like no HV

pedestal Channel 1

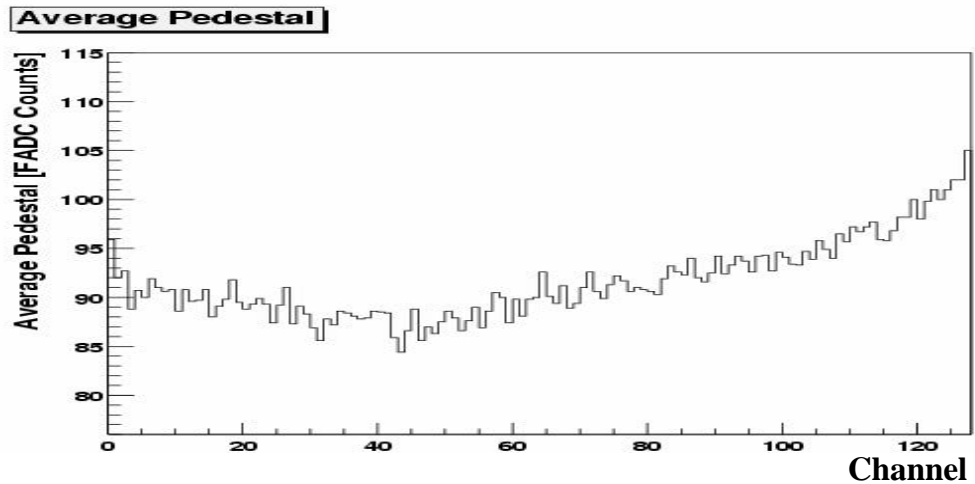


# Pedestal - TIB002, APV3

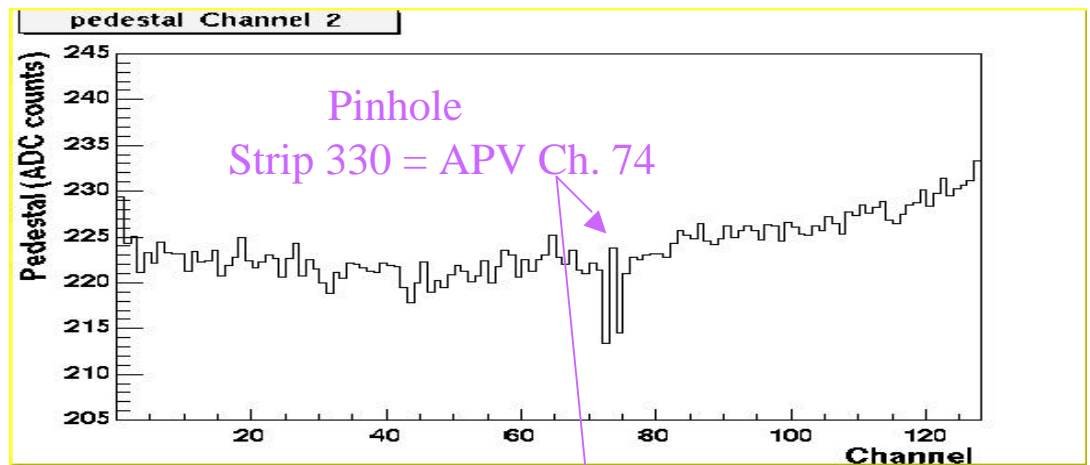
## ARC – no HV

```

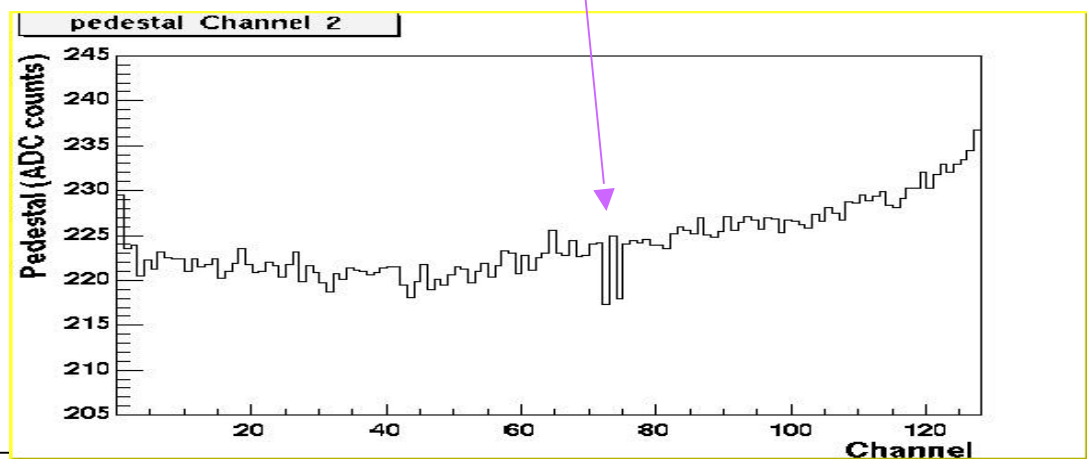
Chip Settings:
I2C.Address= 72
Mode= 43
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IPRE= 98
IPCASC= 52
IPSF= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



CMS – like  
no HV



CMS – like  
450V

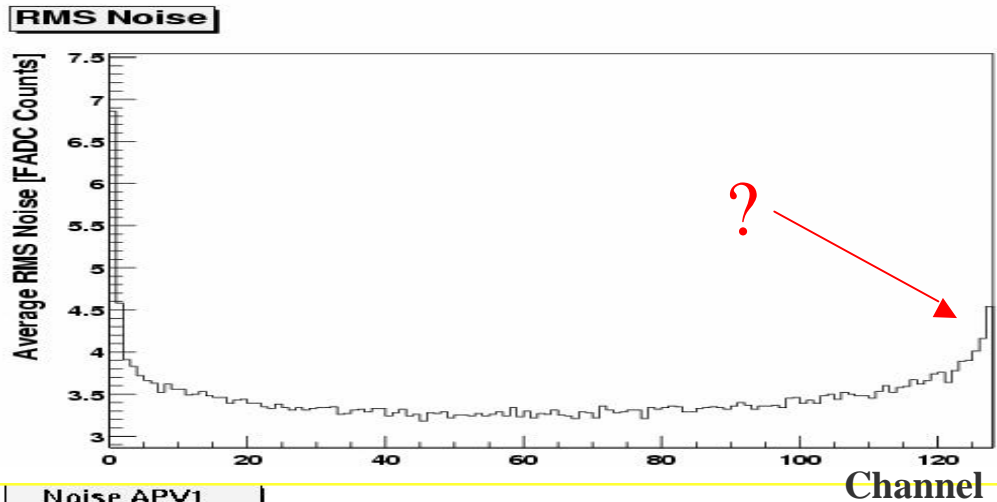


# Noise - TIB001, APV1

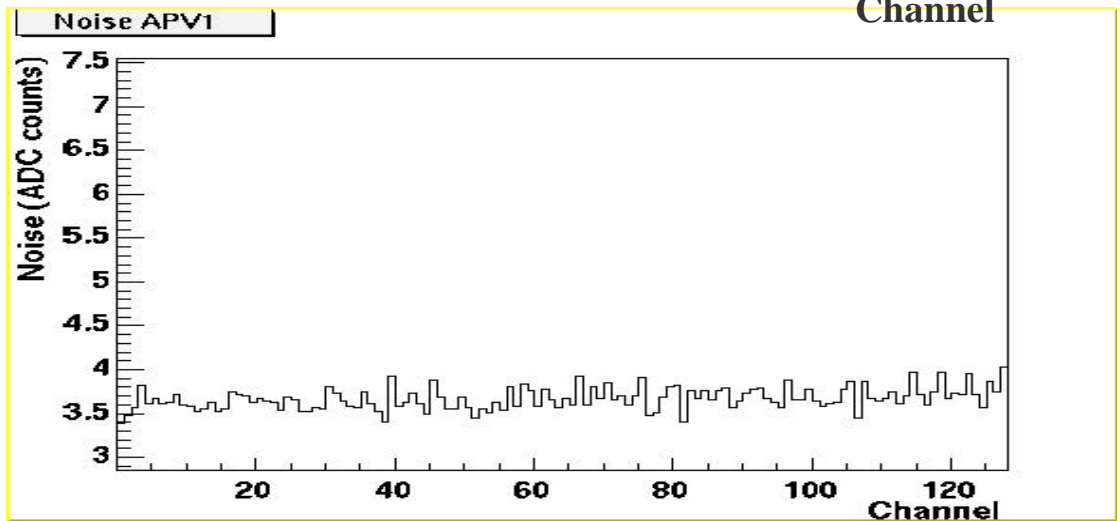
## ARC – no HV

```

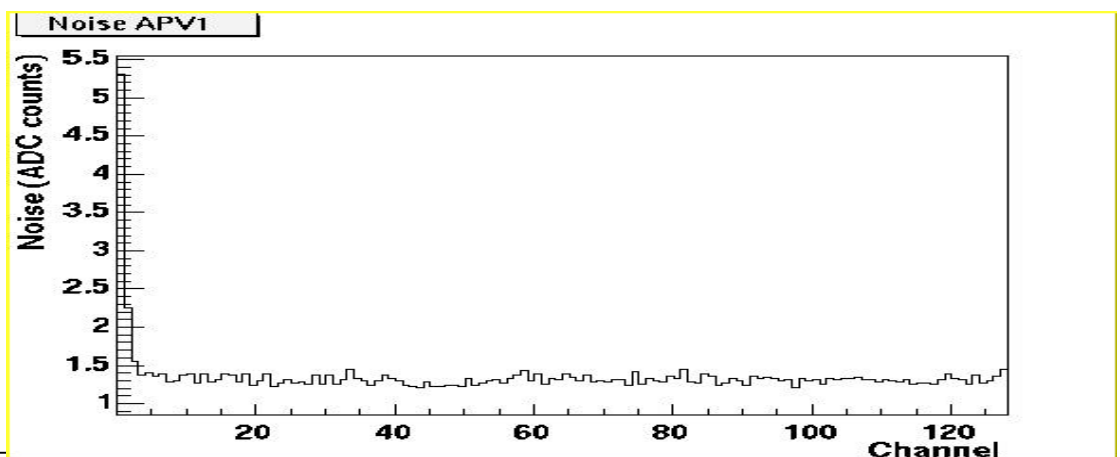
Chip Settings:
I2C.Address= 64
Mode= 43
Latency= 4
IPRE= 98
IPCASC= 52
IPSE= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Error= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



## CMS – like no HV



## CMS – like 300V

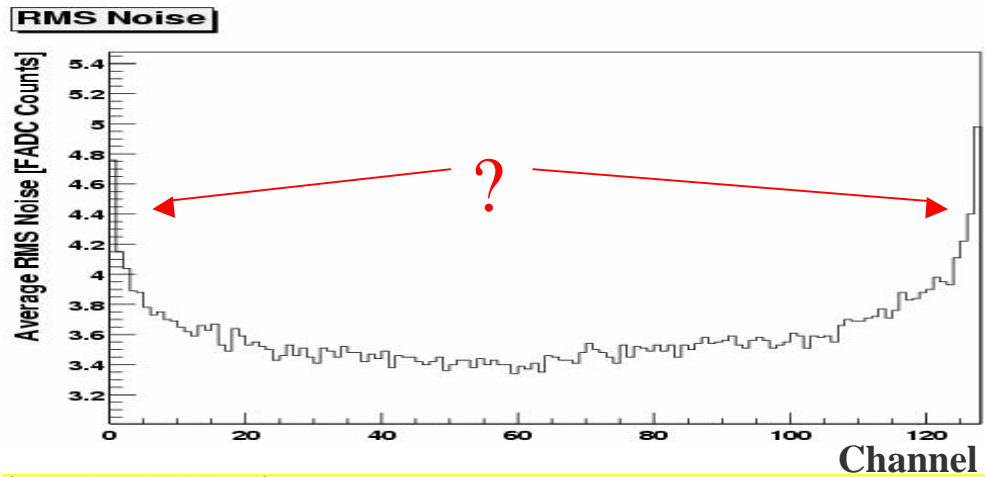


# Noise - TIB001, APV2

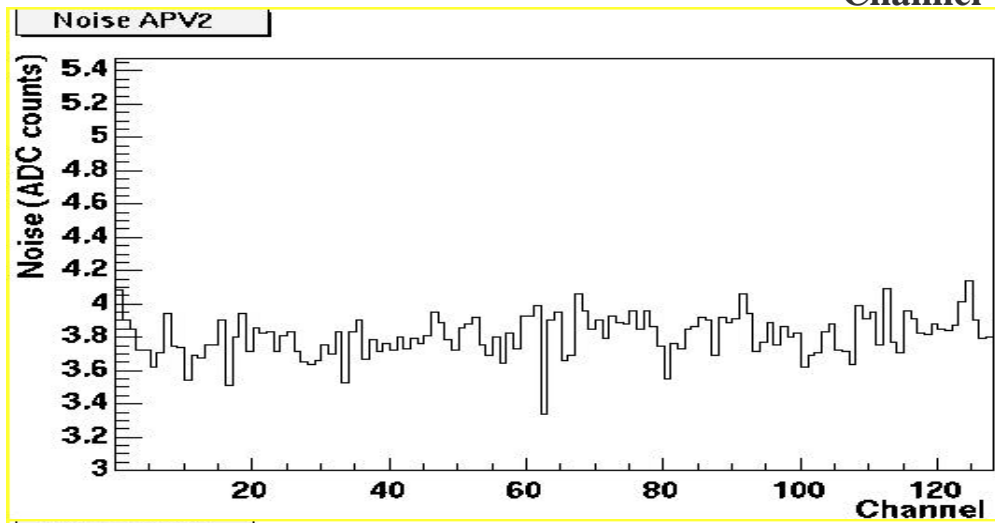
## ARC – no HV

```

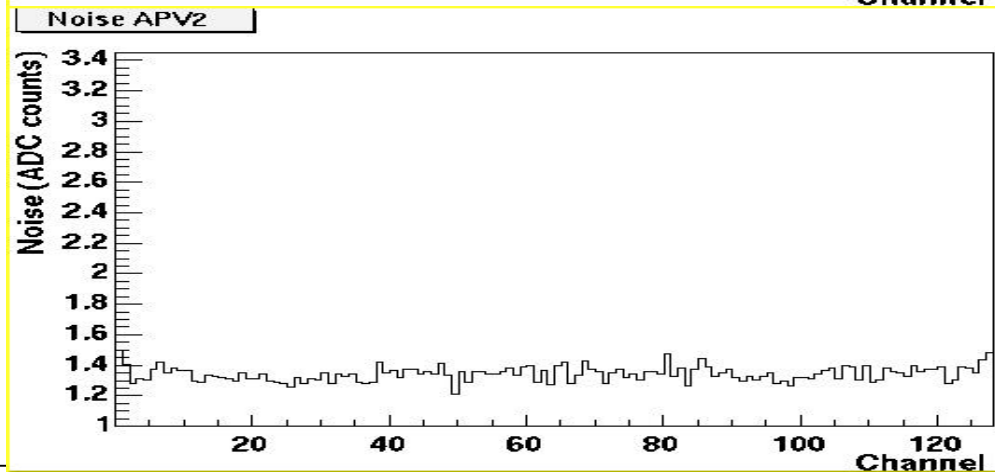
Chip Settings:
I2C.Address= 66
Mode= 43
Latency= 4
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IPCASC= 52
IPSF= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VPSF= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



## CMS – like no HV



## CMS – like 300V

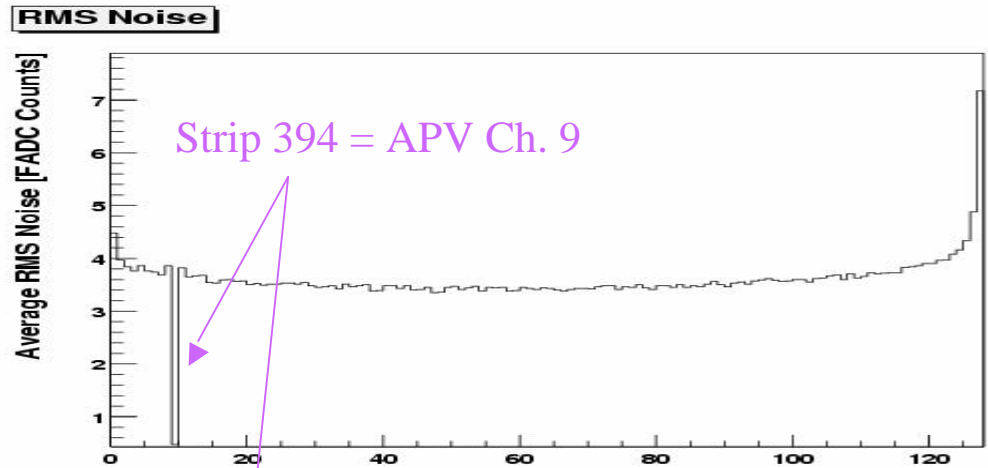


# Noise - TIB001, APV4

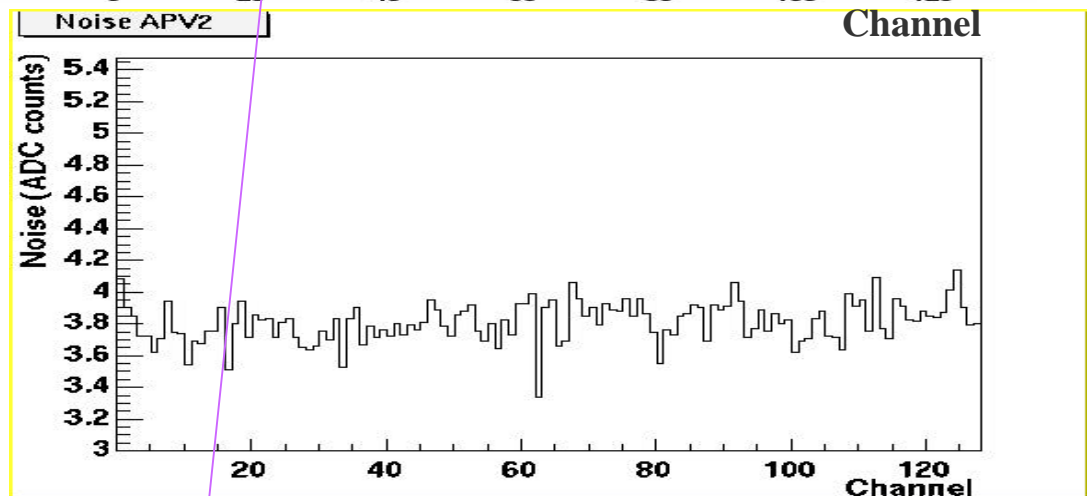
## ARC – no HV

```

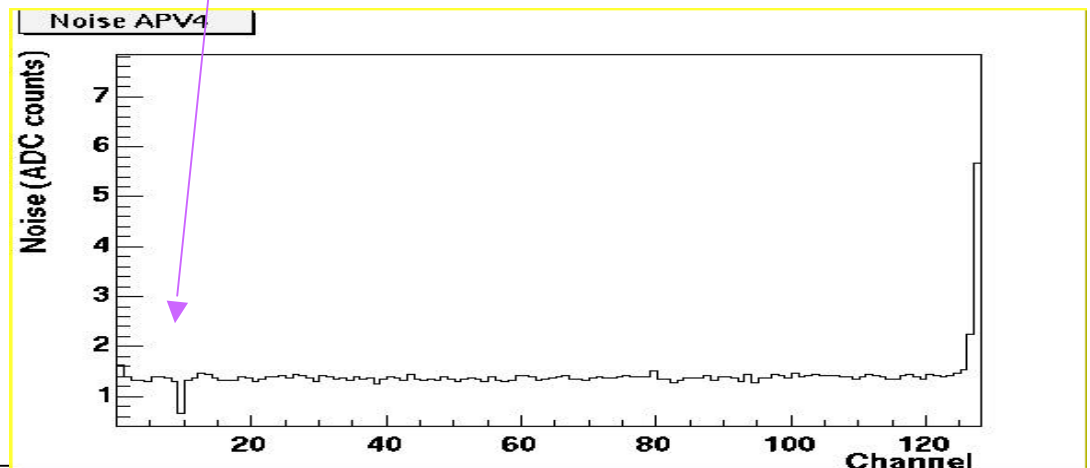
Chip Settings:
I2C.Address= 74
Mode= 43
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IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VEP= 30
VES= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



CMS – like  
no HV



CMS – like  
300V



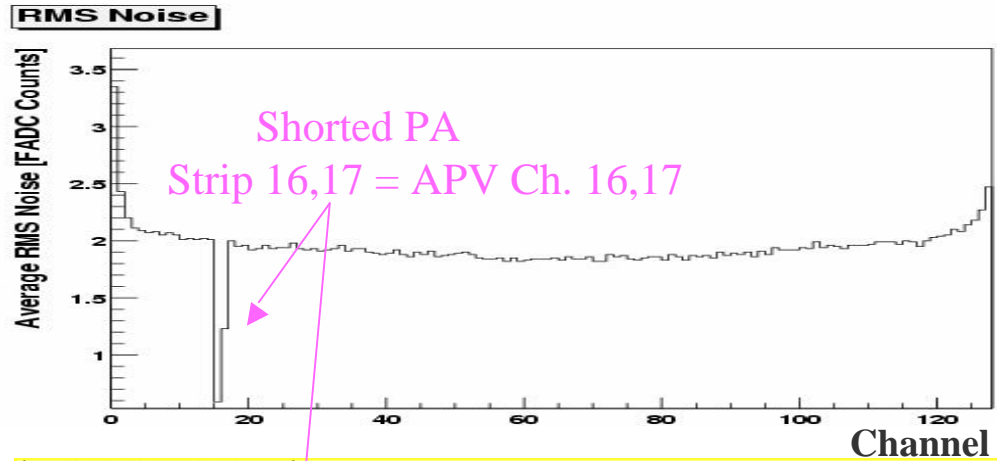


# Noise - TIB002, APV1

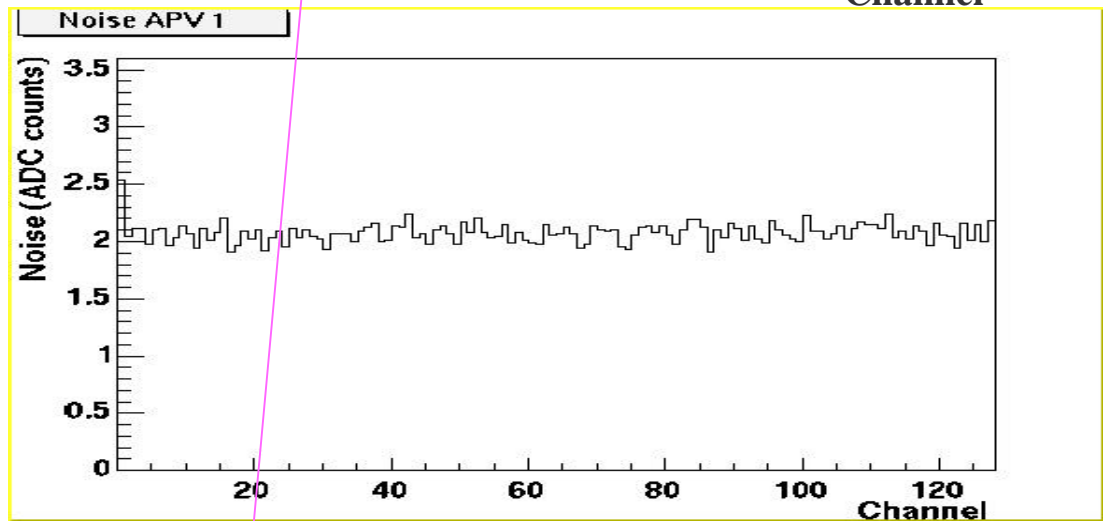
ARC – no HV

```

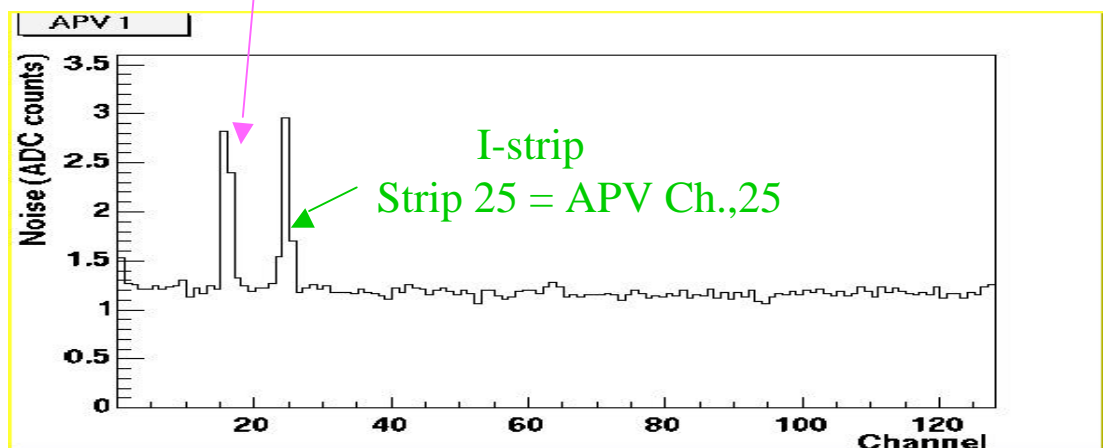
Chip Settings:
I2C.Address= 64
Mode= 43
Latency= 4
IPRE= 98
IPCASC= 52
IPSF= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



CMS – like  
no HV



CMS – like  
450V

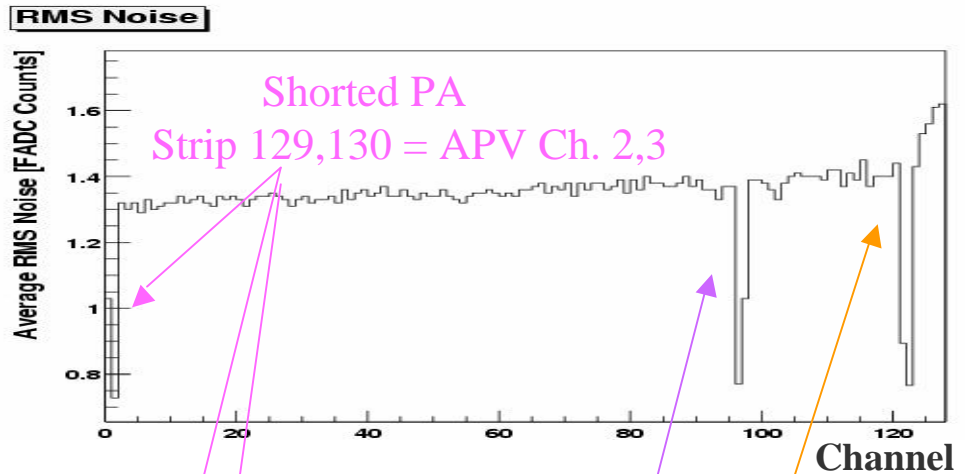


# Noise - TIB002, APV2

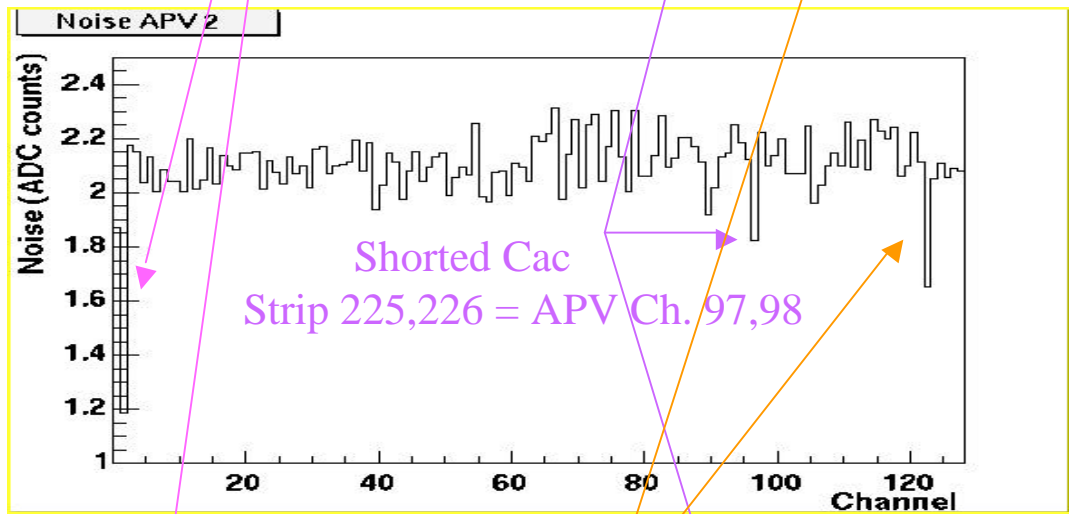
ARC – no HV

```

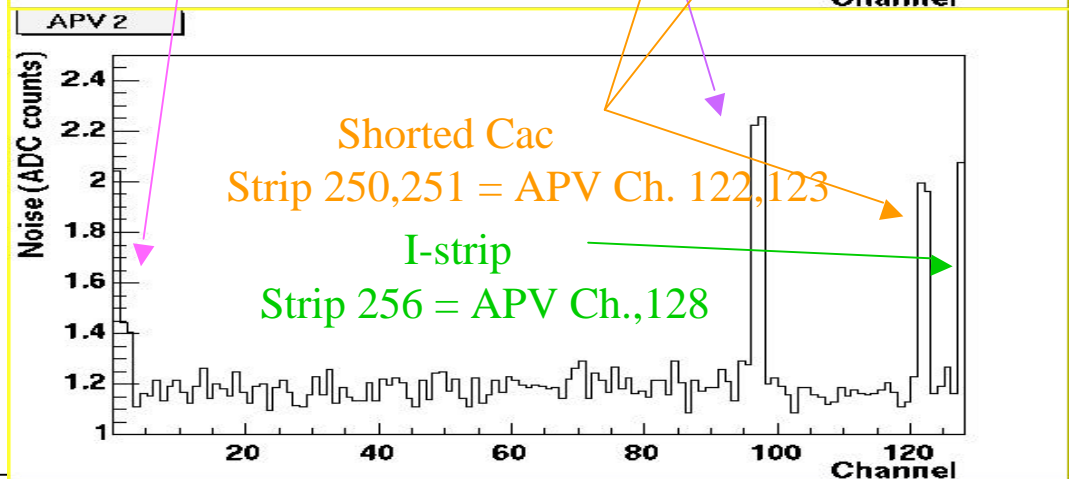
Chip Settings:
I2C.Address= 66
Mode= 43
Latency= 4
IPRE= 98
IPCASC= 52
IPSE= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VFS= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



CMS – like  
no HV



CMS – like  
450V

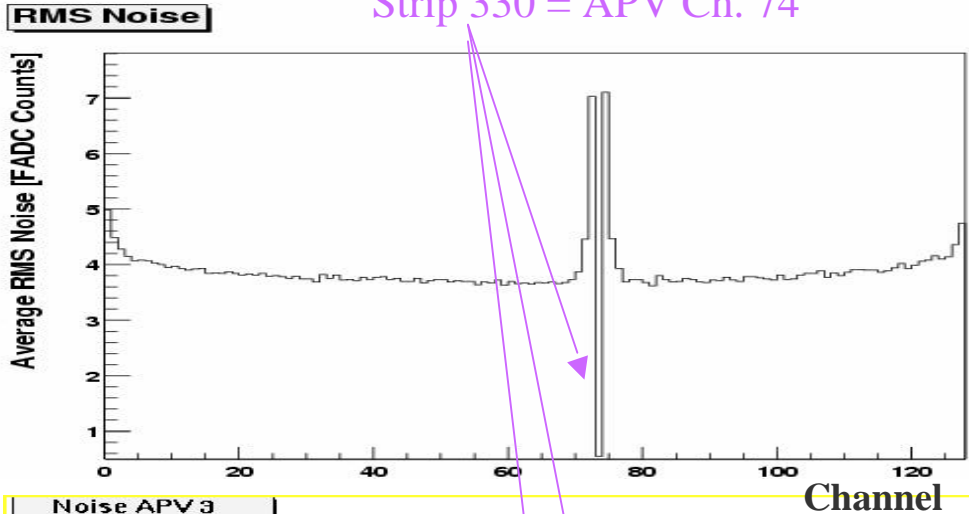


# Noise - TIB002, APV3

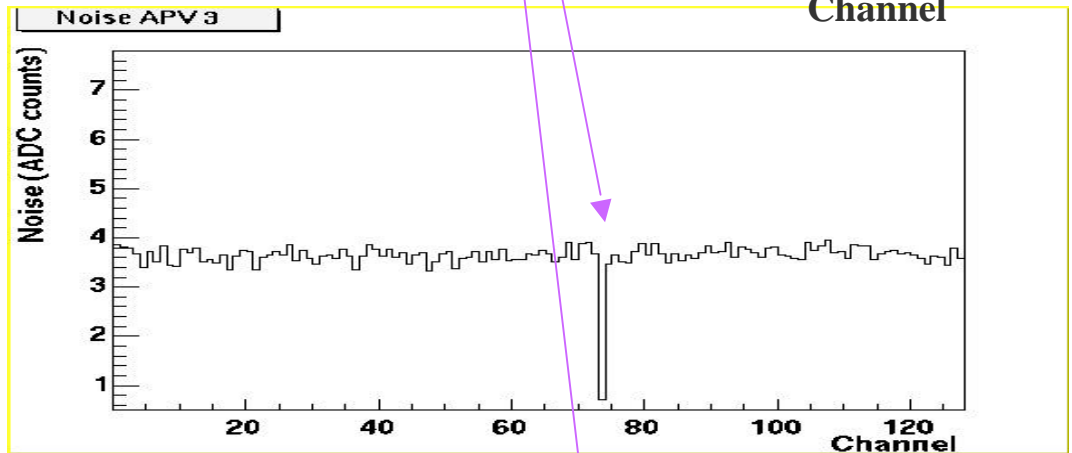
ARC – no HV

```

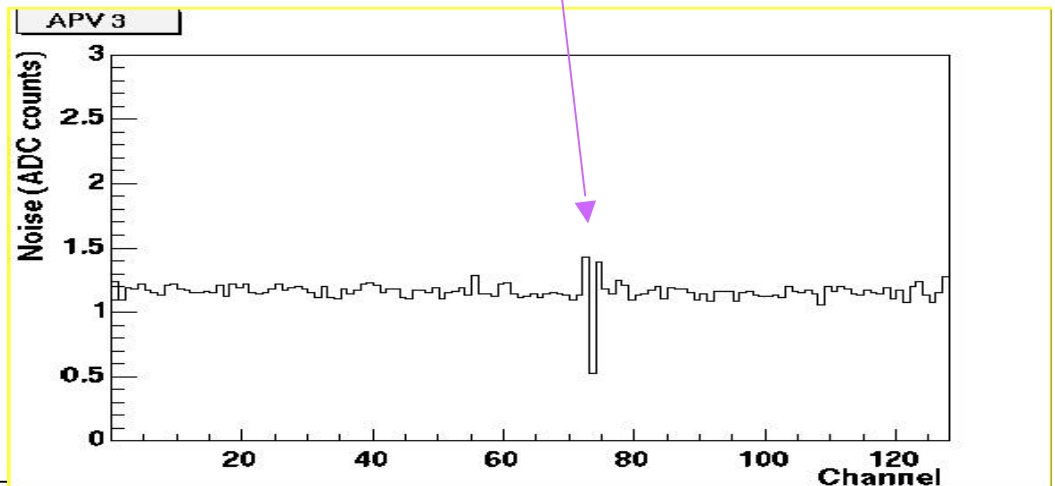
Chip Settings:
I2C.Address= 72
Mode= 43
Latency= 4
IPRE= 98
IPCASC= 52
IPSF= 34
ISHA= 34
ISSF= 34
IPSP= 55
IMUXIN= 34
ISPARE= 0
ICAL= 29
VFP= 30
VES= 60
VSP= 40
CDRV= 254
CSEL= 1
MUXGAIN= 4
Errors= 0
MUX_Res= 3
PLL_1= 1
PLL_2= 0
PLL_3= 127
    
```



CMS – like  
no HV

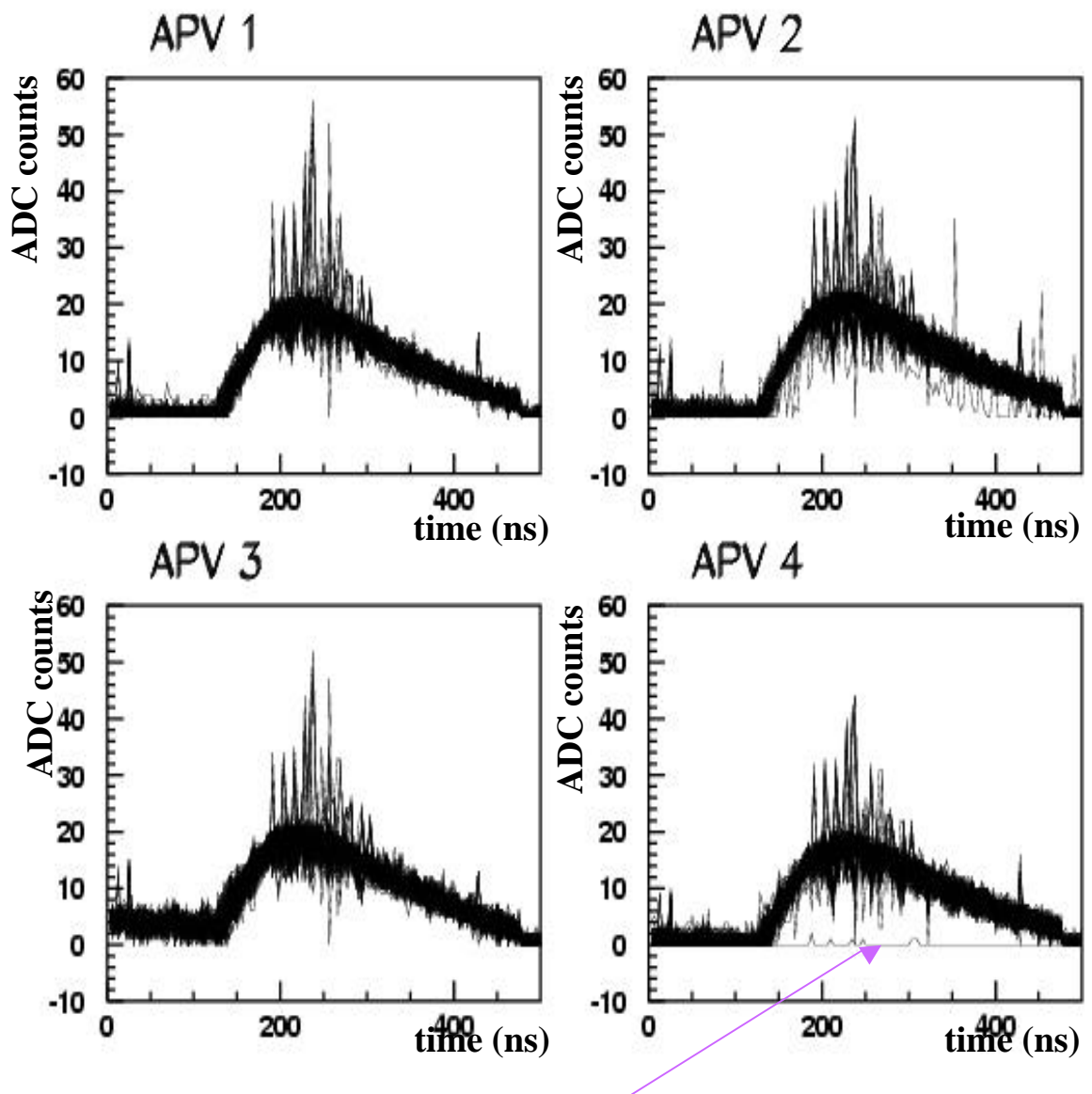


CMS – like  
450V



# Pulse Shape - TIB001

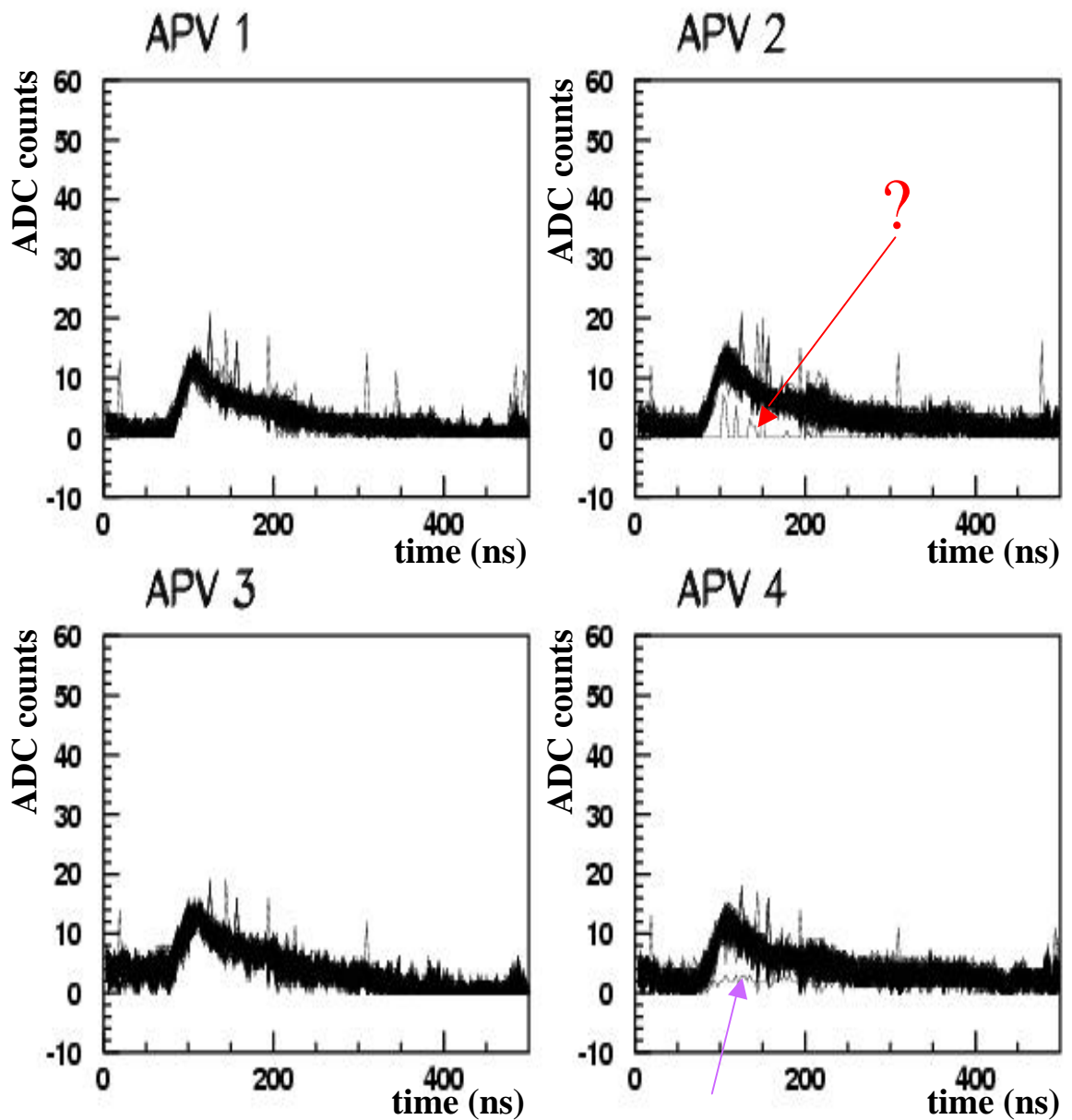
## Peak mode



Strip 394 = APV Ch. 9

# Pulse Shape - TIB001

## Deconvolution mode



Strip 394 = APV Ch. 9

## Conclusions

### ARC system – functionable in Pisa

#### Pedestal

- ✍ Similar structure for both systems

#### Noise

- ✍ APV edges channels – higher noise
- ✍ APV middle channels – similar noise with CMS-like system
- ✍ ARC system finds all defected strips, except high current ones, even without HV bias on sensors

#### Pulse shape

- ✍ generally, as expected
- ✍ additional spikes – to be understood