The CMS Tracker Control System

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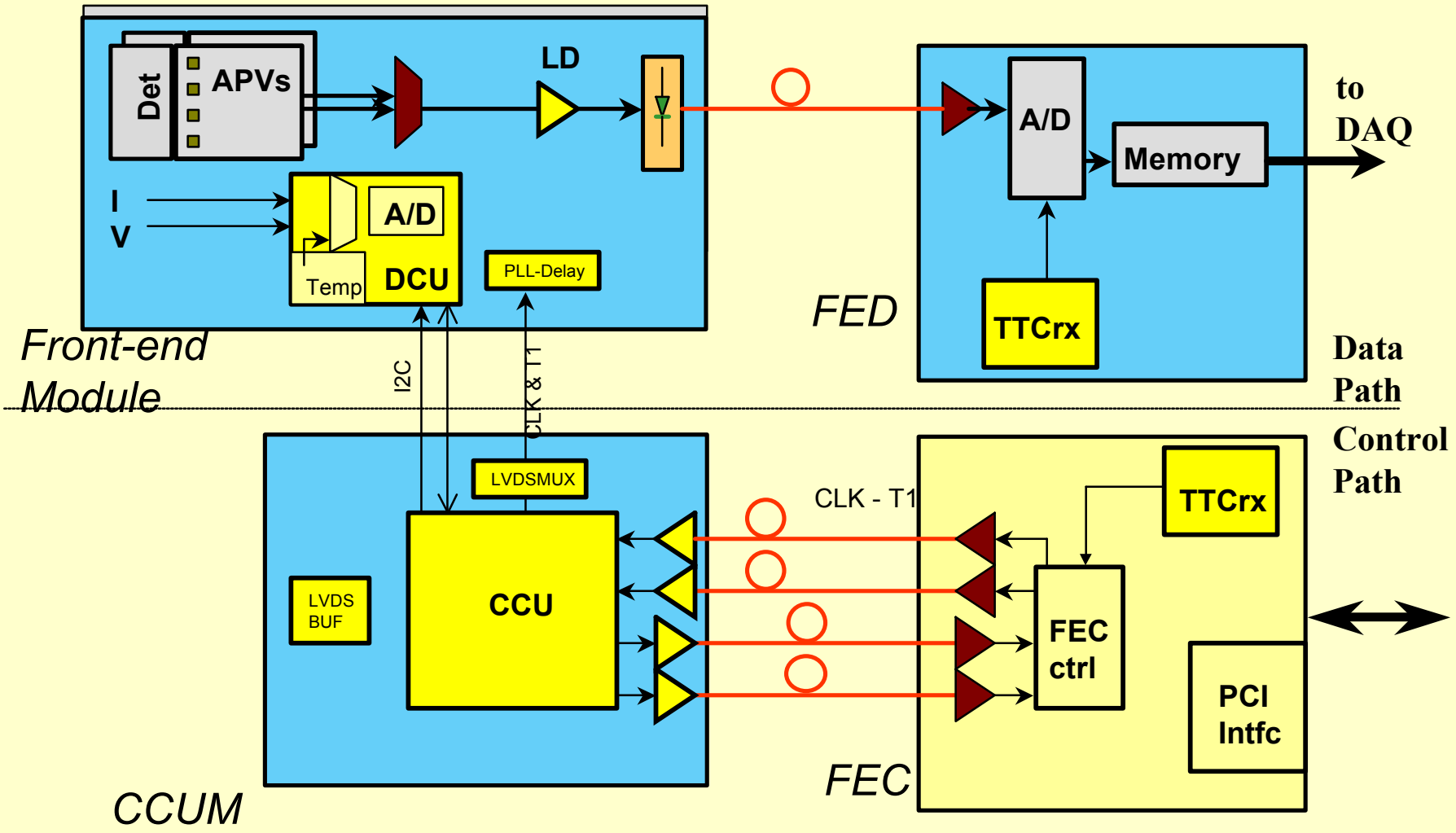
July 4, 2002

Tracker R-O: General Architecture



IC components

- CCU25
- DCU25
- TTCrx-D
- PLL25
- LD
- RX40
- LVDSBUF and LVDSMUX

Cards

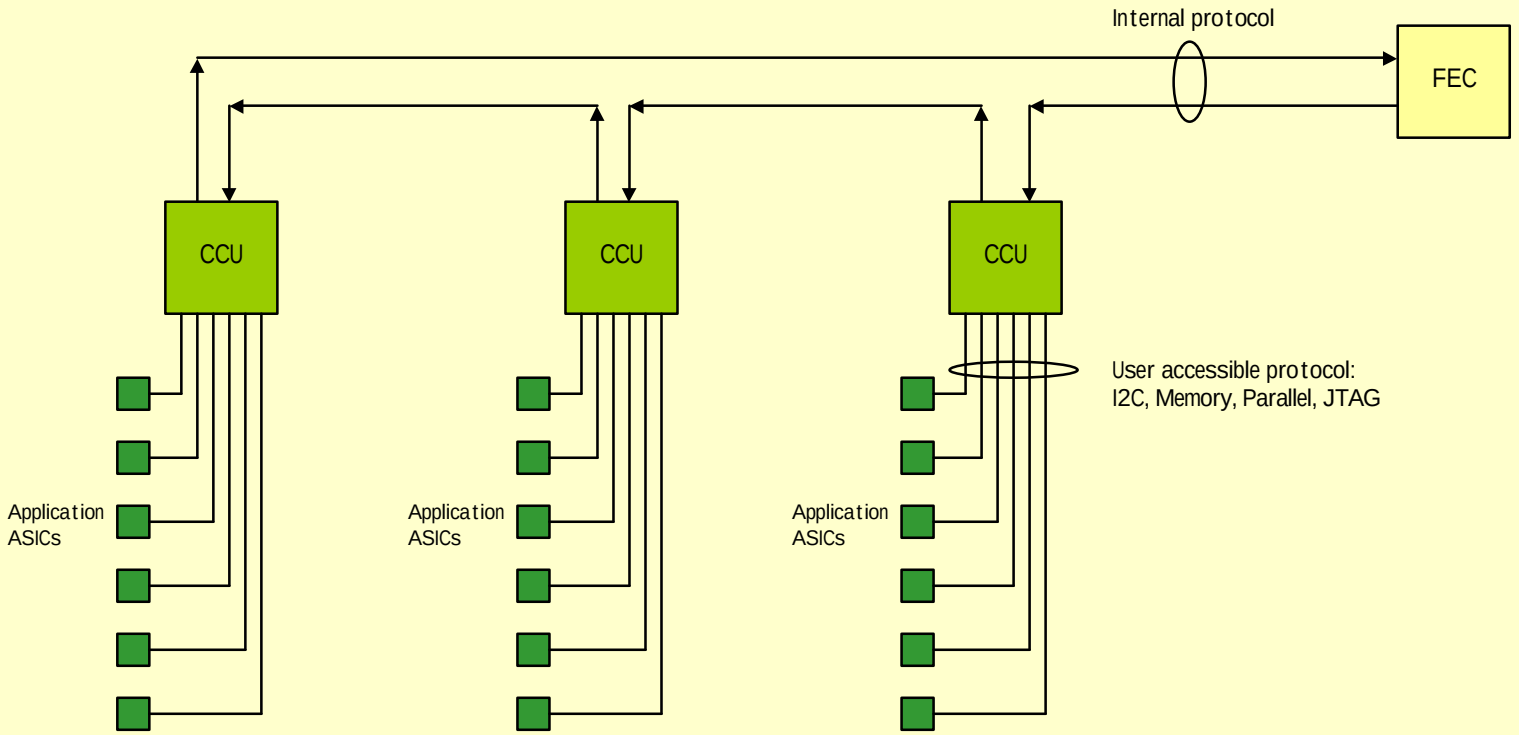
- FEC
- CCUM
- TSC

... for each item

- Hardware
  - Architecture, Functionality and some details of implementation
- Packaging
  - Selected packages
- Software
  - Drivers
  - Development environment
- Documentation

CCU and ring protocol

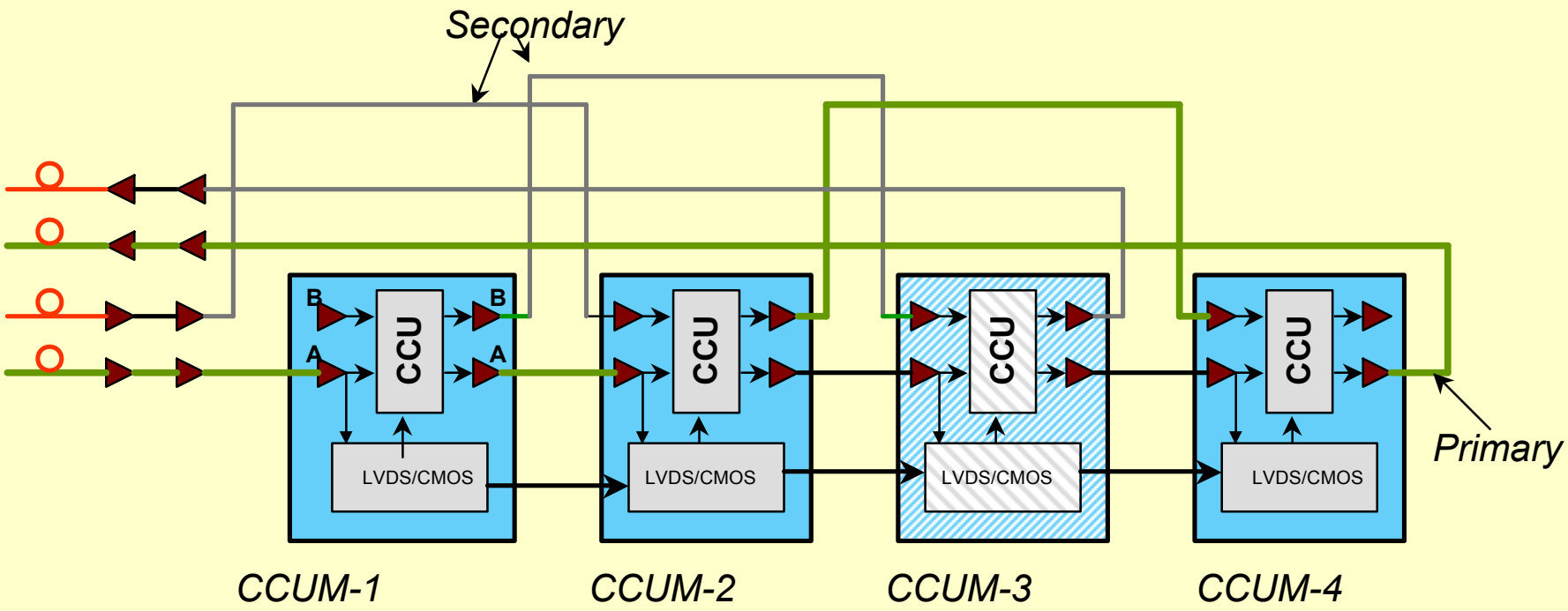
Architecture of Network



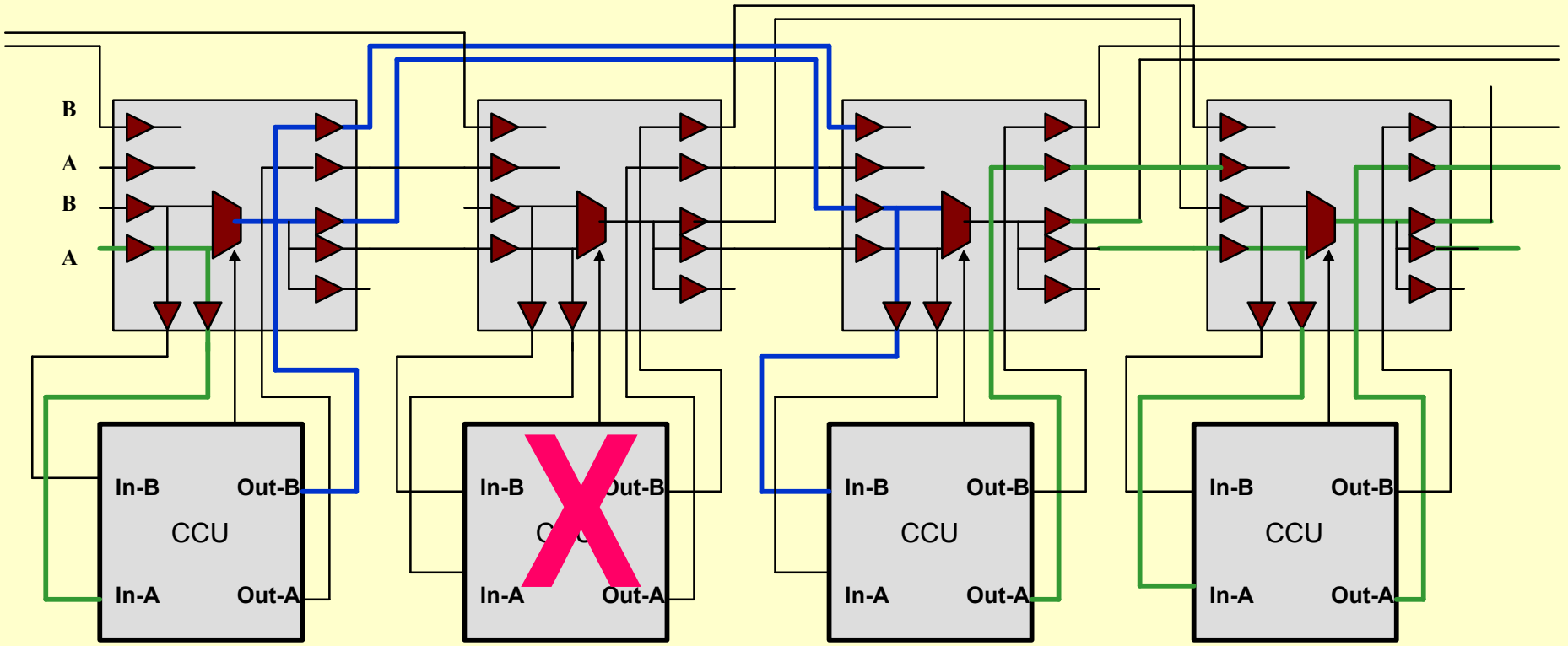
Rationale

- Needed to be able to carry slow control, trigger and timing (40 MHz clock)
- R/W
- As close as possible to a “standard” protocol
- Support for redundancy
- Able to adapt to several protocols of different front-end chips

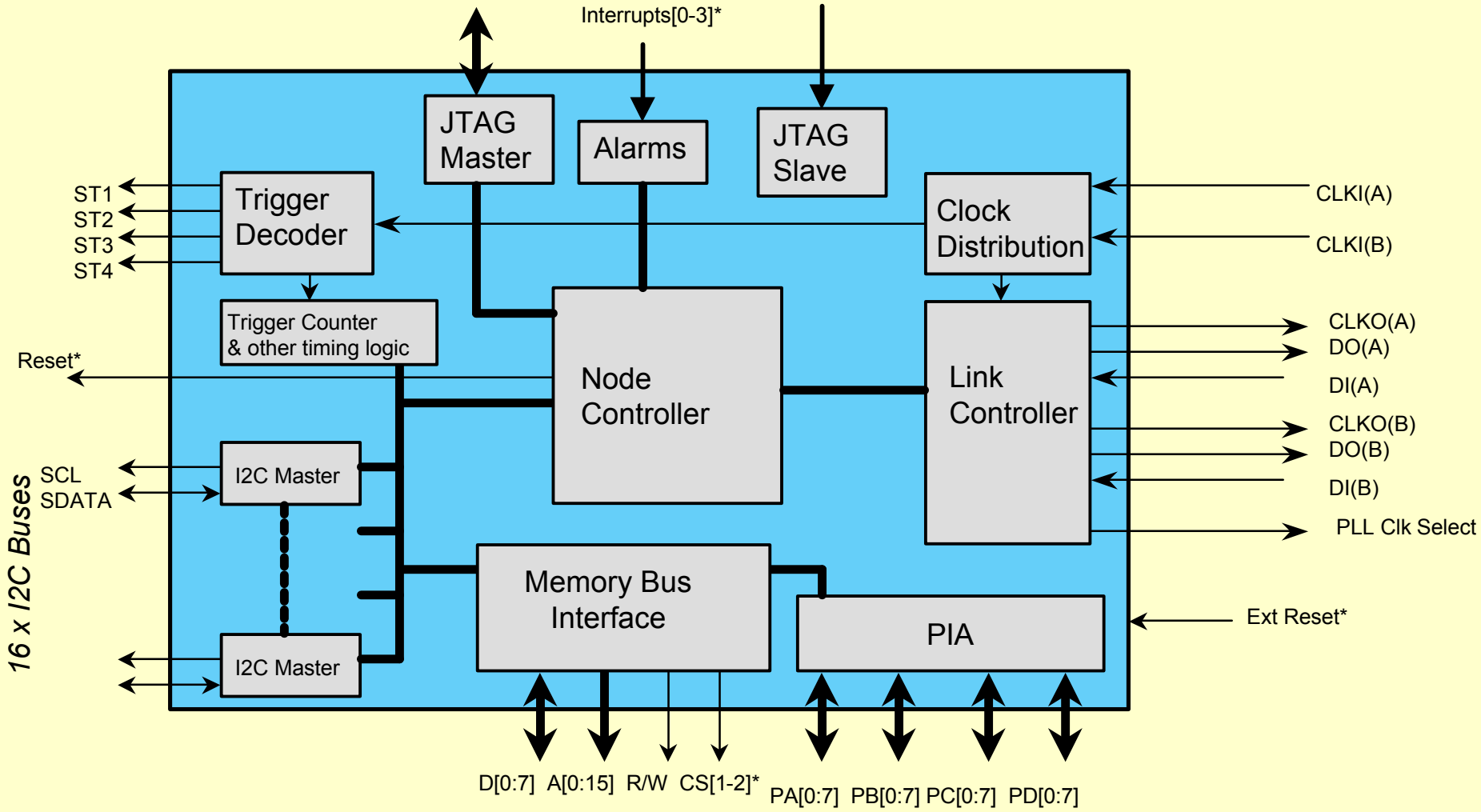
Architecture for Redundancy



CCU-M Cabling with Redundancy (v.5)



CCU: Communication and Control Unit



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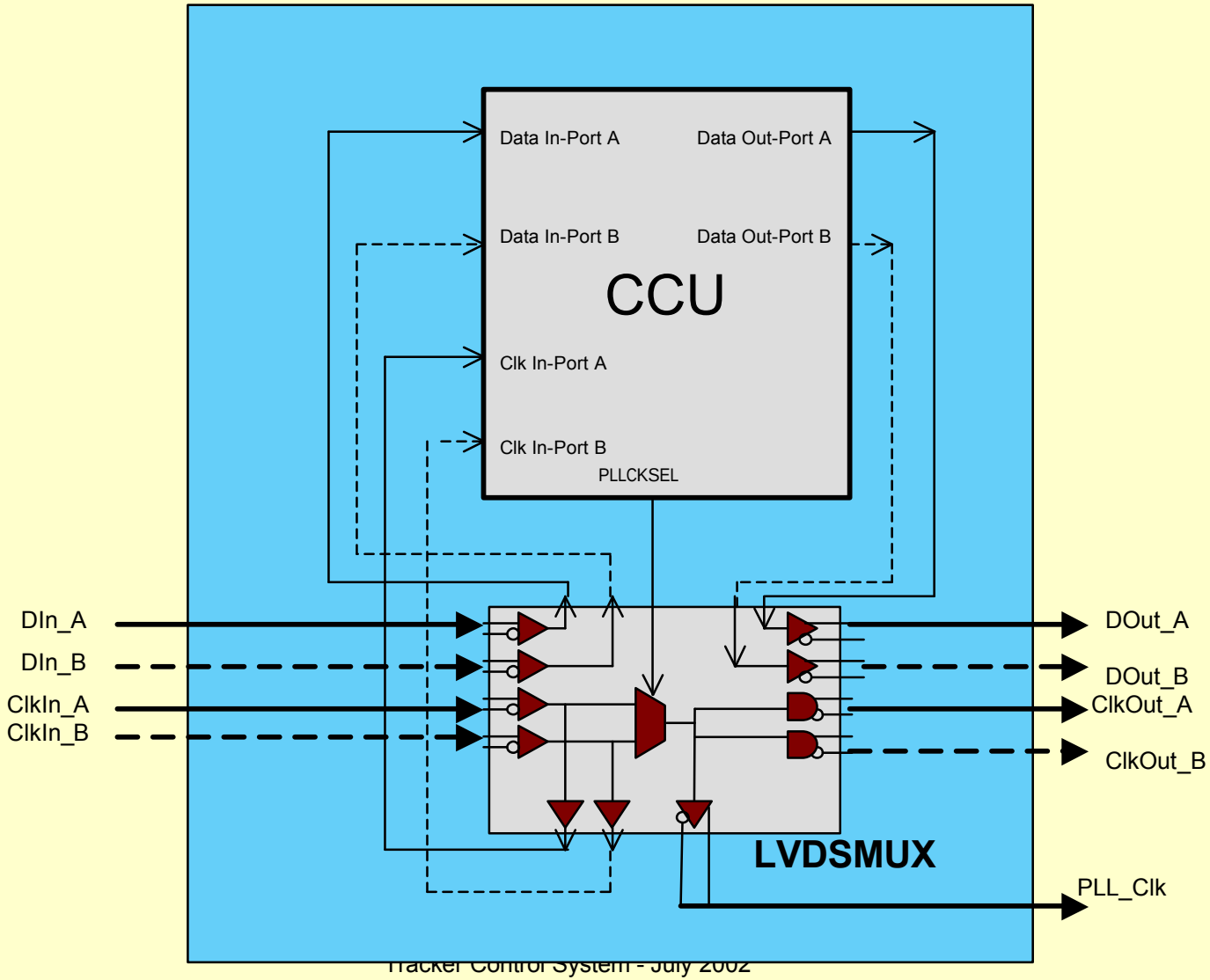
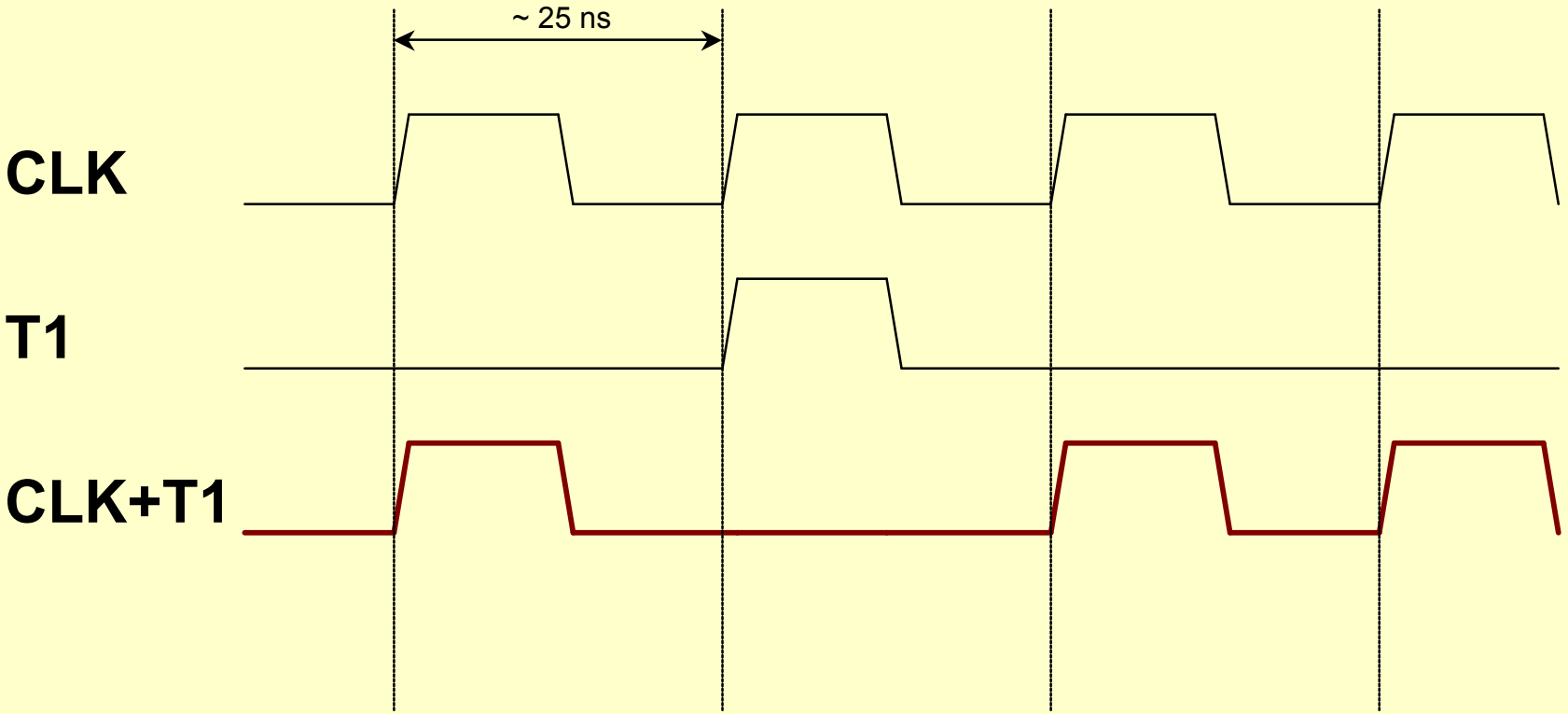
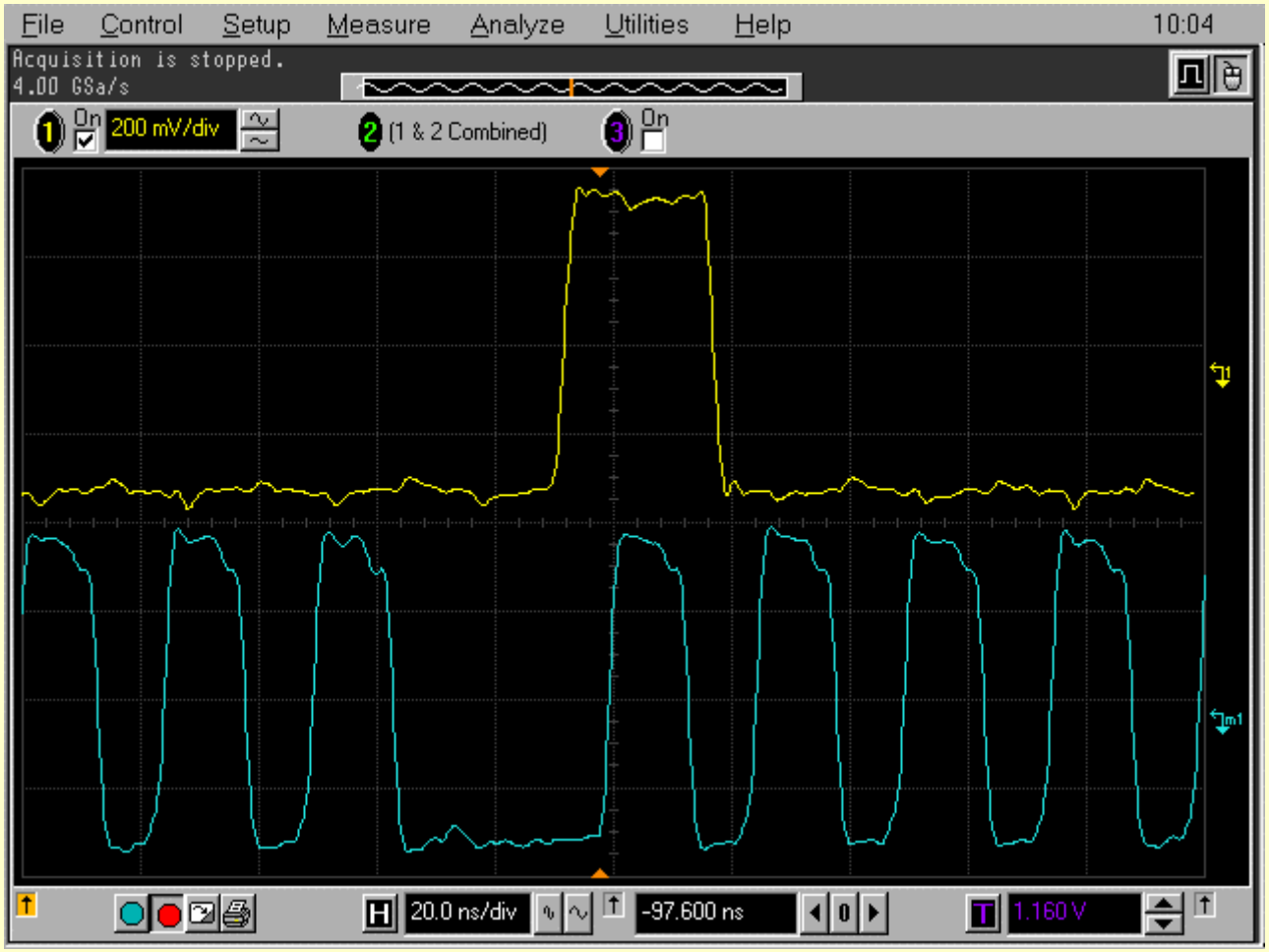


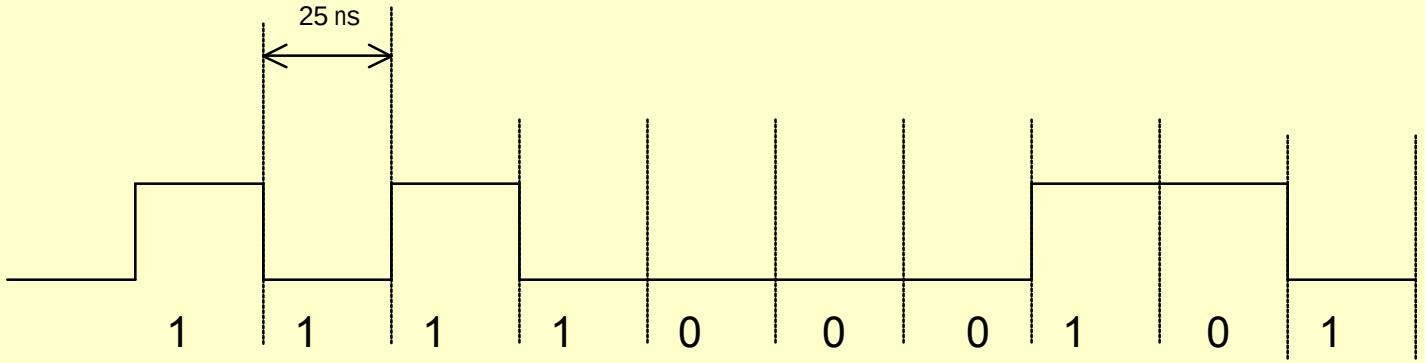
Clock to CCU



Clock to CCU


File Control Setup Measure Analyze Utilities Help 10:04
Acquisition is stopped.
4.00 GSa/s
On 200 mV/div
(1 & 2 Combined)
On
20.0 ns/div
-97.600 ns
1.160 V

NRZI Coding



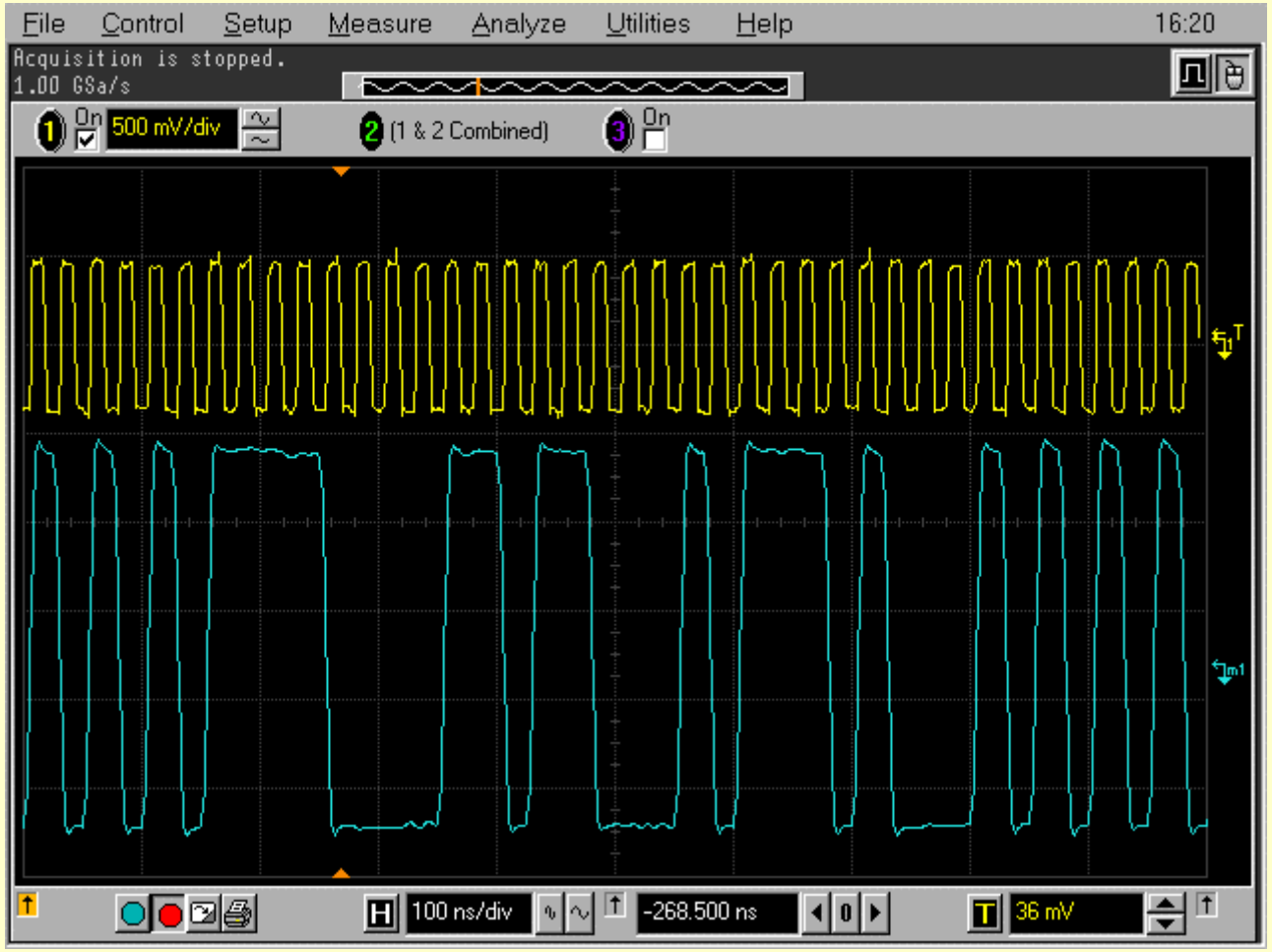
- Non-Return-Zero-Inverted
- 40 Mbit/sec with 20 MHz bandwidth
- “1” signaled by level change
- “0” signaled by no level change

CCU Ring protocol

4 bit Binary	Hex Value	5 bit Symbol
0000	0	11110
0001	1	01001
0010	2	10100
0011	3	10101
0100	4	01010
0101	5	01011
0110	6	01110
0111	7	01111
1000	8	10010
1001	9	10011
1010	A	10110
1011	B	10111
1100	C	11010
1101	D	11011
1110	E	11100
1111	F	11101

Control Symbol	Code	Comment
Idle	11111	Idle
J	11000	In SOF field
K	10001	in SOF field
H	00100	Special
R	00111	Reset
S	11001	Set
T	01101	Termination

Coding on line



Token: “JKTRRR”

LAN Protocol (1)

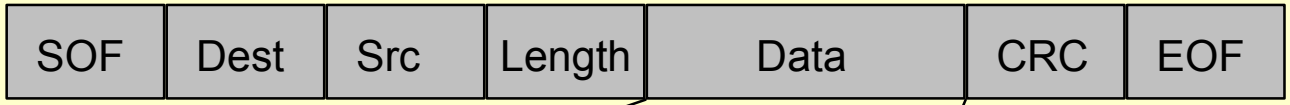
- Ring-like topology
  - Circulating token indicates bus available
  - Source waits for token:
    - » removes token, injects data packet
  - Packet circulates, passed by all nodes
  - Destination copies packet in, sets “S” symbol
  - Packet returns to source, removed by source
  - Source inserts new token

LAN Protocol (2)

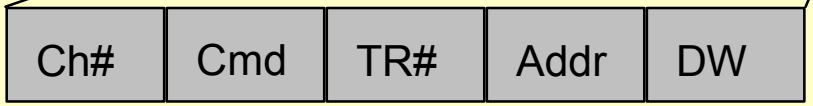
- All nodes can generate packets
- For simplicity:
  - Only FEC can perform network supervision
    - » inserts first token
    - » monitors token integrity
    - » receives all data packets from CCUs
- FEC requires CPU for protocol manag.

LAN protocol: Packet Format

Universal



Channel Specific



(Example for an I2C byte write)

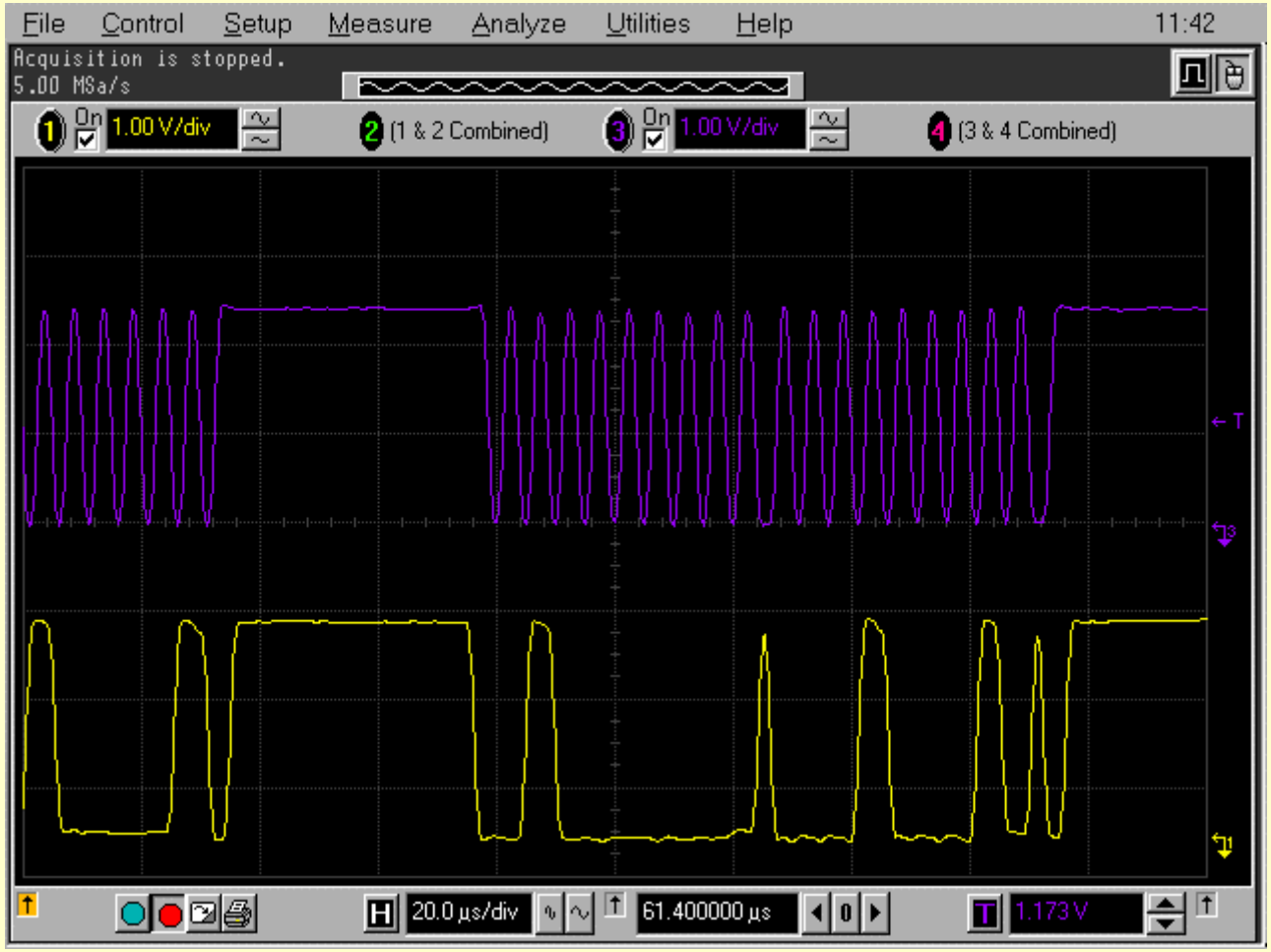
LAN Protocol (3): Transaction example

- Transaction from FEC to CCU
  - FEC sends packet
  - CCU receives packet and sets “S” symbol
  - CCU directs data portion to channel
  - Channel performs action
  - Optional: Channel sends ACK packet to CCU specifying TR#

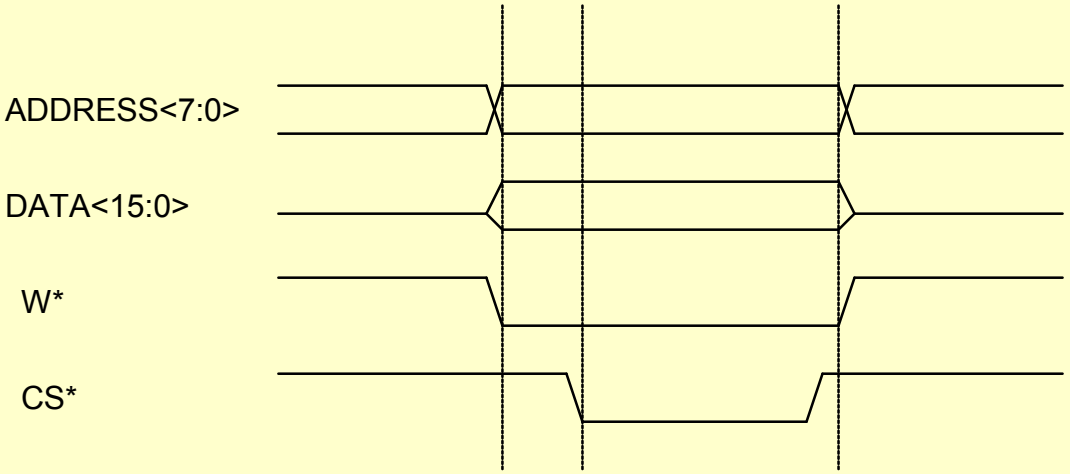
LAN Protocol (4): Addressing

- CCU Address allocation
  - FEC has address “00”
  - Special Broadcast address: “0x80”
  - Up to 127 CCUs on ring
- Channel Addressing
  - 0: CCU Node controller
  - 0x10-0x1f: I2C channels
  - 0x20: I2C broadcast
  - 0x40: Memory channels
  - 0x30-0x33: PIA channel
  - 0x50: Trigger distribution channel
  - 0x60: JTAG master controller
  - 0xfe-oxff: Special interrupt channel

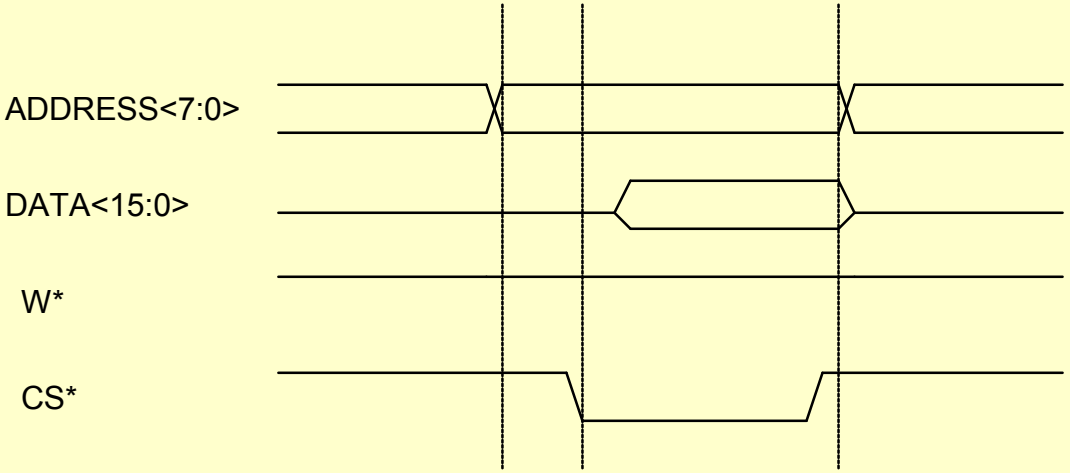
I2C Protocol (back-to-back @ 100KHz)



CCU25 – Memory protocol



Write cycle



Read cycle

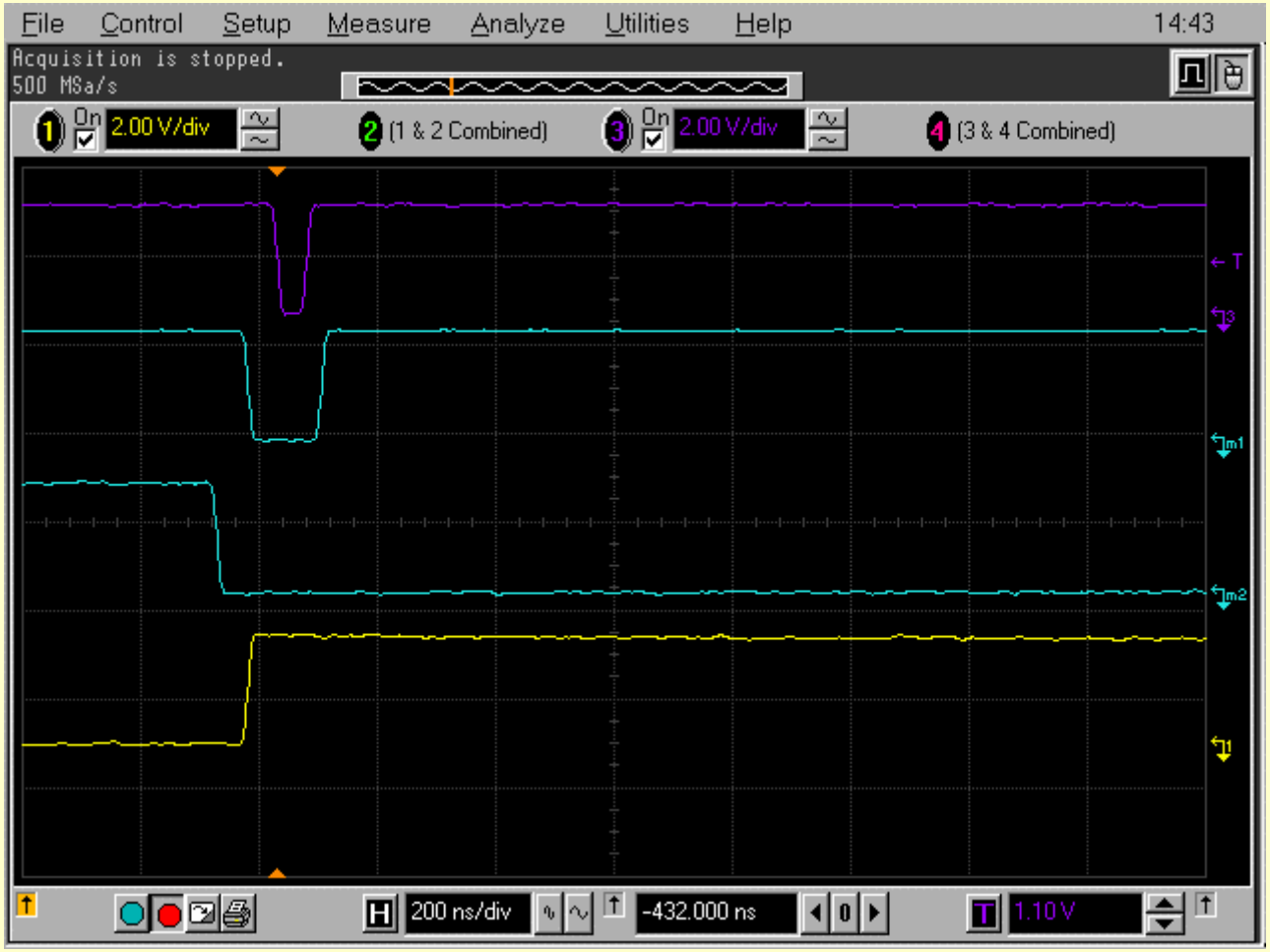
Memory transfer

CS*

RW*

Address

Data



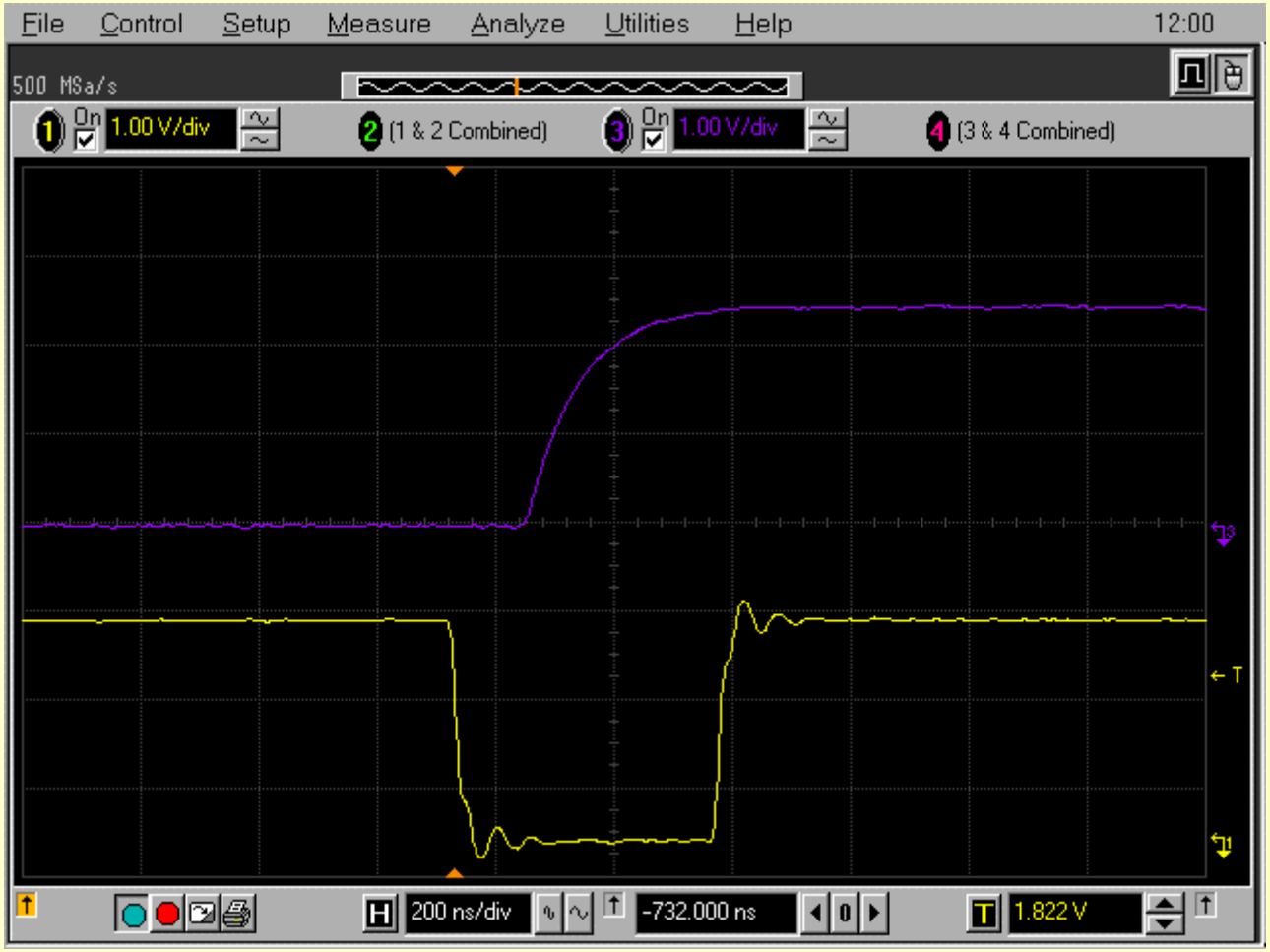
Parallel Port Protocol

- 4 8-bit bi-directional ports per CCU
- Architecture like Motorola PIA
  - 8 Programmable direction data lines
  - 1 input strobe
  - 1 output strobe

PIA port after Reset

I/O line changing direction

Reset to CCU

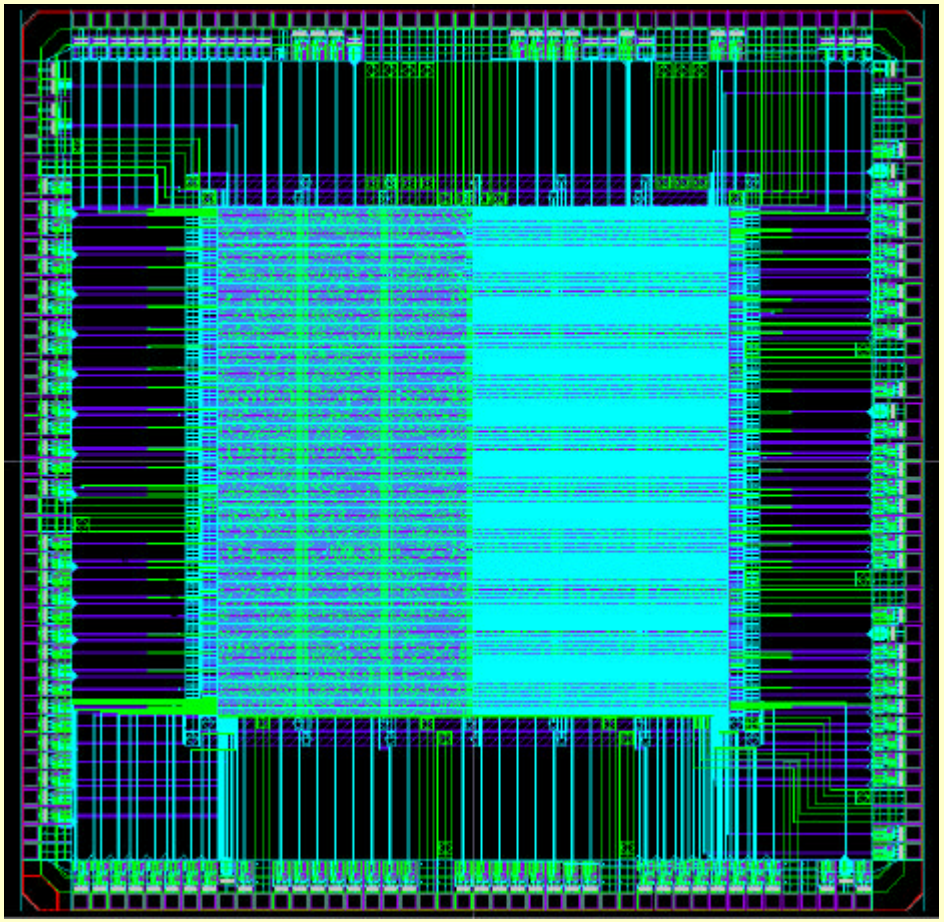


JTAG Master port

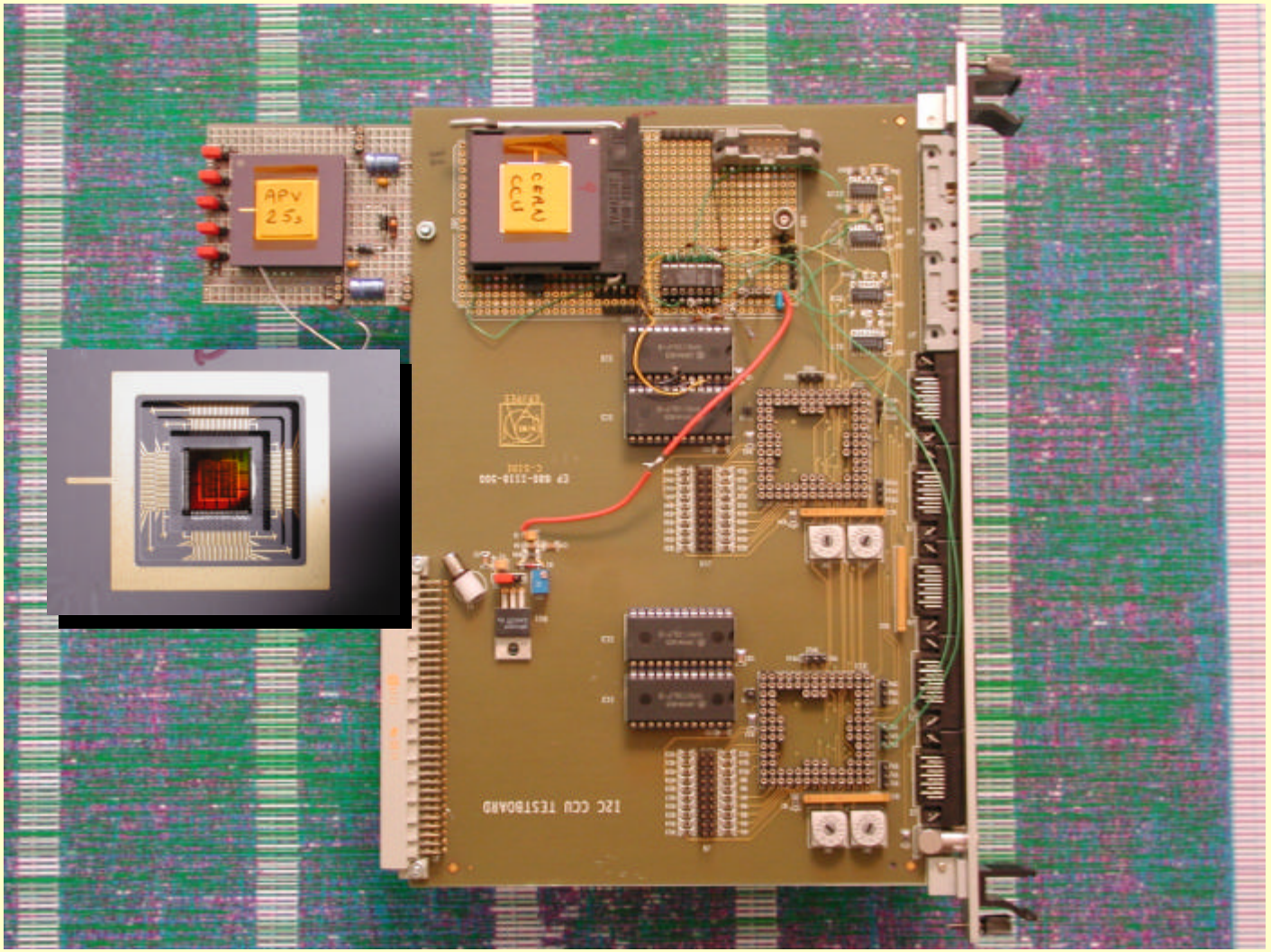
- Simple master port
- Limited intelligence on controller
- Entire JTAG sequence programmed from FEC
- Need special ring packet
- Need special software support from FEC

CCU25 in 0.25 µm

- Features
  - 6.3x6.3 mm^2, 3 metals
  - Fully synthesized (Synopsys)
  - Three independent clock trees
  - Pad-Limited
  - Slew rate limited IO pads
  - I_{DD} = 100 mA @ 2.5V
  - 196 pin fpBGA array 14x14 with 1 mm pitch

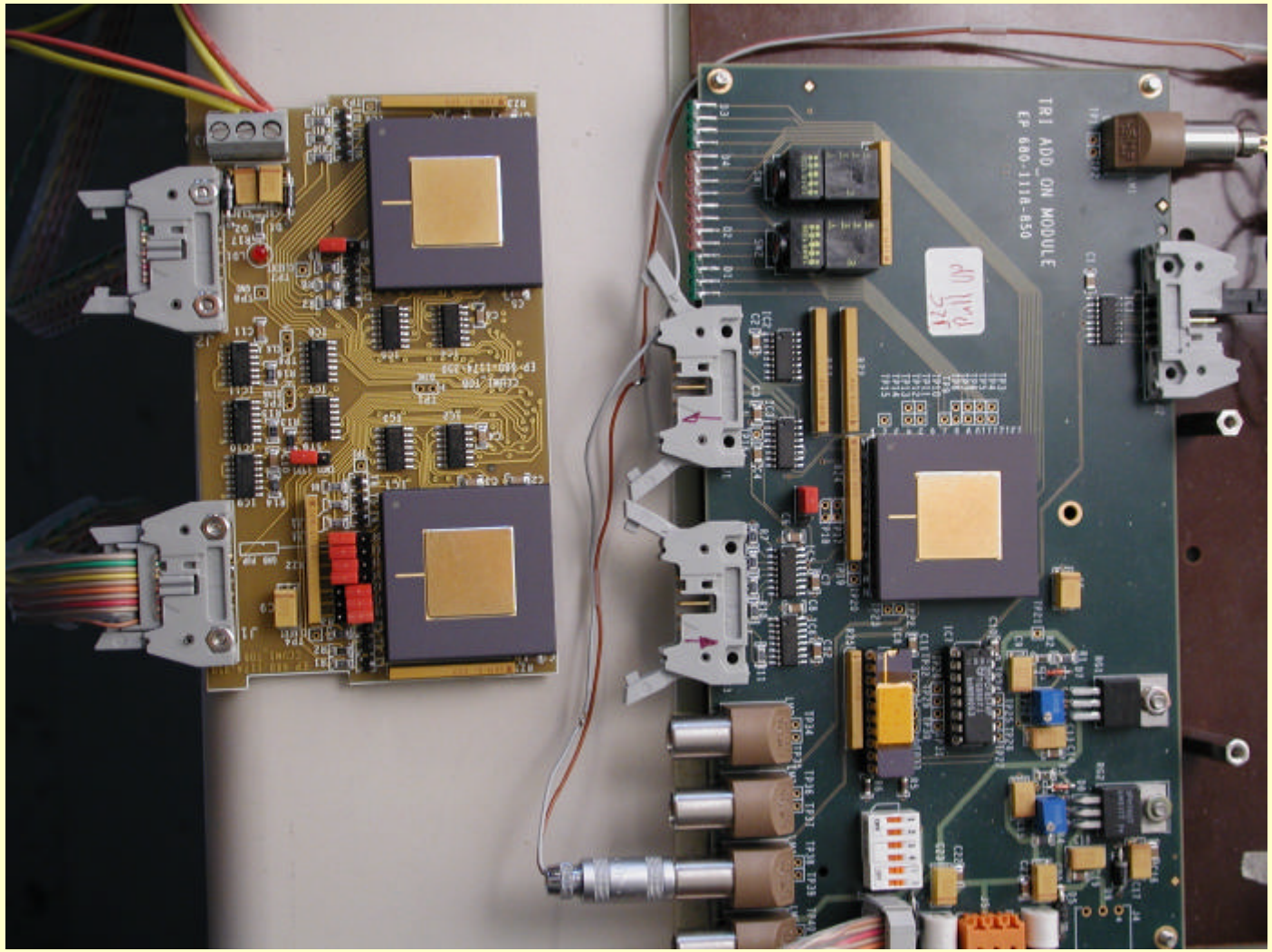


CCU25-Proto card



A.Marchioro /EP

CCUM with 12 I2C channels for ROD proto



CCU25 redundancy features for SEU

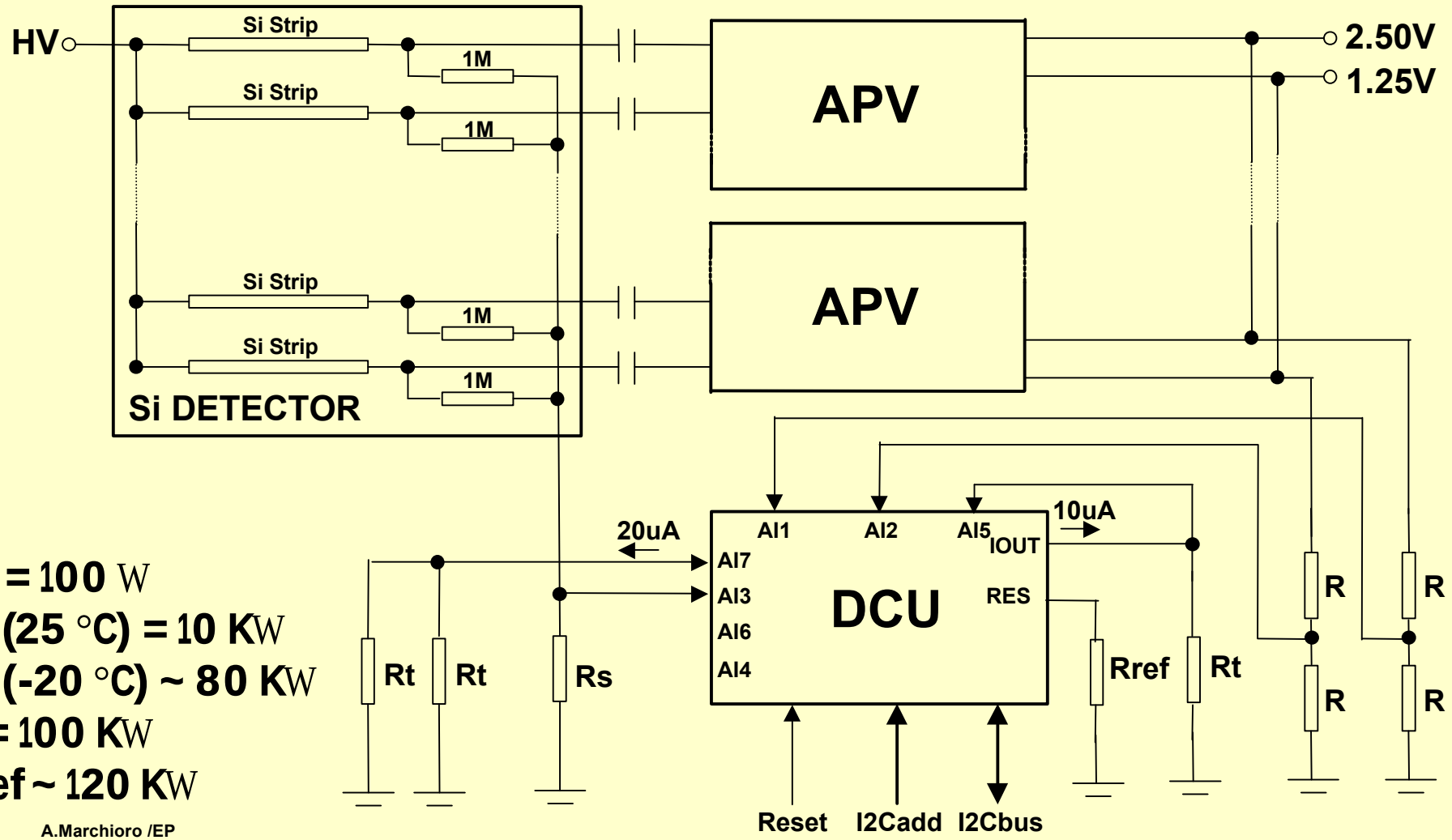
- Node controller: 3 x logic + voting
- Data path: parity on all registers
- Control FSM: One-Hot + Auto-Reset
- Several status SEU registers + counters

DCU

Monitoring with DCU

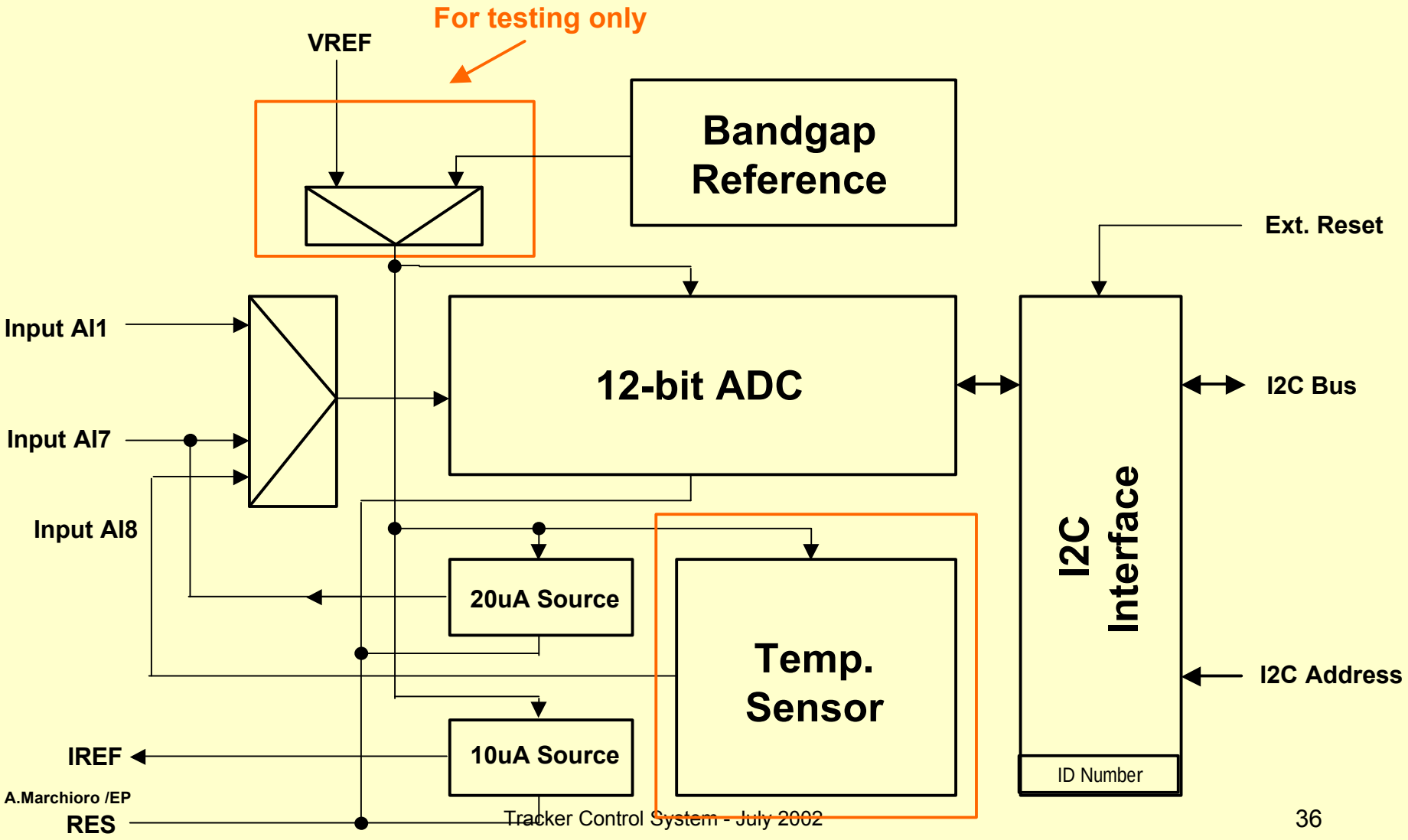
- Detector Control Unit
  - Generic Voltage, Current and Temperature Monitoring
  - 12 bit Analog to Digital Converter
  - I2C Interface
  - Rad-Tolerant
  - Low-Power

Detector Monitoring



Rs = 100 W
Rt (25 °C) = 10 KW
Rt (-20 °C) ~ 80 KW
R = 100 KW
Rref ~ 120 KW

DCU Architecture

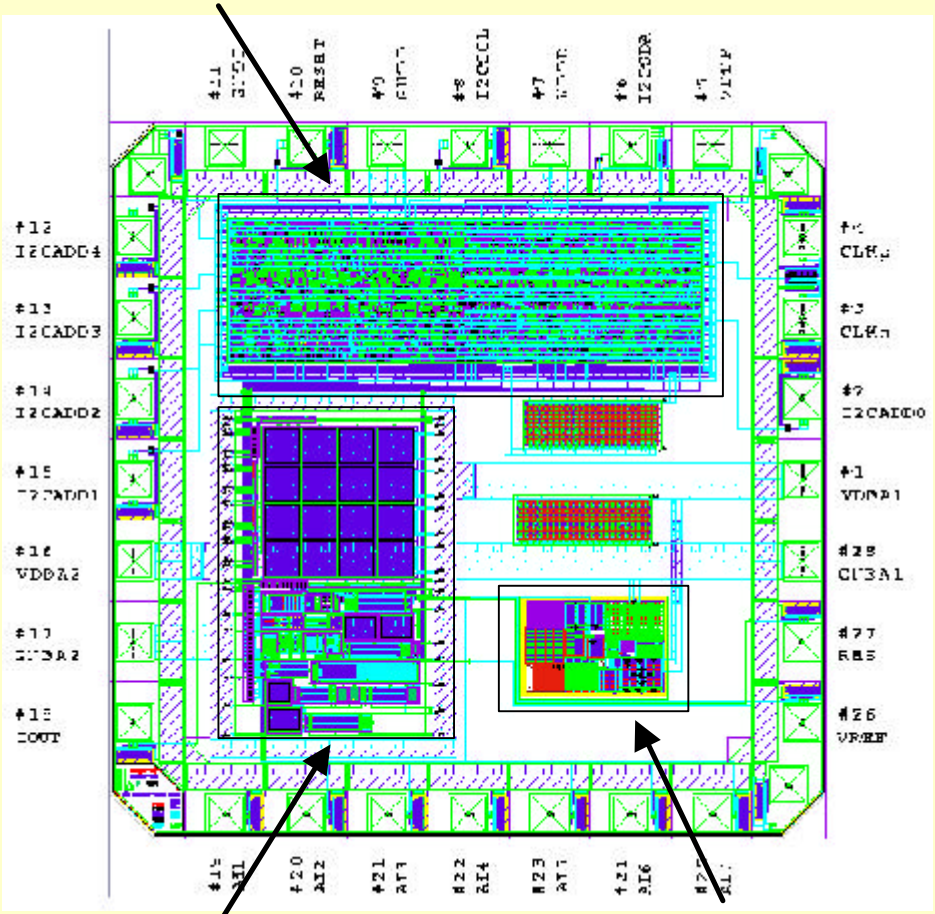


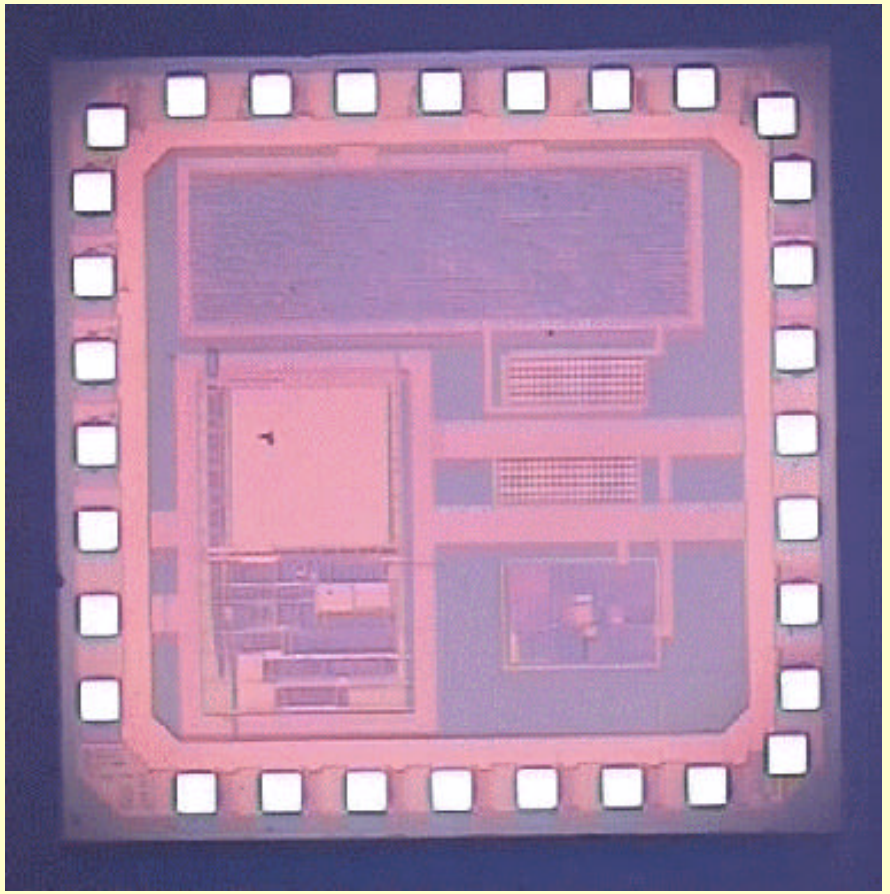
I2C Registers

- Internal addresses:
  - ***Control Register* CREG** (r/w - reg_add = 000)
    - » CREG[2:0] ⇒ select the ADC input channel
    - » CREG[3] ⇒ selects the ADC operating mode
    - » CREG[6] ⇒ performs a “software” reset (an external reset pin is also provided)
    - » CREG[7] ⇒ starts an ADC acquisition
  - ***Status & Data High Register* SHREG** (read only - reg_add = 001)
    - » SHREG[3:0] ⇒ The 4 MSBs of the result of the last ADC acquisition
    - » SHREG[6] ⇒ A majority error (SEU) occurred
    - » SHREG[7] ⇒ The DCU is in the IDLE state
  - ***Data Low Register* LREG** (read only - reg_add = 011)
    - » LREG[7:0] ⇒ The 8 LSBs of the result of the last acquisition
  - ***Auxiliary Test Register* AREG** (r/w - reg_add = 010) [DO NOT USE !]
  - ***Test Register* TREG** (r/w - reg_add = 100) [DO NOT USE !]
  - ***ID Registers*** (read only - reg_add = 111-110-101)
    - » ***Unique 24-bit serial number in each chip***

DCU Layout (proto 1)

ADC digital blocks & I2C interface

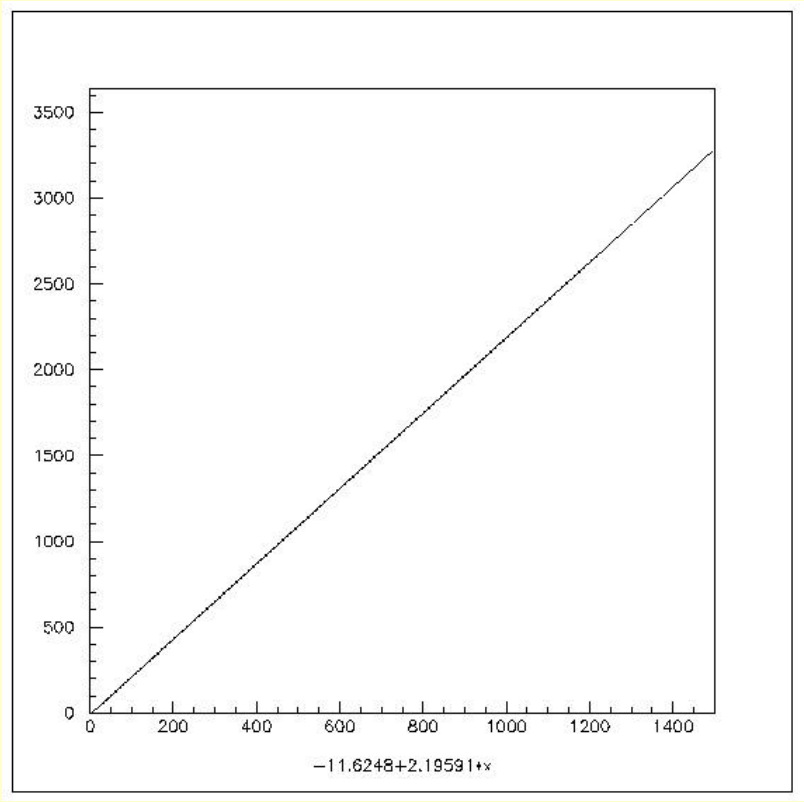


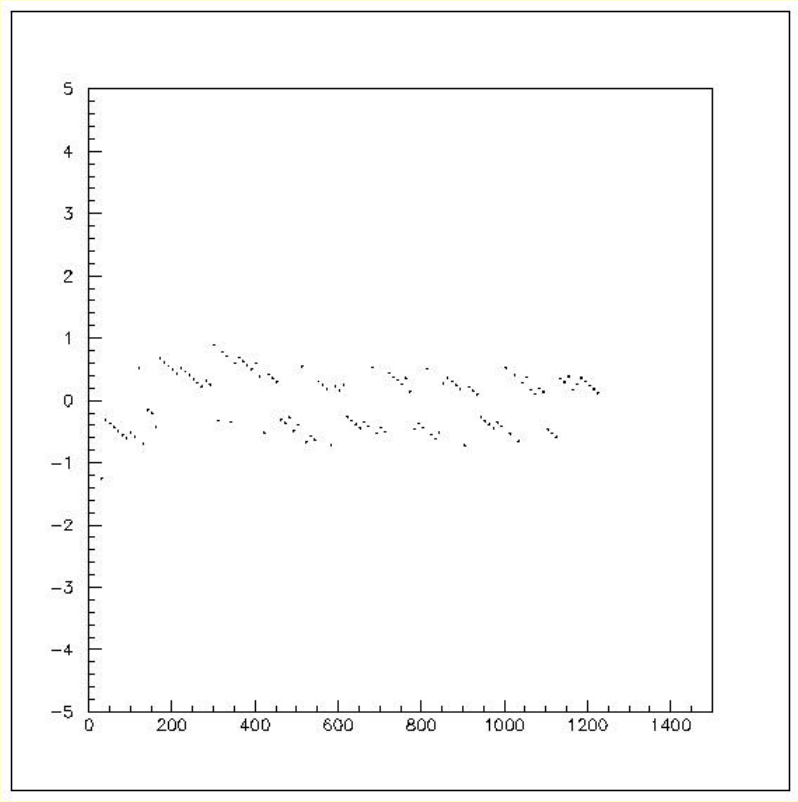


ADC analog blocks

Bandgap

ADC Test Results (1)



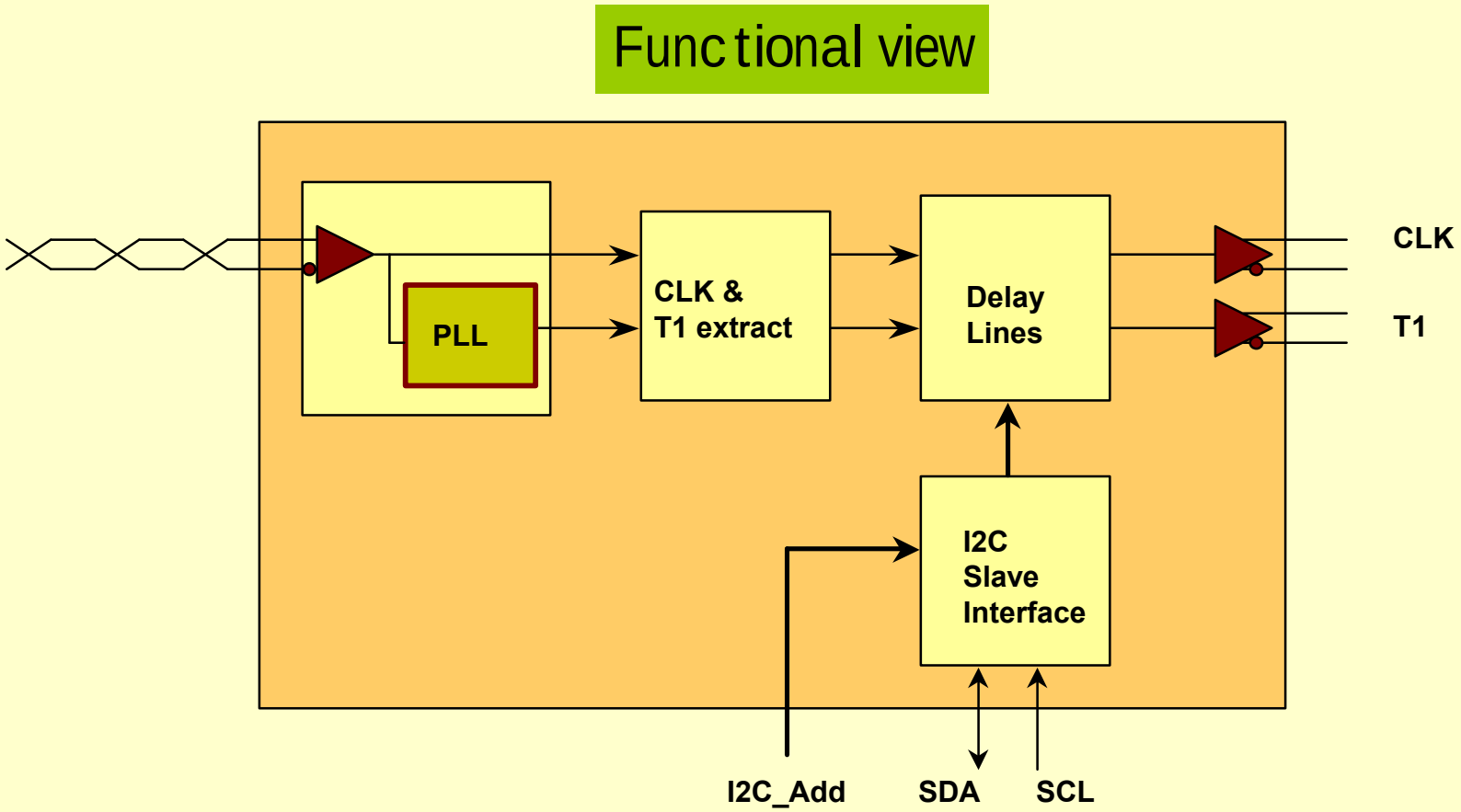


- Gain ~ 454 mV/LSB
- -1LSB < INL < 1LSB

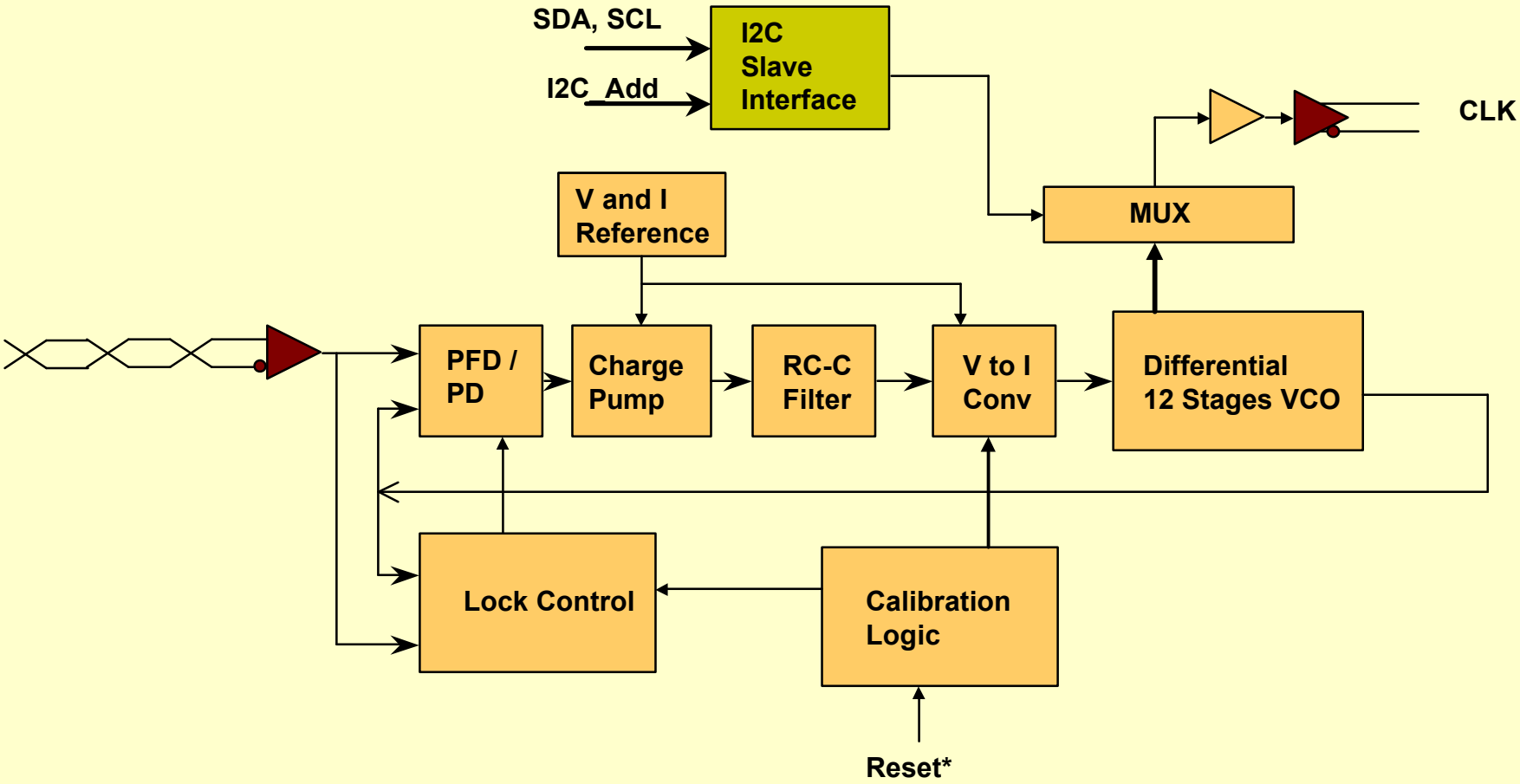
ADC Gain and INL ("low input range" mode: 128 input voltages in the range GND < Vin < 1.25V)

PLL

Timing Distribution PLL-Delay chip



PLL25 Detailed architecture

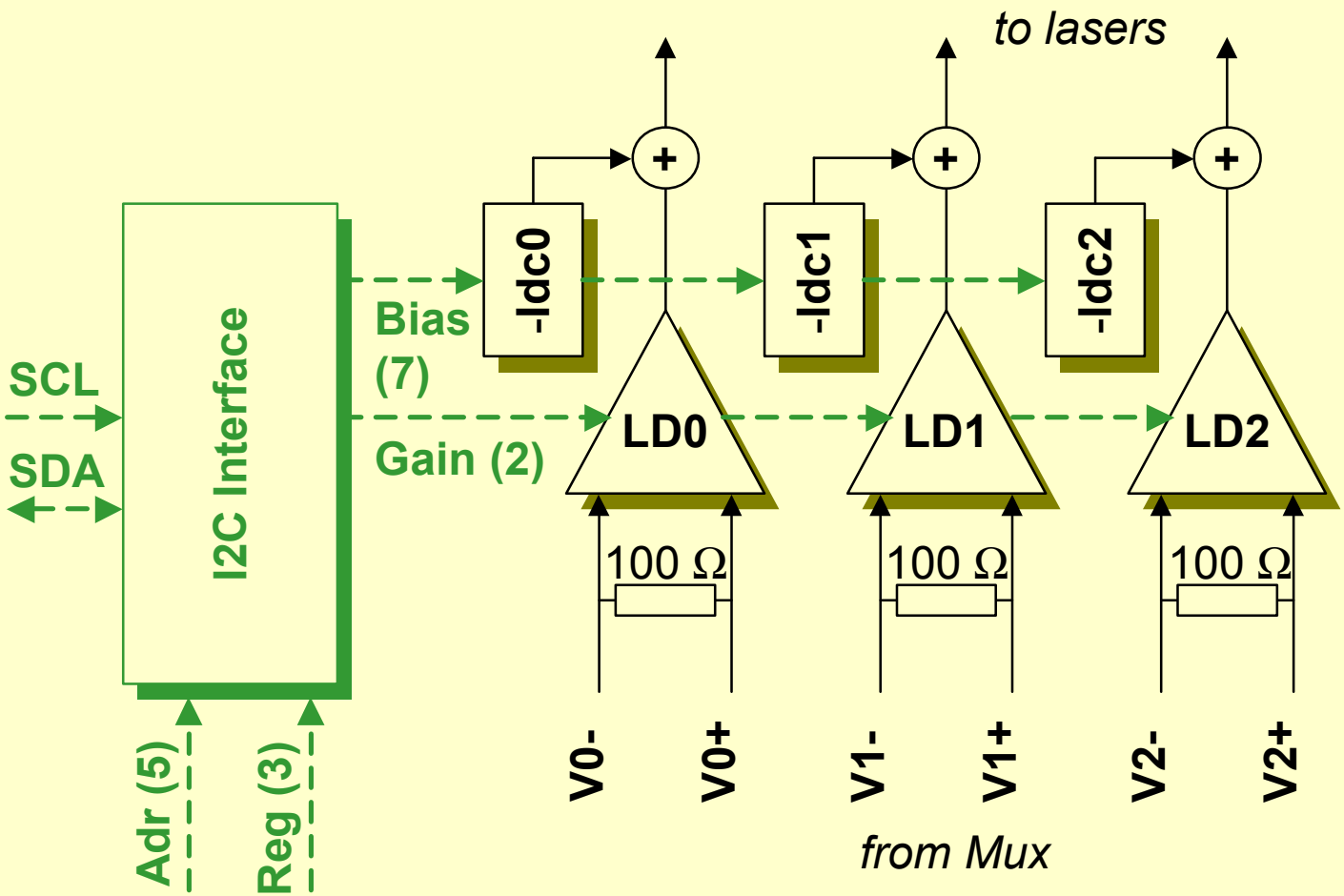


On Resets

- Power-on and master Reset is distributed with CMOS (valid low) level from the Digital Opto-Hybrid
- Tracker uses “101” sequence for re-synchronization
- At the moment the FEC ignores “channel B”
  - Mod is under consideration, please advice!

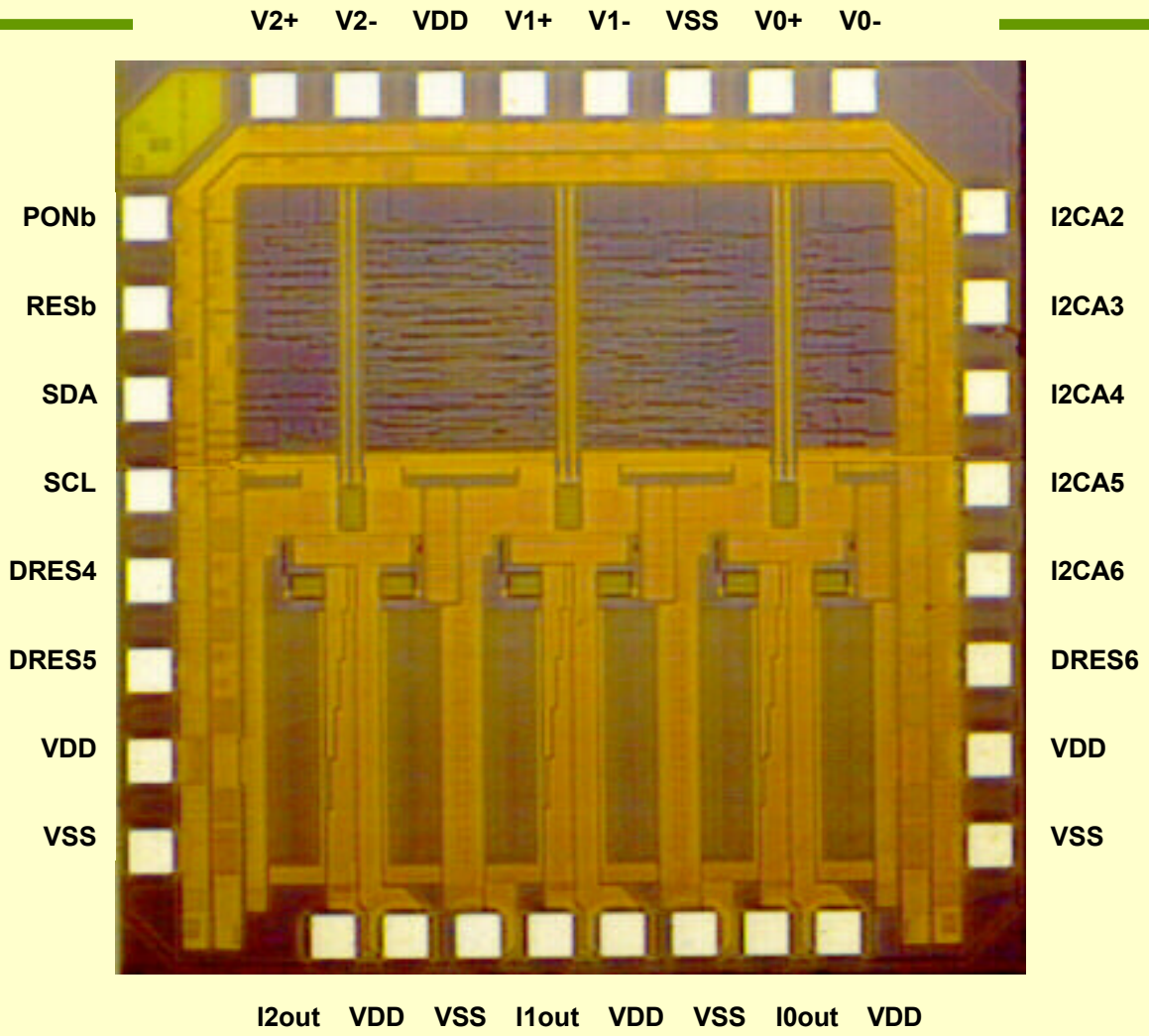
LLD

Linear Laser Driver: Block Diagram



•**MANUAL / DATASHEET: available on http://cern.ch/proj-lld**

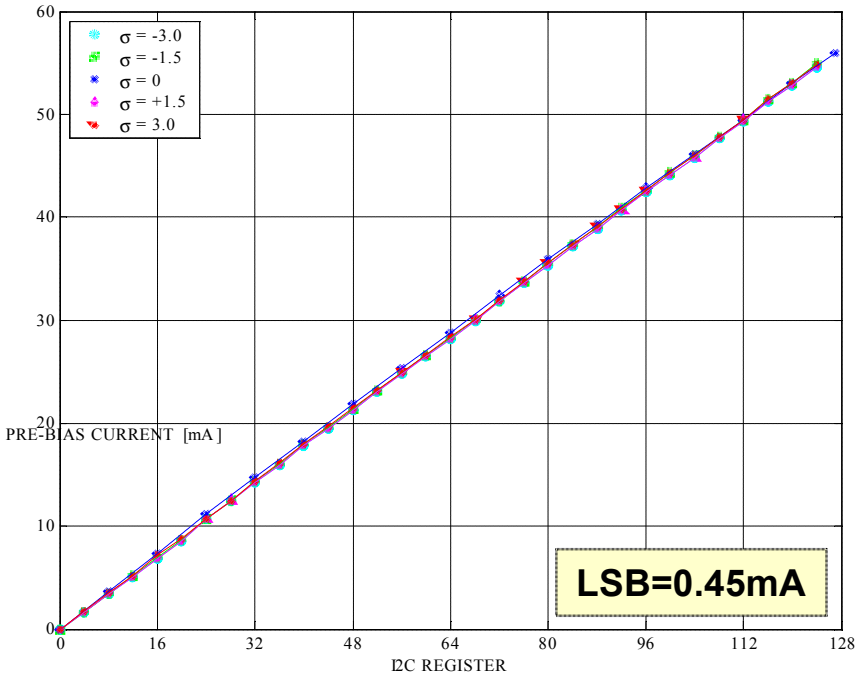
Linear Laser Driver (LLD): Layout



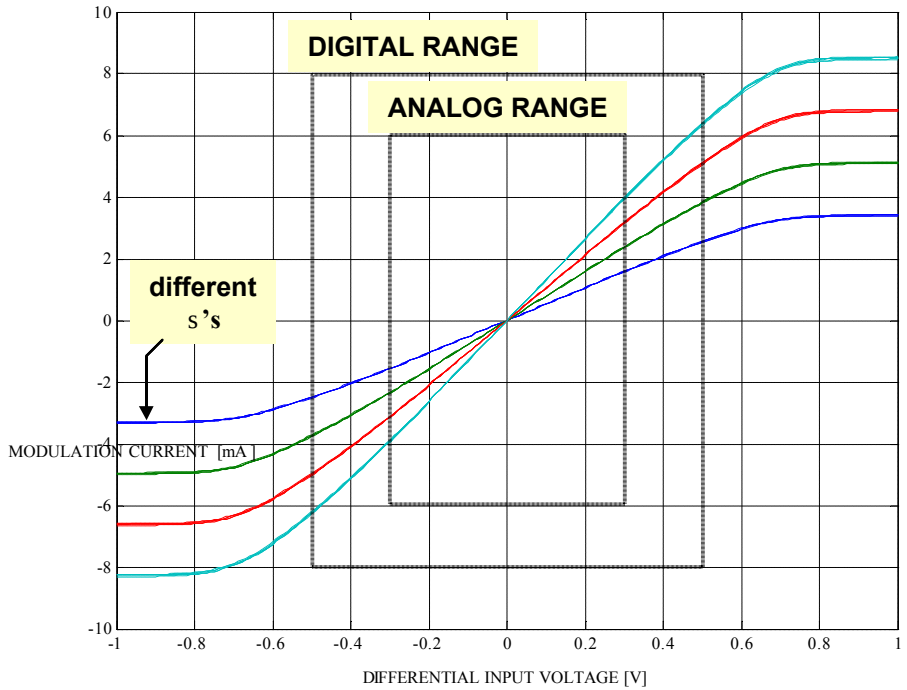
- 0.25µm CMOS (2.5V)
- Size: 2.00 x 2.00 mm
- Modularity: 3 channels
- Fully differential architecture
- Common anode biasing mode
- Linearity 1% (active bulk)
- I2C interface (tripled logic)
- Programmable gain/pre-bias
- On-chip pre-bias generation up to 55mA
- Individual channel masking

LLD: Transfer Characteristic

LASER PRE-BIAS CURRENT



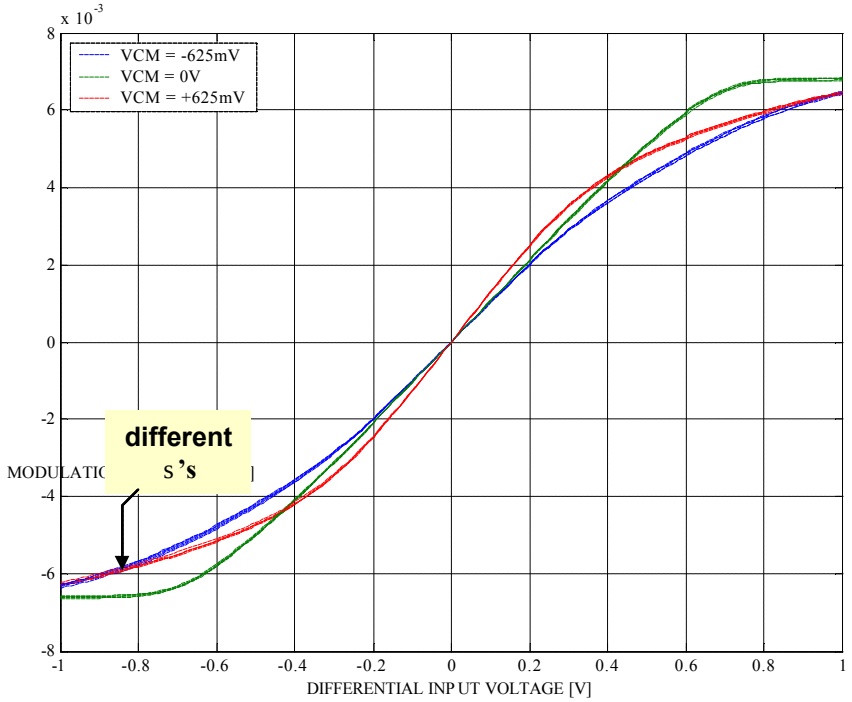
TRANSFER CHARACTERISTIC



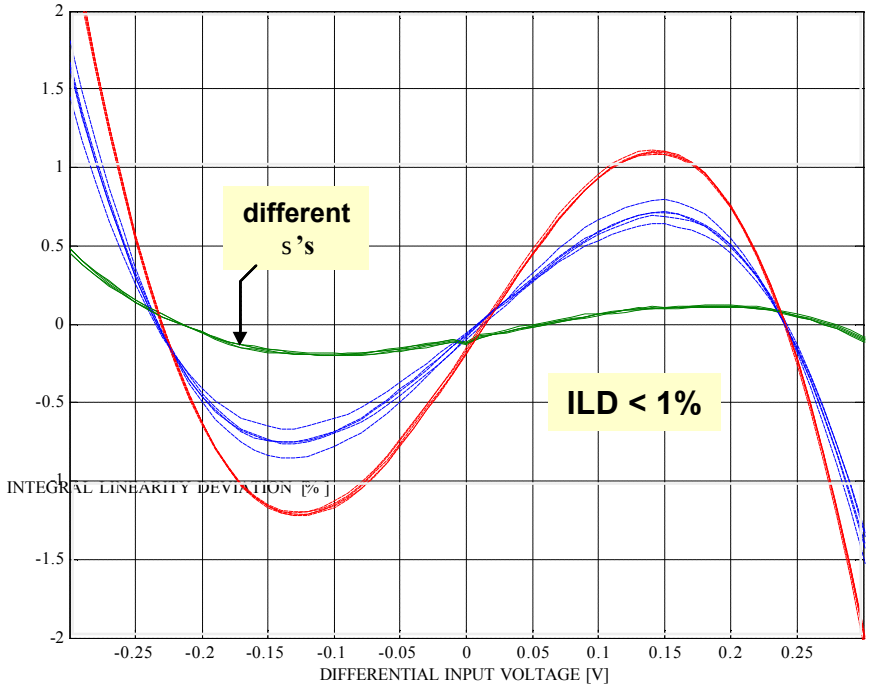
- Programmable pre-bias: 55mA (7bits)
- Switcheable gains: 5mS, 7.5mS, 10mS, 12.5mS

LLD: Gain and Linearity

TRANSFER CHARACTERISTIC



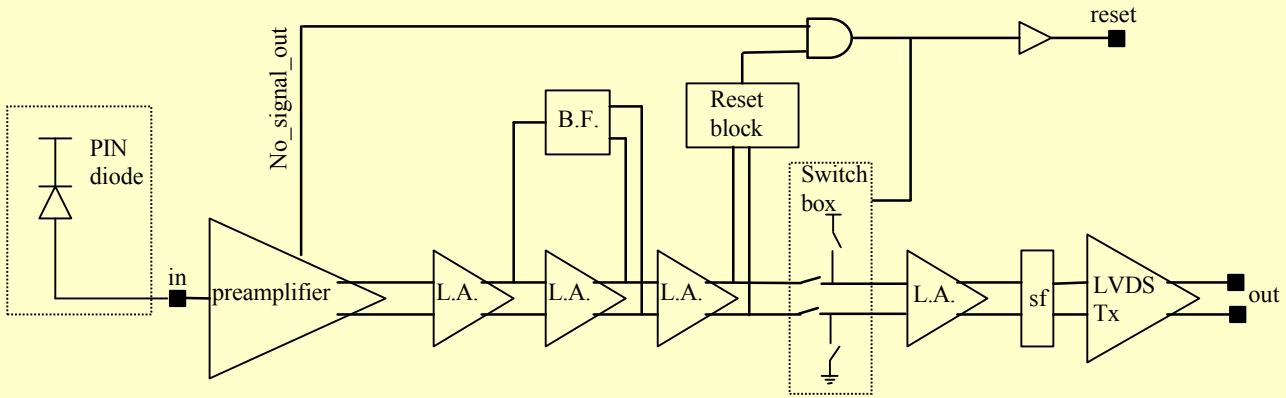
LINEARITY



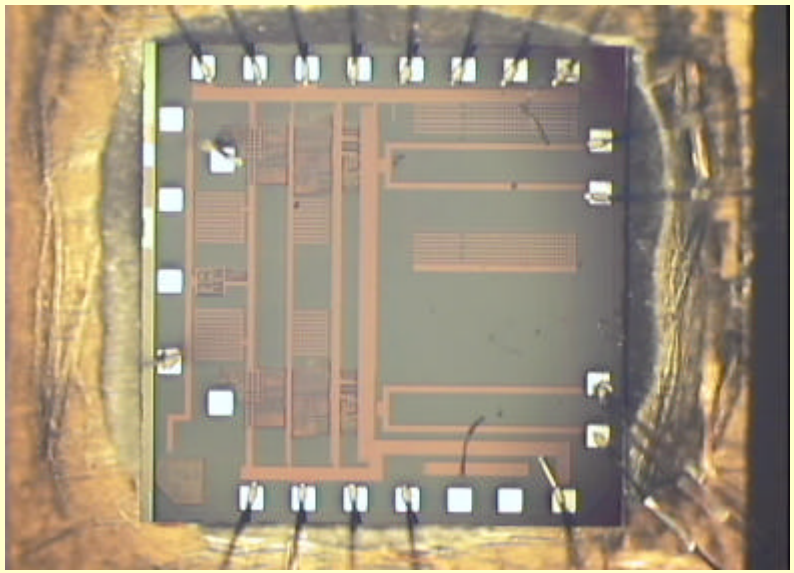
- Linear operating range: ±300mV
- Integral linearity deviation: <0.5% (Vcm=0)

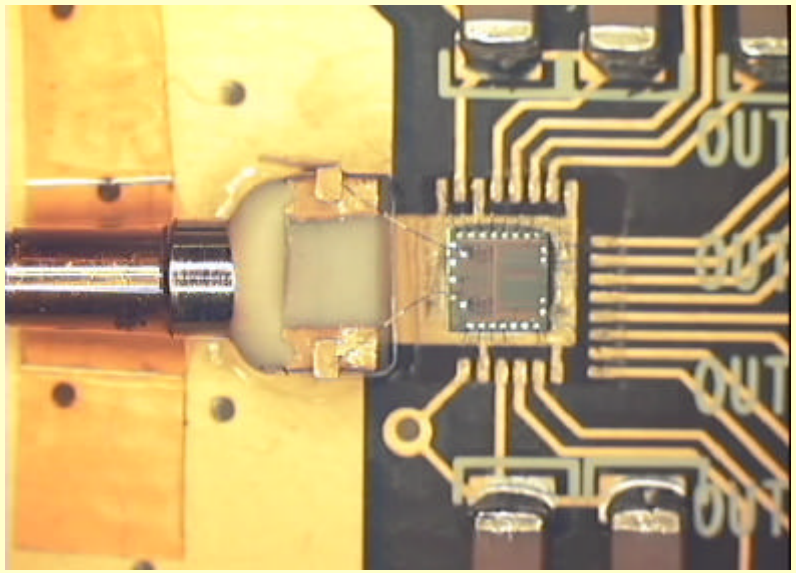
RX-40

RH Receiver for digital opto-link

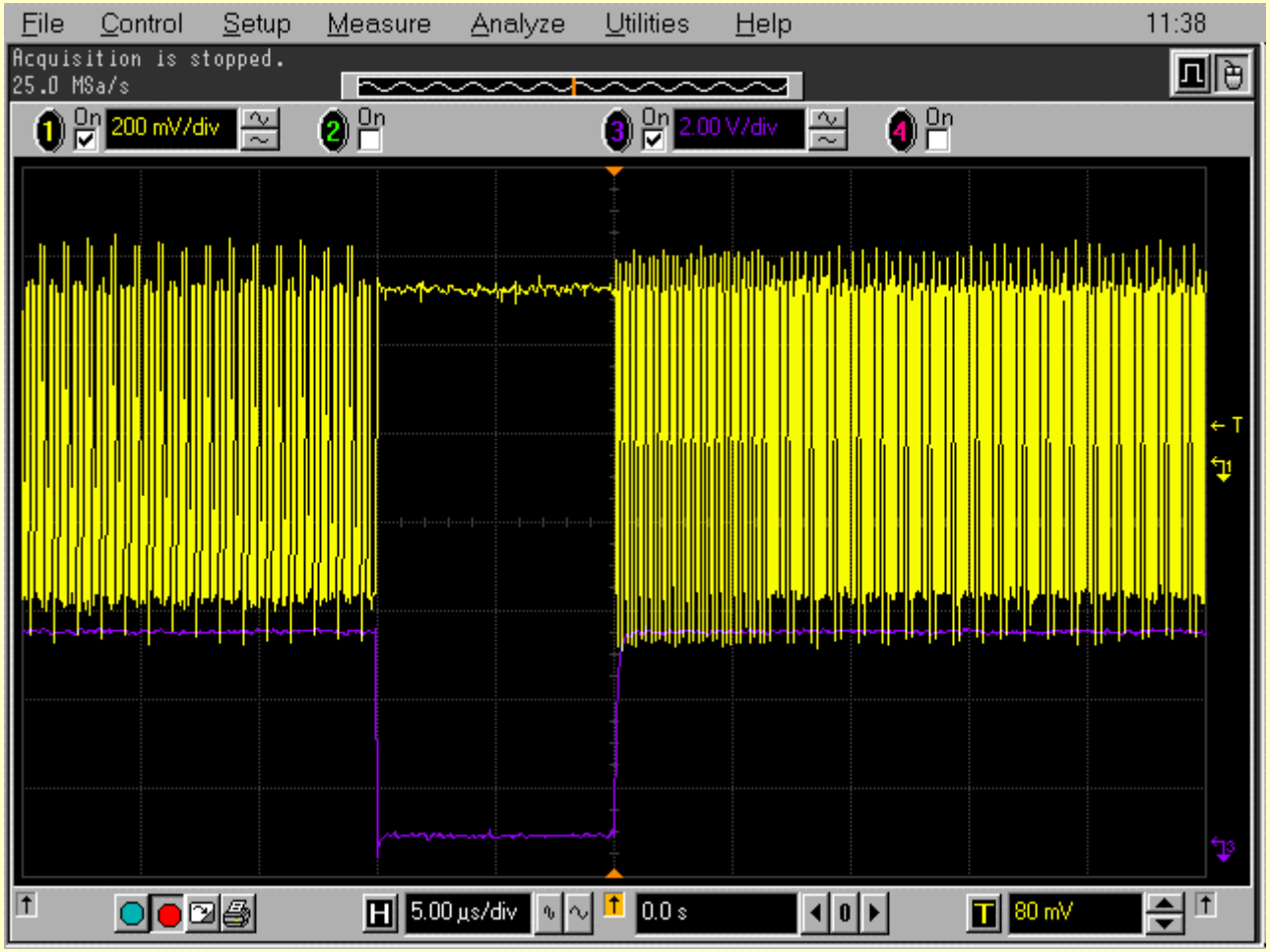


RX-40



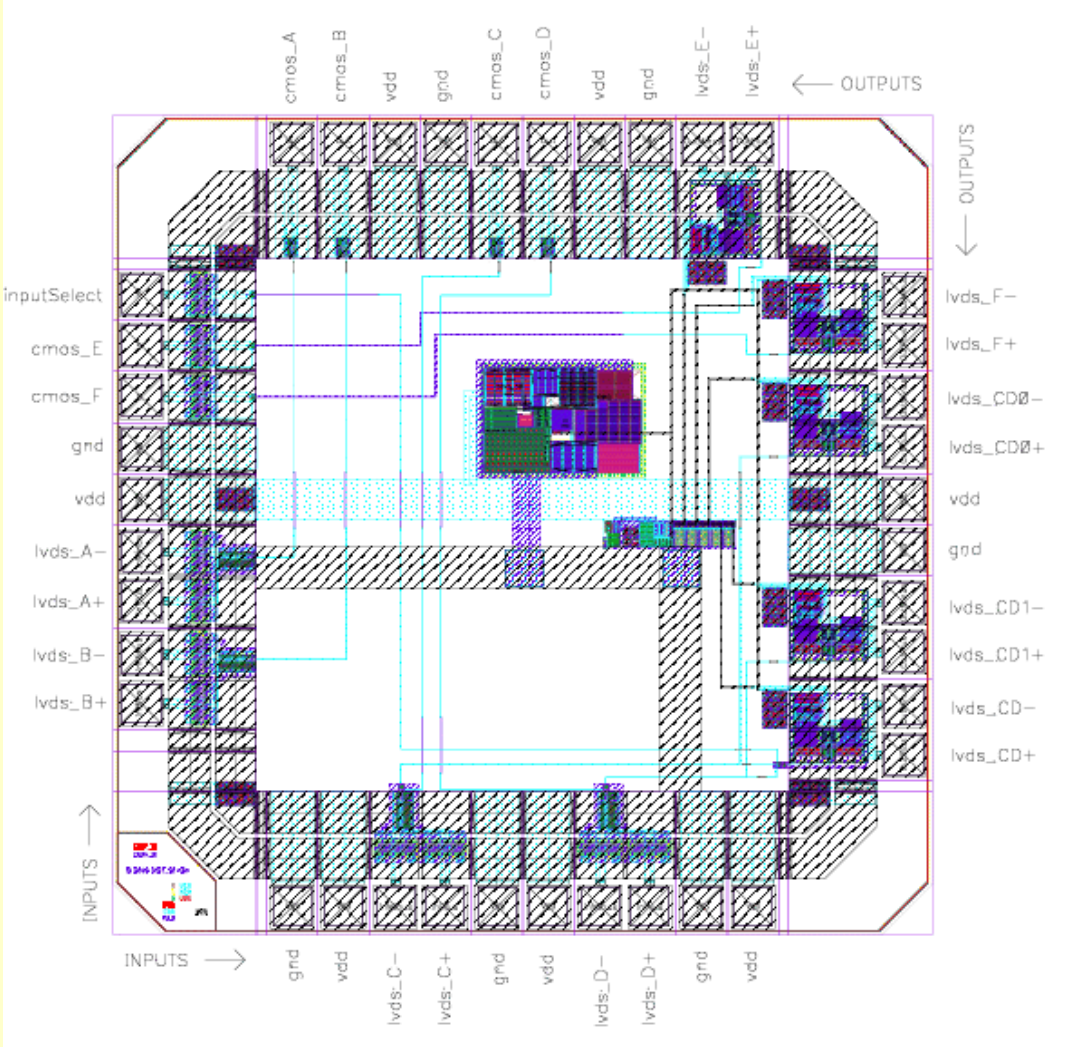


Reset from DOH



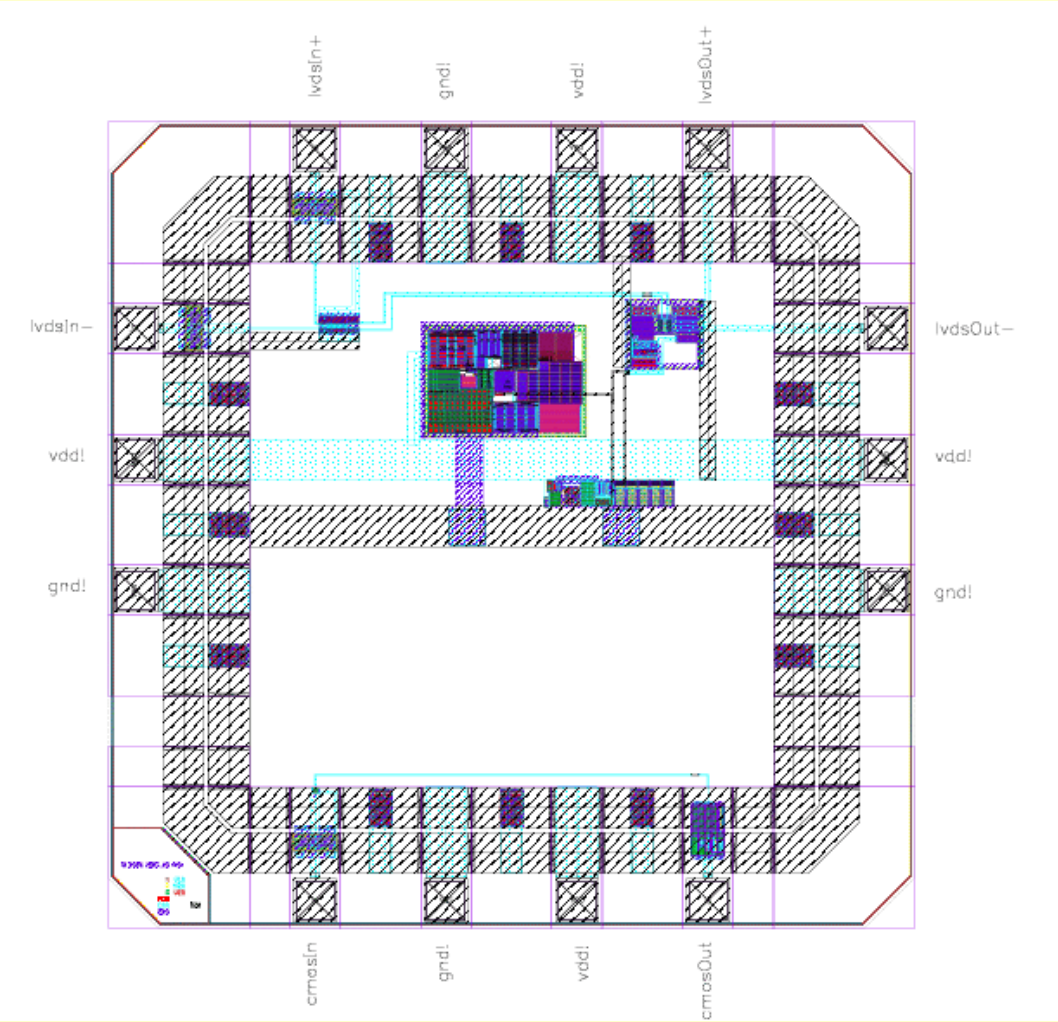
Small chips

LVDSMUX



- Used next to CCU25 for clock regeneration and distribution to ROD etc.
- 0.25µm CMOS (2.5V)
- Size: 2.00 x 2.00 mm
- Packaged in TQFP32 (7*7 mm^2)

LVDSBUF



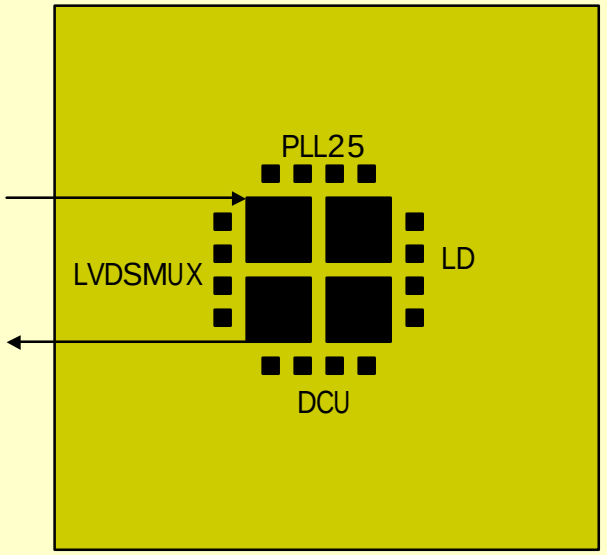
- Used on mother-cables and petals
- One LVDS + 1 CMOS repeater
- Slew rate control on CMOS
- Size: 2.00 x 2.00 mm
- Packaged in SOIC-8L

Built-in protection against SEU

- CCU25
  - Measures: 3x redundancy in node controller
  - Parity in data path and one-hot FSM
- PLL25
  - 3x redundancy on 99% of chip
- DCU
  - 3x redundancy on I2C interface
- LD
  - 3x redundancy on I2C interface

SEU Test on Components

- Irradiation with 200 MeV protons at PSI in December 2001
- Test card housing 4 CCUs, + 4 x (LD + DCU + PLL25 + LVDSMUX)
- Test procedure:
  - Configure normally running ring (remote FEC)
  - Loop reading status registers from all chips waiting for SEU events
  - Monitor I_{DD} currents on all chips with ADC on DCU itself



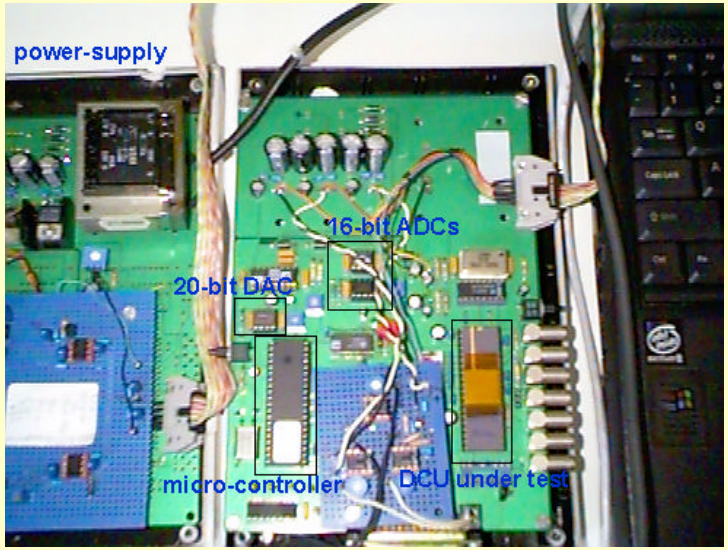
CCU25: production testing

- About 2,000 chips will be packaged
- Test vectors from design verification vectors to be translated to the IMS digital tester
- Test-fixture card with ZIF socket for fpBGA196 for IMS is being done
- Test time < 1 sec per device
- Total test time when ready < 2 weeks

DCU Production testing (1)

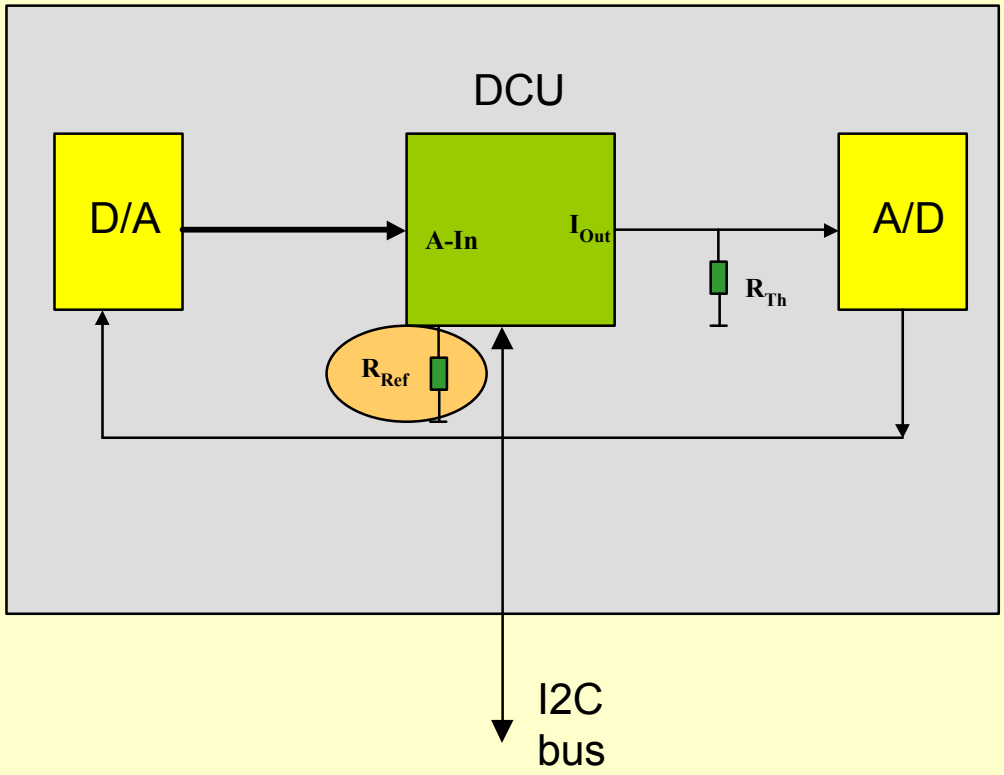
- Need one DCU per FE hybrid
- Not only a functional test but need also storing of calibration parameters
- Test on IMS tester probably too slow
  - Storing of calibration parameters from IMS too cumbersome
- Need dedicated test card
- Calibration in two phases

DCU Production testing (2)



Few points on Analog Inputs

Need to take two measurements at different temperatures

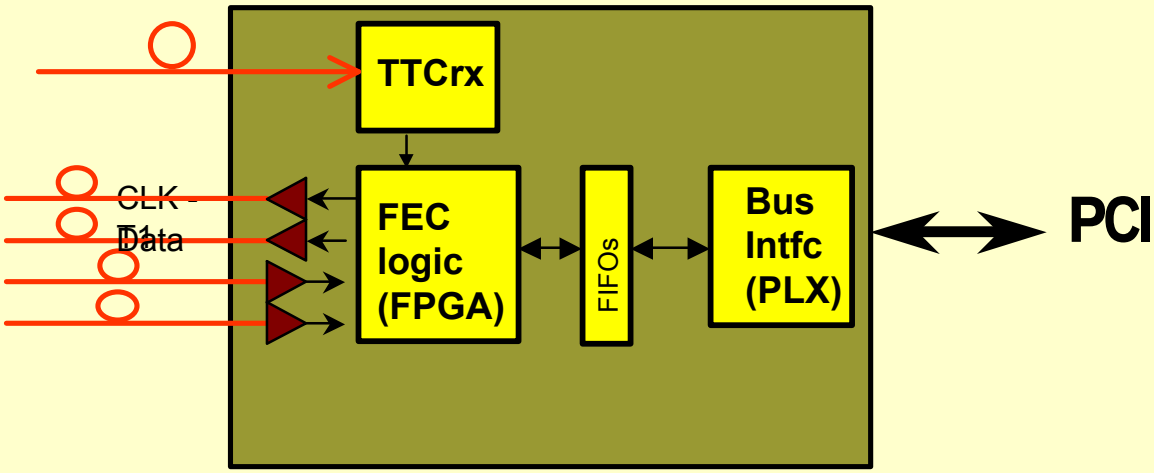


DCU Production testing (3)

- Two steps approach
  - While on test card characterize each DCU for
    - » I2C functionality
    - » Analog inputs
    - » Current references
  - Absolute voltage calibration and temperature calibration only when mounted on hybrid
    - » Store DCU parameters in DB at this stage

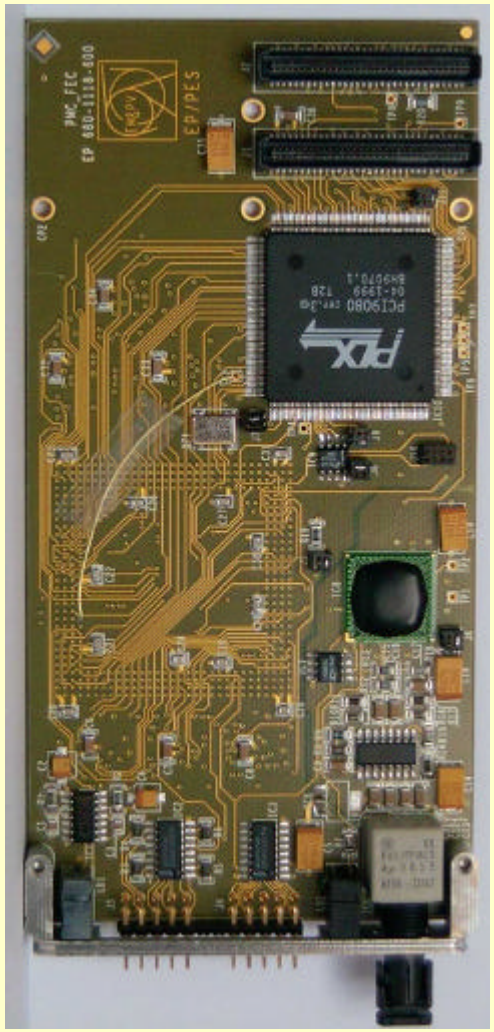
FEC

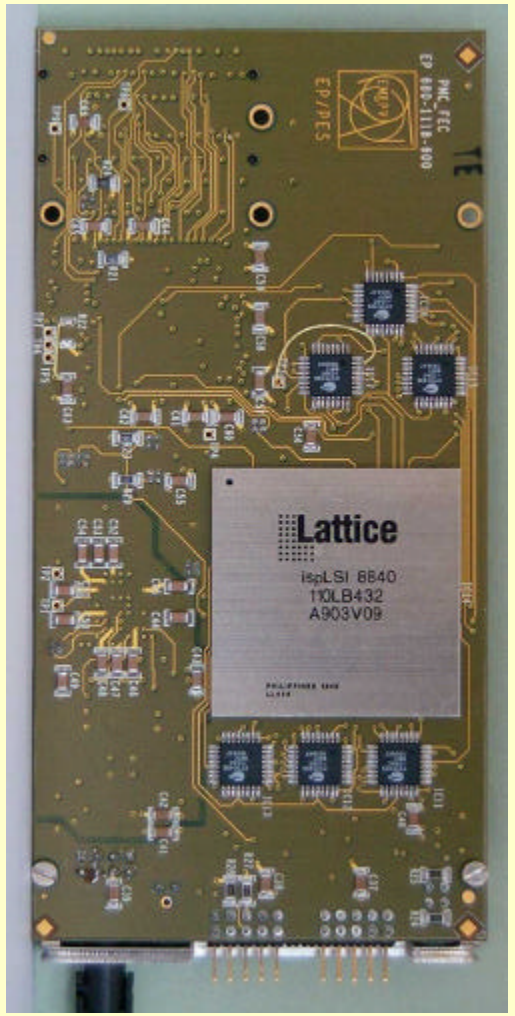
Current FEC Block diagram



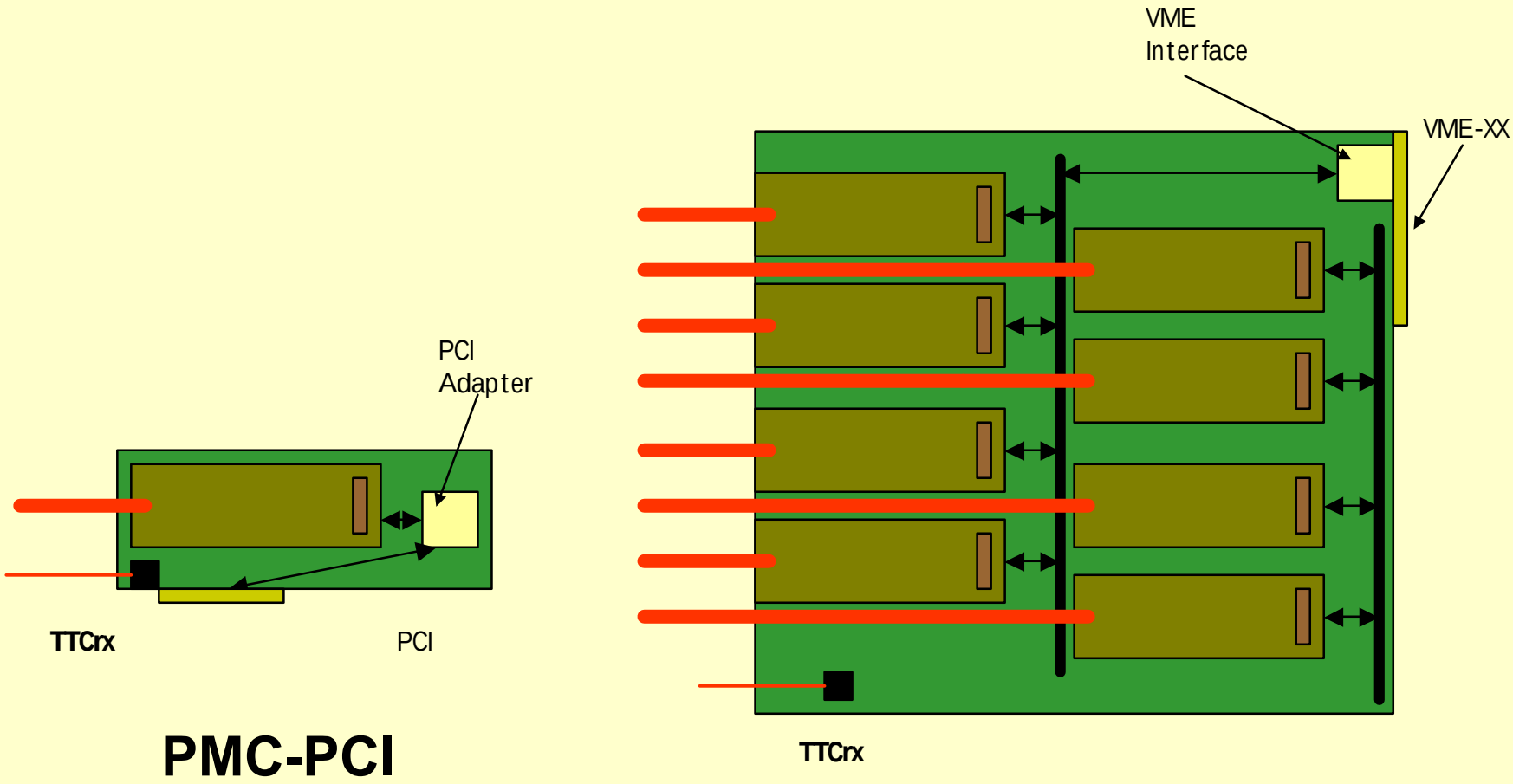
Current Version

- FEC
  - Available in PCI-PMC format
    - » Electrical I/O
    - » Optoelectronics on separate add-on board





Production version: Modular approach



PMC-PCI

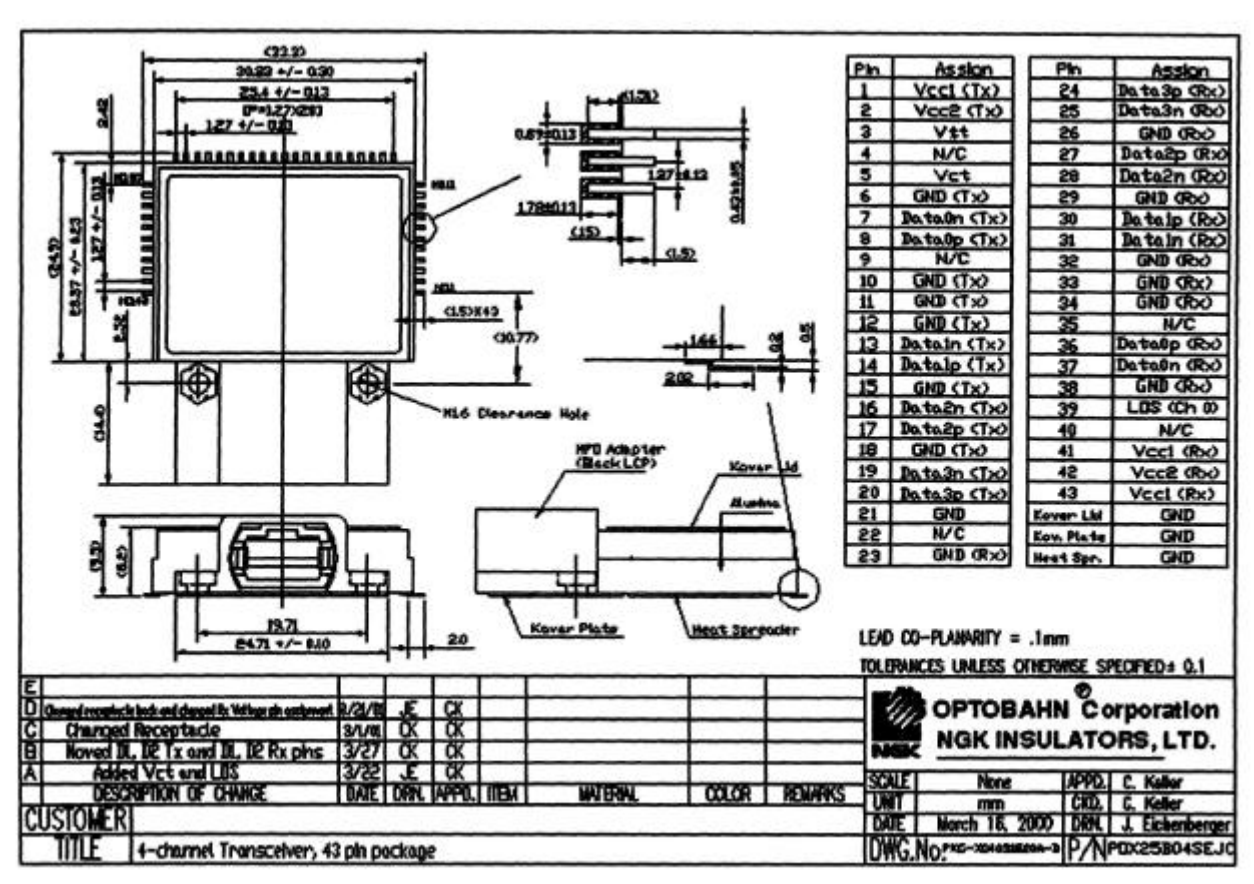
VME-9U (~360x400mm)

Specifications for final FEC

- Modularity of x1 (lab use) or 8x (experiment)
- 8 ways matches exactly one fiber-cable
- TTCrx on carrier card
- Split the internal FEC bus
  - All components and TX-RX FIFOs still on module
  - PCI or VME interface on carrier card
- Opto-electronics on module

Optical component

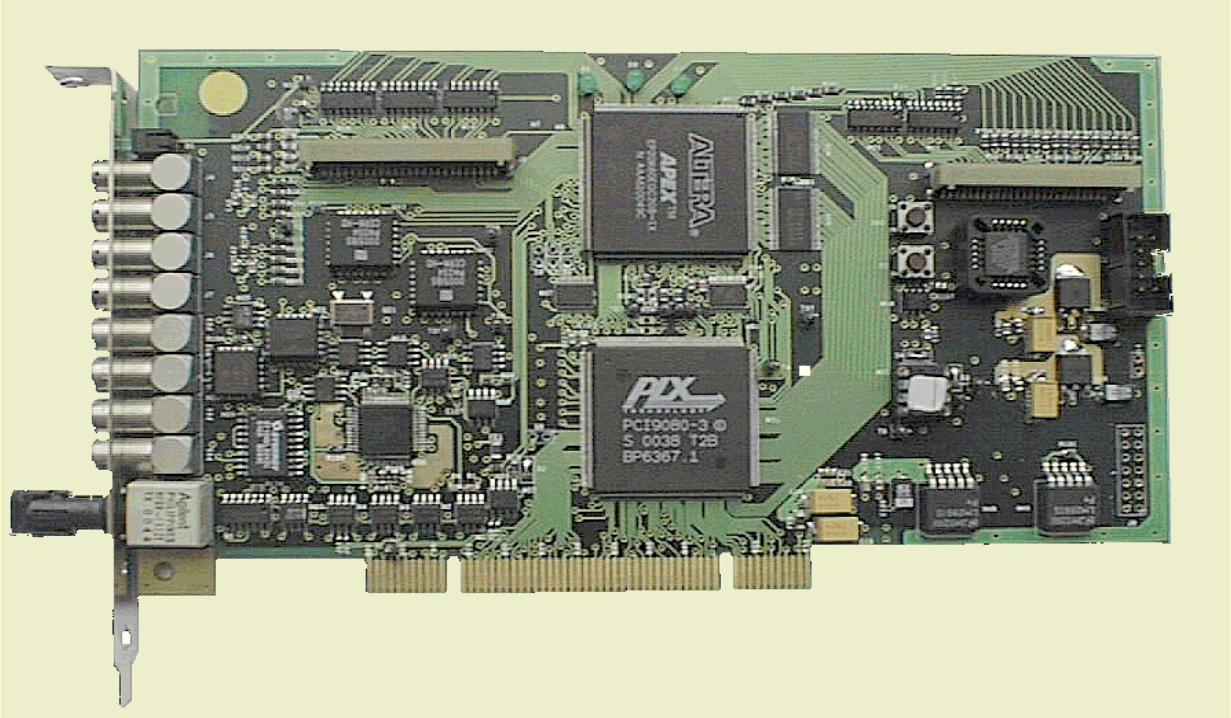
- 8 ways transceiver
- Mounted directly on FEC module
- Can't be used with electrical version !



TSC

Trigger Sequencer Card

A solution for test stations trigger management

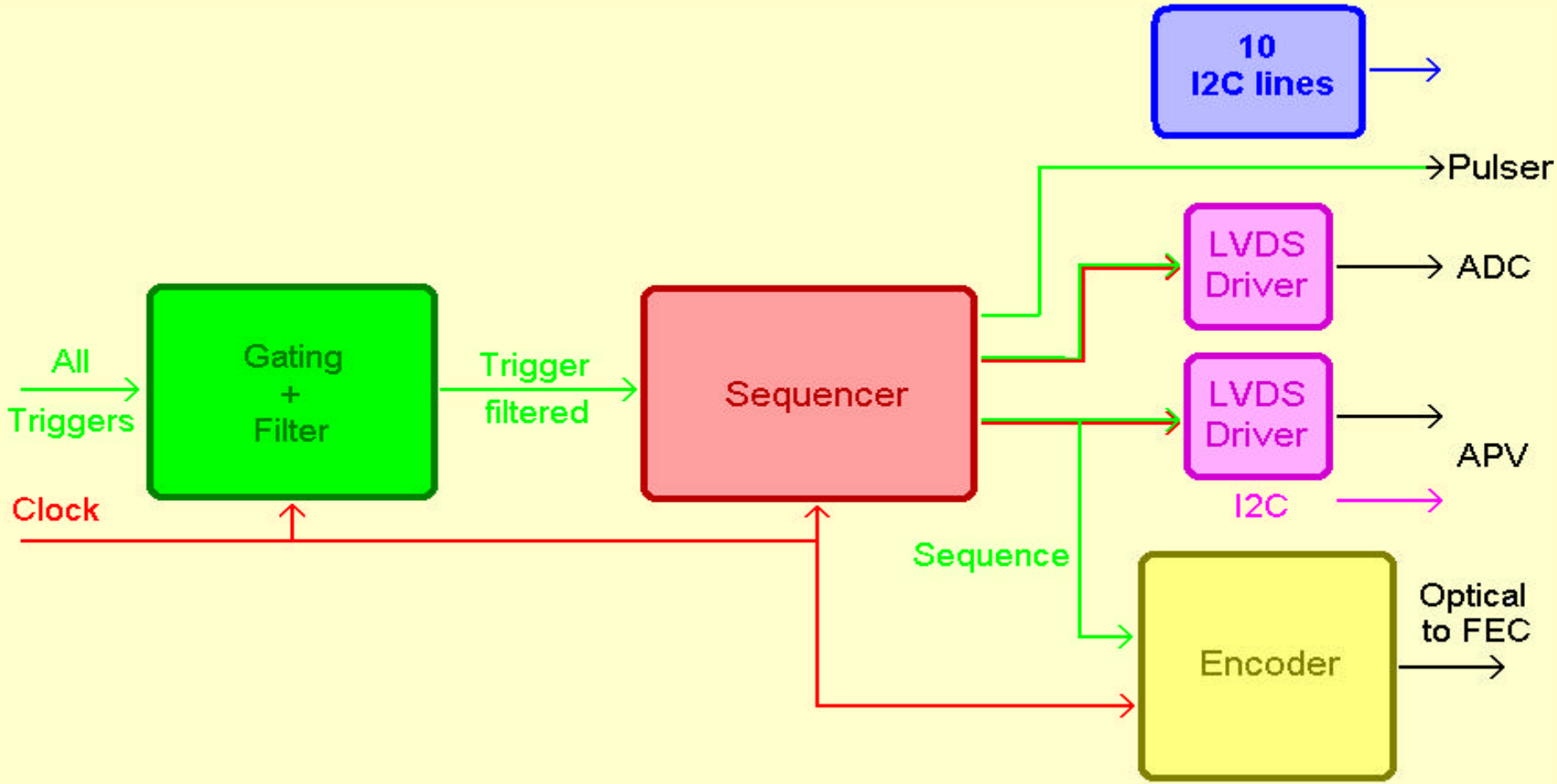


TSC features

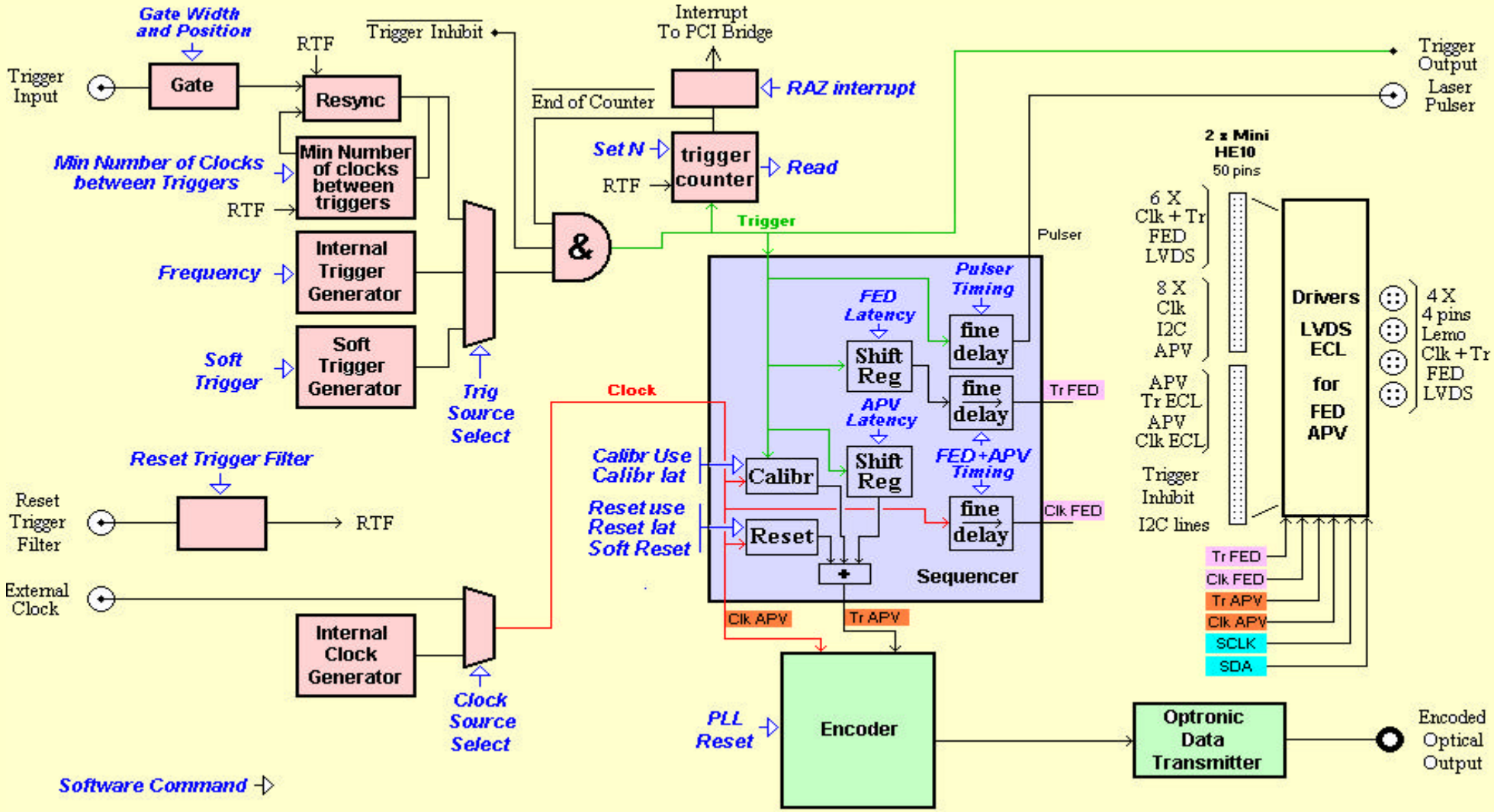
- Wait for any trigger
- Filter (gate, N clocks between triggers, count)
- Internal and external clock
- Internal and external triggers
- Make special sequence for APVs (calibration 110, reset 101)
- Electrical output for ADCs
- Electrical output for APVs
- Optical output for FEC

Documentation available at ftp://lyoftp.in2p3.fr/cms/Tsc/tsc02.pdf or .doc

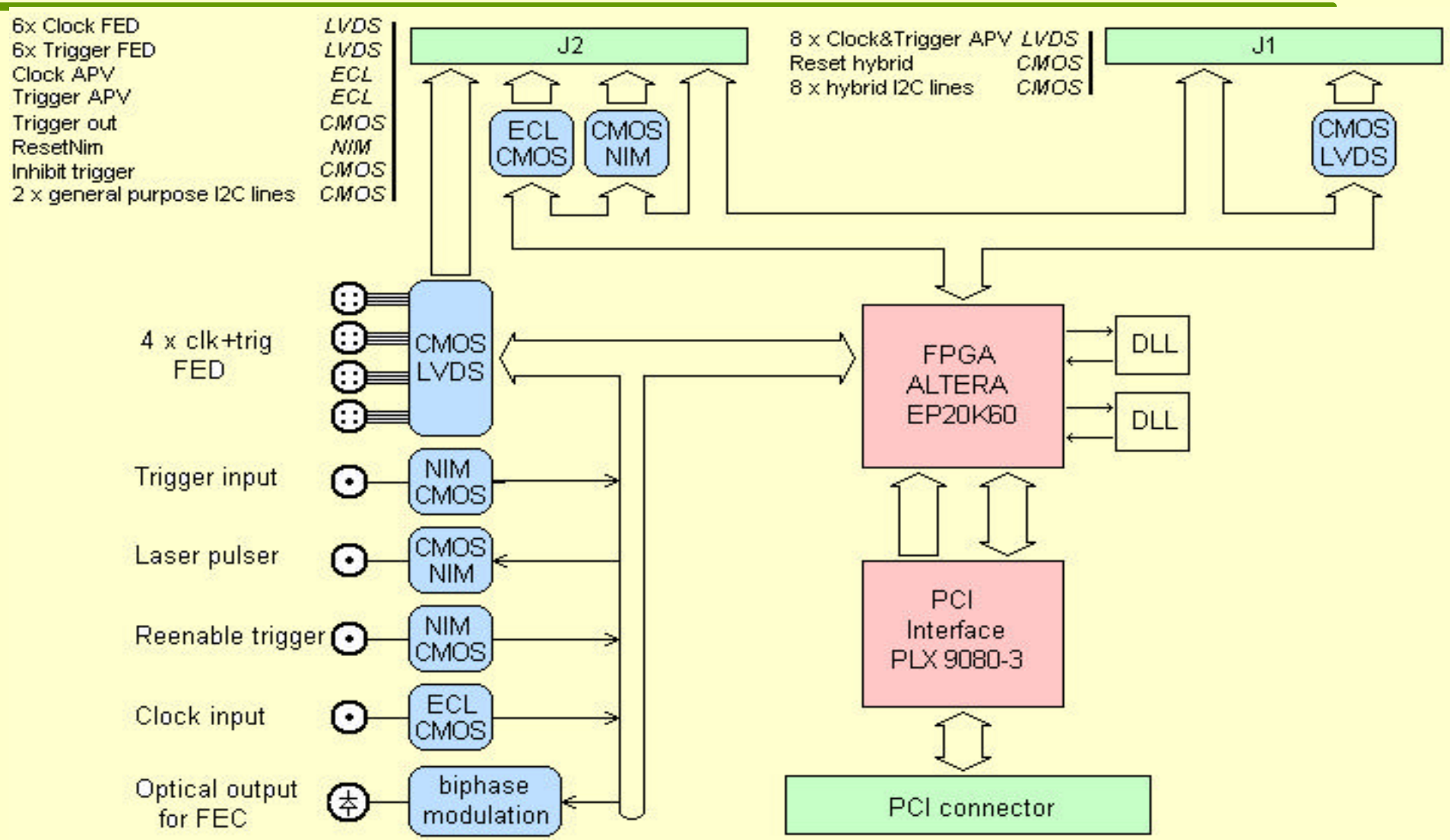
TSC simple block diagram



TSC block diagram

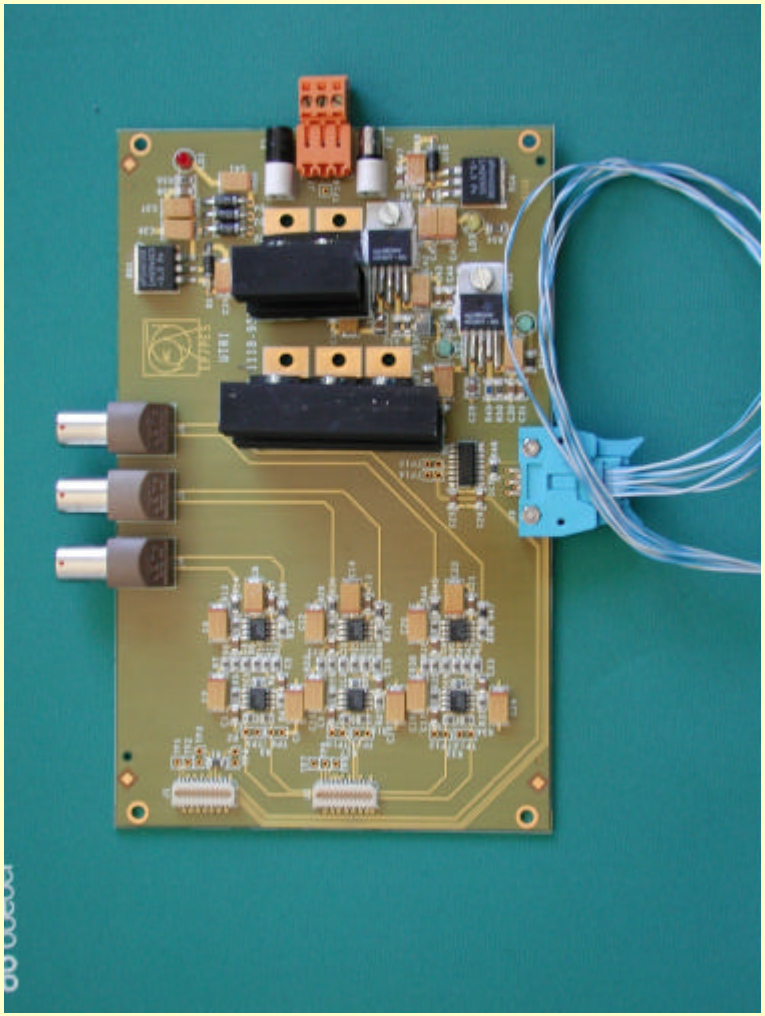


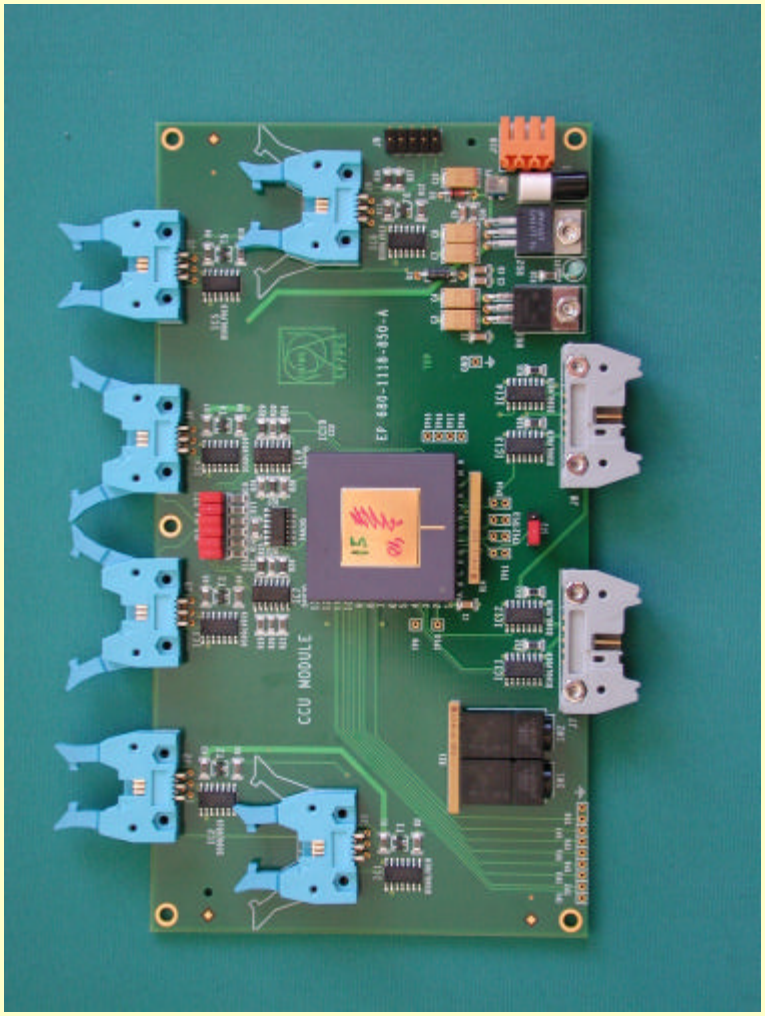
TSC functionnal block diagram



CCUM

UTRI and CCUM0





Documentation

- Doc on all components is posted on:
  CMS Tracker Control
  http://cern.ch/CMSTrackerControl

- Integration results in:
  CMS Electronics Integration
  http://cern.ch/CMSTEI/index.htm