Procedures for Module Test

Lino Demaria, Marco Meschini, Frank Hartman, Guido Dirkes

Draft2 (from 4/3/2002)

1 Introduction

The CMS Tracker will be exposed to the high radiation fluxes of LHC collider, that determine high bias voltages and the need to run at the low temperature of –10C degrees. Moreover the access will be very limited and therefore the Tracker has to guarantee a very stable running for a period of several years. For all these reasons the large number of modules of the tracker have to be tested extensively and with redundancy in order to detect all possible faults and eventually fix them. In addition it is needed a fast feedback and trace ability of potential sources of faults during production in order to guarantee a high efficiency in constructing modules of the highest quality, despite the large number of laboratories and institutions involved, and this implies to have redundancy in the testing procedures. On the other hand present manpower, time schedule and existing equipment have to be taken into account. Therefore one has to find a reasonable balance of these two aspects, a point taken into consideration in this document.

In every step of production several tests are done on all components. Purpose of this document is to describe and define the strategy of electrical tests performed with three different test setups provided with DAQ and full electronic readout chain: FHIT, ARC and CMS-like systems, all described elsewhere [1,2,3].

The production centers interested by this document are:

- hybrid manufactures
- APV25 bonding centers
- gantry centers
- module bonding centers
- module qualification centers.

When other tests, other than electrical ones, but specific to the module qualification have to be done, they will also be described in the paper as they are under the responsibility of the Module Test Working Group (MTWG).

Shipping is a crucial point of the Tracker production scheme, which may introduce failures. These may be obvious ones like breaks, but may also be tricky ones like contamination, charge up or small scratches, which may cause for example an increase of the leakage currents. Therefore all deliveries have to be checked carefully after reception.

2 Basic tests definition

The list of tests is not the final one. Tests will be in the following divided in mandatory and optional tests. During M200 the test strategy should include a large set of tests emphasizing redundancy and debugging capabilities. Time optimization will be possible only at a later stage after having well understood the first phase. General criteria to define module qualification and grading are needed already for M200, but they are meant to be a best guess: only after M200 a better qualification criteria will be possible. The list of tests is on table 1, the explanation of the single tests are in the next subsection. The grading is subdivided into A, B and rejected modules, where quality B modules will be considered as spares.

	Hybrid	**APV25** recept.	**bonding**	**Gantry** recept.		**Bonding** recept.	after bond	after T cyc	**Module** Deep test	**qualification** Long term
Optical inspection		x		x		x				
Setup-self test	x	x	x	x	x	x	x	x	x	x
I-V test					opt	opt	x	x	x	x
Basic Test: H0-test (APV25,MUX,PLL,DCU) F-test, C-test	x	x	x	x	x	x	x	x	x	x
PSh-test									x	x
PLL-test									x	
B-test			x				x	x	x	x
L-test							x	x	x	
Pipe-test									x	

Table 1: tests to be done in the various assembly and test centers. "Opt" means optional during production but it is mandatory for commissioning

The settings of APV25, MUX, PLL and DCU to be used during the tests are specified in tables 2 to 4, that are the standard value specified in references [4,5,6]. If special settings are needed they will be specified in the text.

The silicon detectors have to be ramped up or down with a speed of 10 V/s.

In all tests a constant k is assumed to convert ADC values to ENC. This does not mean an absolute calibration is required for all setups, but k has to be know at 10-20% level and must be coherent in all set-ups using the same hardware: it will ease the comparison among tests performed with different hardware.

A general description of the tests is in the following. All tests can be performed in different conditions of bias, temperature and at hybrid or module level and are always done both in peak and deconvolution mode of APV25.

2.1 Setup self test

This test has to be available in order to be able to certify the setup is well behaving. This test is not giving any output to DB or LF. It is assumed that every day at the starting of a new set of module/hybrid qualifications, or at any time the operator requires it, a setup self-test is issued to guarantee the setup is well performing.

Bias Name	Description	Value	Meaning
IPRE	Preamp Input FET Current Bias	98	460uA
IPCASC	Preamp Cascode Current Bias	52	60uA
IPSF	Preamp Source Follower Current Bias	34	50uA
ISHA	Shaper Input FET Current Bias	34	50uA
ISSF	Shaper Source Follower Current Bias	34	50uA
IPSP	APSP Current Bias	55	80uA
IMUXIN	Multiplexer Input Current Bias	34	50uA
ICAL	Calibrate Edge Generator Current Bias	29	+/- 25 000 (1 m.i.p. 300 ? m) electrons
VFP	Preamp Feedback Voltage Bias	30	-0.75V
VFS	Shaper Feedback Voltage Bias	60	-0.75V
VPSP	APSP Voltage Level Adjust	40	+0.69V
LATENCY	Delay Between Write and Trigger Pointers	132	3.3us
MUXGAIN	Sets Gain of Multiplexer	xxx00100	100uA / mip

Table 2: nominal settings for the APV25-S1

Preamp Polarity	Inverting
Read-out Frequency	20MHz
Calibration Inhibit	OFF
Trigger Mode	1-sample
Analogue Bias	ON

Table 3: Standard APV25-s running mode

Description	Value
Mux resistor bits	255
PLL trigger delay	0
PLL phase shift	0

Table 4: MUX and PLL settings

2.1.1 ARC system:

For the ARC system these are the tests implemented:
2.1.1.1 Read and write test of status register;
2.1.1.2 Read and write tests of chips handling the I_2C
2.1.1.3 Scan of I_2C addresses
2.1.1.4 Memory self test

2.1.2 CMS like system

For the CMS like system tests of the single units are implemented:
2.1.2.1 basic functioning of TSC, FEC, FED, CCU
2.1.2.2 scan of I_2C addresses

2.2 Optical inspection

All steps in production start with an optical inspection after reception.
Using a stereo microscope with a magnification of about 10-20X the optical inspection allows to check whether obvious damages like touched bonds, scratches and any kind of unusual appearance, have happened.

Optical inspection can also be done after electrical tests, to help understanding the reason for badly behaving strips.
In any case, action might follow if potentially dangerous damages are found and/or repairs are possible (i.e. damaged or shorted bonding wires). Result of this test will be either nothing unusual observed or a possible damage found, writing on the DB a Y/N flag and a string describing the problem found and giving a pointer to a web page where a test sheet (see appendix) and the picture of the damage can be found.

2.3 IV-test

The sensor bias voltage is taken up to V_{max} following the standard ramp up procedure of 10 V/s, recording current values every 100V and leaving the sensor at V_{max} for one minute: the final current is then recorded too.

2.4 Basic test

It is the core test for hybrid and module. It is made out of three different tests and it should take a couple of minutes:

2.4.1 H0- test (hybrid)

The correct functioning of the components mounted on the hybrid is tested (APVMUX, APV25, DCU, PLL). Tests are:

2.4.1.1 r/w I_2C tests for all registers (APV25, MUX, PLL and DCU test);
2.4.1.2 check of LV as measured by DCU (DCU test)
2.4.1.3 check of LV currents (APV25, chip per chip and total) by biasing one chip at the time and checking the baseline response (APV25 and MUX test);
2.4.1.4 check correct header (APV25 test);
2.4.1.5 : check of temperature measured by DCU (DCU test)

2.4.2 F-test (fast)

It is the measurement of pedestal, noise before (RN_i) and after common mode subtraction (N_i) for at least 1000 events. Both ARC and CMS-like systems have to use the same algorithm for the computation of this variable. Headers are checked through all data acquisition. During F-test the reset should not be sent.

2.4.3 C-test (calibration)

The response of the APV25 to a internal calibration signal at the input of the preamplifier is measured. It is done at a fixed timing, roughly corresponding to the maximum amplitude of the shaped signal. The calibration signal is distributed to 16 channels per APV at the time, one channel every eight, and the response of every channel is corrected for a common shift of pedestals due to a common mode rejection feature of the APV25 chip. A variation of APV gain, linearity, shaping or multiplexing will be detected as a variation on the response to the calibration signal. By sending a calibration signal chip per chip, also the proper performance of the MUX can be checked.
When connected to a module a small fraction of calibration signal is lost in the channel

strip, depending on its total capacitance, since it is in parallel with the preamplifier. This makes the C-test sensitive mainly to strip shorts and disconnected channels.
Runs with calibration pulses of 2 and 3 mips can be used, taking at least 1000 events with a calibration pulse for every channel, for a total of at least 8000 events.

2.5 B-Test (Backplane pulsing)

Injecting a pulse on the backplane via an AC coupling on the HV line a signal is induced in all strips. This amplitude of the induced signal should be roughly equivalent to that of 2 mips per channel and the response of every channel is measured. Unbonded strips are easily spotted with this test, showing a very different behavior than normal strips, but this test is able to spot also other defects. The feature of on chip common mode subtraction does not invalidate the relevance of this test, but it is best performed without the inverting stage on.

For TIB modules the backplane pulse will be injected before the RCR filter (2 volts) , while for TOB and TEC might be send after, with the sensor backplane in parallel with the RCR filter (about 2 V).

2.6 L-tests (test with light)

The light test is meant to verify the response of the silicon to a physical signal. The light could be generated by a Led or by a Laser.

There are two different tests foreseen with light.

1 Pulsed light. The light spot can fire several strips so that during the test all channels should be given a light signal corresponding to around 2-4 mips. The response of every channel is compared to the average response of the other channels or in term of the absolute value. The light has to be sent at the very end of the silicon strips, so to spot not only unbonded channels, shorted strips, but also breaks of the aluminum readout lines at the very end of the lines. This signal may even be suited to check the PLL, see later in the text.

2 Continuous light, defocused

Recent results indicate that this test is capable to detect pinholes quite efficiently.
Due to the fact that the level of leakage current of sensors before irradiation is very low, other tests might not be so sensitive to all sensor pinholes, coming intrinsically from the sensor fabrication or possibly from the bonding. Continuous light determines an increased leakage current and by driving it close to value expected at the end of LHC it ease the detection of pinholes as a variation in the pedestal value of the defective channels.

In addition this test is suitable to check the measuring power of the DCU, above the level of sensitivity, which is not reached at the bare unirradiated module.

2.7 Pipe-test (pipeline check)

It is a more advanced F-test: by taking events with a reset signal and scanning for different latency bins it measures pedestal and noise at different pipeline cells locations. This test can spot problems of pipeline cells for every channel that are otherwise not seen in a standard F-test. This test takes few minutes (about 4 minutes) and therefore is not foreseen where the testing time is limited.

2.8 Psh-test (pulse shape)

It is a more advanced C-test. The calibration pulse is measured at different time latencies, with steps of 6.25 ns (minimum step is 3.125 ns, which value do we want?). This allows to determine the shape of the signal at the output of the shaper of the APV25 and therefore to better disentangle the source of a possible problem tagged by a C-test. A calibration signal of 2 mips is used.

This test takes several minutes (about 10 minutes) and therefore is not foreseen where the testing time is limited.

2.9 PLL test

If a PLL chip fails dramatically in sending proper trigger or clocks, it will certainly determine a failure of a fast test. A check of the proper performances of the fine delay A PLL test is foreseen making a fine time scan using the PLL delay of the response of the APV25 to an external signal. The signal can be a fast (< 5ns) light or others. This test has still to be investigated in detail.

3 Variables definition

Several variables will be used in the tests description; therefore here is a list of variables that will be often used later. Not all these variables will go to the DB, see later on the document for this topic.

Test global variables:

TS-ID	= test station ID	
Op-ID	= operator ID	
DB-vs	= Data base version	
LF-vs	= Local file version	
Soft-vs	= software version ID	
Alg-ID	= pedestal/noise algorithm ID	
Set-ID	= set up configuration file ID	
T_{room}	= room temperature	[C]
H_{room}	= relative room humidity	[%]
TS-T_i	= test station temperatures	[C]
TS-H_i	= test station relative humidities	[%]
k	= constant for ADC to Electron constant	[e-/ADC]
t_{start}	= date/time when the test was started	
t_{end}	= date/time when the test was ended	

Module global variables

MD-ID = module/Hybrid identifier
MD-type = module/Hybrid type (TOB1-2, TEC1-8,TIB1-2,TID1-4)
MD-grade = Module grade
MD-stat = Module/Hybrid status flag

MD-T1 = module sensor temperature #1
MD-T2 = module sensor temperature #2
H-T = hybrid temperature (from DCU) [C]
I25 = total 2.5V current from power soppy [mA]
I125 = total 1.25 current from power supply [mA]
$I25_i$ = 2.5V current taken by chip #I [mA]
$I125_i$ = 1.25V current taken by chip #I [mA]
VDC125 = voltage of 1.25V line measured by DCU [mV]
VDC25 = voltage of 2.5V line measured by DCU [mV]
V125 = voltage of 1.25V line measured by power supply [mV]
V25 = voltage of 2.5V line measured by power supply [mV]
V_{max} = max bias voltage (500V) [V]
V_{std} = standard running voltage (300V) [V]
I = leakage current [? A]

Channel variables:

Nchan = channel number
$Stat_i$ = channel status flag
P_i = pedestal of i-th channel (average on all pipeline cells); [ADC]
$P_{i,?}$ = pedestal of i-th channel at ? -th pipeline element; [ADC]
RN_i = raw noise of i-th channel (average on all pipeline cells); [ADC]
N_i = noise of i-th channel (average on all pipeline cells), after event per event CMN subtraction; [ADC]
$N_{i,?}$ = noise of i-th channel at fixed ? pipeline element, after event per event CMN subtraction; [ADC]
CMN_l = common mode noise distribution, done chip per chip, Nbin= 400, min = -20 , max= 20; [ADC]
p_{Ni} = probability of i-th channel for fluctuations at least three sigmas above pedestal; [%]
C2i = response of i-th channel to calibration signal of 2 mips; [ADC]
$C3_i$ = response of i-th channel to calibration signal of 3 mips; [ADC]
CF_i = fluctuation of calibration signal ;
PSh_i = pulse shape distribution of i-th channel for a calibration signal of 2 mips Nbin = , tmax= [ADC]
$CPRT_I$ = calibration pulse rise time of i-th channel (2 mips) [ns]
$CPFT_i$ = calibration pulse fall time of i-th channel (2 mips) [ns]
$CPPT_i$ = calibration pulse peak time of i-th channel (2 mips) [ns]
$CPPA_I$ = calibration pulse amplitude time of i-th channel (2 mips) [ADC]
B_i = response to backplane pulse of i-th channel; [ADC]
L_i = response to a light pulse of i-th channel; [ADC]
LF_i = fluctuation of the light signal [ADC]

$?_{Li}$ = efficiency of the i-th channel to respond to a light beam with a signal above a certain threshold; [%]

Some module global variables are describer in Table 5.

The results of the tests might be written to the Data Base (DB) and/or to a local output (LF) file. Both ARC and CMS-like system will write identical information on the DB. The LF will contain more information and has a more flexible structure: the format of the LF will be a RootDB file. The transfer from LF to DB is done by a program (Parser) that converts LF to XML file to be sent to BigBrowser.

Variable	Format	Meaning
Module/Hybrid grade	string	A,B or rejected
Module/Hybrid status flag:	16 bits word	bit 0-5: i-th chip APV25 status (0=ok,1=not ok)
		bit 6 MUX status
		bit 7 PLL status
		bit 8 DCU status
		bit 9 sensor status
		bit 10 number of bad strips exceeded
		bit 11 optical test
Bad strip status flag	16 bits word	bit 0 F-test status (0=ok,1=not ok)
		bit 1 C-test status
		bit 2 B-test status
		bit 3 L-test status
		bit 4 Pipe-test status
		bit 5 PSh status
		bit 6 F-test at Vmax status
		bit 7 F-test status at low temp (1=ok,0=not ok)

Table 5: description of the summary variables.

Each test has a header that contains the following information both for the LF and the DB

MD-ID	integer
MD-type	integer
MD-grade	string
MD-stat	16 bits
bad ch & stat.	integer array
TS-ID	integer
Op-ID	integer
DB-vs	integer
Soft-ID	integer
Alg-ID	integer
Set-ID	integer
k	real

DB and LF Test header (optical test results should be included…)

4 APV testing

These tests are done at chip level and are performed by Imperial College. They are reported here for completeness. See (missing reference !) for a more detail description.

The sequence of tests is :

i) I_2C response, current tests.
ii) Measurement of ?P_i,, N_i,? in peak and deconvolution mode
iii) Measurement of ?$P_{i,,?}$?.
iv) Calibration pulse shape measurement

Bad channels are defined according to cuts on pedestal, noise and calibration figures. Only APV chips that have no bad channels and have passed positively all tests go to next production stages.

5 Tests at Hybrid manufacturers

This test will be done after M200.
The test at hybrid manufacturer are made with the FHIT setup. It is essentially a Basic-test. The list of information written to LF is the following

Basic-test flag	integer
T_{room}	real
TS-T	real
t_{start}	integer
t_{end}	integer
H-T	real
I25	real
I125	real
$I25_i$	real
$I125_i$	real
VDC125	real
VDC25	real
Alg-ID*10000 + Set-ID	integer

P_i (peak)	real array
Rni(peak)	real array
Ni(peak)	real array
CMNl(peak)	real array
C2i(peak)	real array
C3i(peak)	real array
P_i (dec)	real array
Rni(dec)	real array
Ni(dec)	real array
CMNl(dec)	real array
C2i(dec)	real array
C3i(dec)	real array

Basic-test: DB and LF information

It is strongly suggested that the LF are loaded to the DB by a CMS Tracker group (Strasbourg or CERN). The DB information is the same as in the LF.

5.1.1 Bad channel definition:

A channel is defined as bad channel if it does not pass any of following rules:

1) $PL < P_i < PH$

2) $NL < N_i < NH$

3) $CL < C2_i < CH$

All cuts are defined at +-20% around the mean value for every single variable.

5.1.2 Hybrid grade definitions:

- Grade A if hybrid has less than 0.2% bad channels
- Grade B if hybrid has less than 0.5% bad channels
- Bad hybrid if:
  more than 0.5% bad channels
  any of MUX/PLL/DCU or APV25 fails

6 Tests of Hybrid at Strasbourg

These tests are done during M200…. Comments from Ulrich needed

7 Testing at pitch adapter-APV25 bonding centers

***After reception*:** Optical inspection, Basic-test

The LF is the same as for basic-test but no DB information are filled

After bonding: Basic-test, B*test

The B* test is like the B-test but the pulse is induced to the pitch adapter lines via capacitance coupling using an appropriate hardware. The LF and the DB information are the same:

pa-test flag	integer
T_{room}	real
TS-T	real
t_{start}	integer
t_{end}	integer
H-T	real
I25	real
I125	real
$I25_i$	real
$I125_i$	real
VDC125	real
VDC25	real
Alg-ID*104 + Set-ID	integer

P_i (peak)	real array
Rni(peak)	real array
Ni(peak)	real array
$CMN_{i(peak)}$	real array
C2i(peak)	real array
Bi (peak)	real array
P_i (dec)	real array
Rni(dec)	real array
Ni(dec)	real array
$CMN_{i(dec)}$	real array
C2i(dec)	real array
Bi(dec)	real array

P.a. bonding LF and DB information

7.1.1 Bad channel definition:

A channel is defined as bad channel if it does not pass any of following rules:

1) $PL < P_i < PH$
2) $NL < N_i < NH$
3) $CL < C2_i < CH$
4) $BL < B_i < BH$

All cuts are defined at +-20% around the mean value for every single variable.

7.1.2 Hybrid grade definitions:

Grade A if hybrid has less than 0.4% bad channels
Grade B if hybrid has less than 0.8% bad channels
Bad hybrid if more than 0.8 % bad channels

8 Testing at Gantry Centers

***After reception*:** Optical inspection, Basic-test
The LF is the same as for Basic-test, but no DB information are filled
***After assembly*:** IV-test (optional), Basic-test

The IV-test is considered as mandatory at commissioning of the Gantry center and for few modules after every retuning of the Gantry machine. The hardware used for this test can consist of a manual probe station or can be done via bonding.

The information on LF and DB are written as for the Basic test.

8.1.1 Bad channel definition

A channel is defined as bad channel if it does not pass any of following rules:

1) $PL < P_i < PH$
2) $NL < N_i < NH$
3) $CL < C2_i < CH$

All cuts are defined at +-20% around the mean value for every single variable.

8.1.2 Hybrid grade definitions

Grade A if hybrid has less than 0.4% bad channels
Grade B if hybrid has less than 0.8% bad channels
Bad hybrid if more than 0.8% bad channels

9 Testing at Module Bonding Centers

Here the test strategy is pointing to immediate identification of defects for possible repairs of unbonded, shorted and pinhole channels.

After reception: Optical inspection, IV (M200 compulsory), Basic-test

The LF is the same as for Basic-test, but no DB information are filled

The IV-test is mandatory at the commissioning of the bonding. The hardware used for this test can consist of a manual probe station or can be done via bonding.

Bonding from pitch adaptor to detector follows,
and also bonding to the detector bias lines (for TIB also in the backplane).

After bonding: IV-test, Basic-test(V_{std}), B-test(V_{std}), L-test(V_{std})

The LF is the same as for Basic-test with the addition of IV data, but no DB information is filled.

***Thermal cycle*:** The module is undertaken a thermal cycle down to –10C , passive or (optional) under bias and while taking data.

***After thermal cycle*:** IV-test, Basic-test(V_{std}), B-test(V_{std}), L-test(V_{std})

The LF and DB are identical:

bonding flag	integer
T_{room}	real
t_{start}	integer
t_{end}	integer
Alg-ID*104 + Set-ID	integer
IV data	real array
Basic-test data @ Vstd	
I-t data	real array
B-test data	
L-test data	

Bonding test: LF and DB files

9.1.1 Bad channel definition:

A channel is defined as bad channel if it does not pass any of following rules:

1) $PL < P_i < PH$
2) $NL < N_i < NH$
3) $CL < C2_i < CH$
4) $BL < B_i < BH$
5) $LL < L_i < LH$

All cuts are defined at +-20% around the mean value for every single variable.

9.1.2 Module grade definitions:

Grade A if module has less than 1% bad channels, and I < ICUT1
Grade B if module has less than 2% bad channels and I < ICUT2
Bad module otherwise

ICUT1 = 20 ? ? ?(TIB), 40 ? ? ??? ? ? ?and TEC) at 500V?
ICUT2 = 40 ? ? ?(TIB), 80 ? ? ??? ? ? ?and TEC) at 500V?

10 Testing at Module qualification centers

10.1 Initial tests (Deep tests):

IV-test, Basic-test(V_{std}), PSh-test(V_{std}), I-t(V_{max}), Basic-test(V_{max}), Basic-test(V_{std}), Pipe-test(V_{std}), Psh-test(V_{std}), B-test(V_{std}), L-test(V_{std})

Tests at V_{std} are to get the majority of the initial bad channels; the tests at V_{max} are made to check the performance at the maximum voltage and to stress the sensors; the final tests are made back to V_{std} to identify possible new bad channels coming after the voltage stress and the latest tests are made to identify all possible bad channels with emphasis to pinholes.

10.1.1 Bad channel definition:

A channel is defined as bad channel if it does not pass any of following rules:

1) $PL < P_i < PH$
2) $NL < N_i < NH$
3) $CL < C2_i < CH$
4) $BL < B_i < BH$
5) $LL < L_i < LH$

All cuts are defined at +-20% around the mean value for every single variable

deep-t flag	integer
T_{room}	real
t_{start}	integer
t_{end}	integer
Alg-ID*104 + Set-ID	integer
TS-H	real
MD-T	real array
IV data	real array
Basic-test data @	Vstd1
Pshi	real array
$CPRT_I$	real
$CPFT_i$	real
$CPPT_i$	real
$CPPA_I$	real

I-t data	real array
Basic-test data @	Vmax
Basic-test data @	Vstd2
Pipe-test data	
Pshi	real array
$CPRT_I$	real
$CPFT_i$	real
$CPPT_i$	real
$CPPA_I$	real
B-test data	
L-test data	

Deep test: LF information

deep-t flag	integer
T_{room}	real
t_{start}	integer
t_{end}	integer
Alg-ID*104 + Set-ID	integer
TS-H	real
MD-T	real array
IV data	real array
Basic-test data @	Vstd2
$CPPT_i$	real
$CPPA_I$	real
I-t max value	real
Basic-test data @	Vmax
Pipe-test short results	
B-test data	
L-test data	

Deep test: DB information

10.2 Long term tests

Then the long term test continues with a series of tests repeated many times along a period of few days with periods with the silicon sensor at about room temperature and others at low termperature.
These tests are done in the cold box [7].

Test performed are:

10.2.1 I-V, Basic-test, B-test, PSh-test @ T_{plate}= 25 C

10.2.2 I-V, Basic-test, B-test, , PSh-test @ T_{plate}= -20C

T_{plate} is measured on the cold plate inside the cold box.

long-t flag	integer
T_{room}	real
t_{start}	integer
t_{end}	integer
Alg-ID*104 + Set-ID	integer
Long term data @	t=0
Long term data @	t=? t
Long term data @	t=2 ? t
Long term data @	t=3 ? t
……	
…….	
Long term data @	t=N ? t

Long term: LF information

TS-Hi	real array
TS-Ti	real array
MD-Ti	real array
IV data	real array
Basic-test data @	Vstd1
Pshi	real array
$CPRT_I$	real
$CPFT_i$	real
$CPPT_i$	real
$CPPA_I$	real
B-test data	

Long term data block

long-t flag	integer
T_{room}	real
t_{start}	integer
t_{end}	integer
Alg-ID*104 + Set-ID	integer
Long term data @	Tplate= 25C t=0
Long term data @	Tplate=-20C t=? t
Long term data @	Tplate=-20C t=(N-1) ? t
Long term data @	Tplate= 25C t=N ? t

Long term: DB information

10.2.3 Bad channel definition:

A channel is defined as bad channel if it does not pass any of following rules at the end of the long term test:

1) $PL < P_i < PH$
2) $NL < N_i < NH$
3) $CL < C2_i < CH$
4) $BL < B_i < BH$

10.2.4 Module grade definitions:

Grade A if module has less than 1% bad channels, and I < ICUT1
Grade B if module has less than 2% bad channels and I < ICUT2
Bad module otherwise

ICUT1 = 20 ? ? ?(TIB), 40 ? ? ??? ? ? ?and TEC) at 500V?
ICUT2 = 40 ? ? ?(TIB), 80 ? ? ??? ? ? ?and TEC) at 500V?

11 List of possible failures

It is important to make a list of possible non-conformity. In the following a list of possible problems is attempted. This list is preliminary and will be updated according to the experience gained with M200 and preproduction. A severity flag has to be given for each non-conformity.

Special care has to be taken during M200, to improve the finding and identification of the different kinds of faults, especially at the different level of assembly to enact immediate repairs. The software must be able to detect the faults and give strict orders to the operator. The table 7 is an attempt to identify the fault type for single channel problems and includes a possible repair.

Problems affecting the entire module:

- m.1) APV25/MUX/PLL not responding to I_2C correctly
- m.2) DCU not responding to I_2C correctly
- m.3) APV25 bad header
- m.4) Sensor high leakage current
- m.5) Noisy hybrid
- m.6) Noisy sensors

Problems affecting single channels at hybrid level

- h.1) noisy channel
- h.2) dead channel
- h.3) bad gain
- h.4) saturated channel
- h.5) faulty shaper
- h.6) misbehaving pipelines cells

Problems affecting single channels at module level

- s.1) noisy strip
- s.2) shorted
- s.3) unconnected strip
- s.4) pinhole
- s.5) saturated strip
- s.6) broken strip
- s.7) strip in breakdown at V_{std}
- s.8) strip in breakdown at V_{max}

	Fault type	Tag	
s.1	Noisy strips	Ni>NH	
s.2	Shorted strips	N neighbour strips have Identical behaviour with respect to Pi, Ni, Ci	Check bonding
s.3	Unconnected strips	High but stable noise, no response to B, Light-shot or Light-continuous; with two arrays of LED we are able to determine, a missing bond occurred between PA-sensor1 or sensor1-sensor2	Rebond, if possible
s.4	Pinholes	Noise increases linear with the level of injected leakage current via the continuous light of the LEDs	Remove bond
s.5	Saturated strip	Saturated channel, possible pinhole if strongly light dependent	Remove bond
s.6	Broken strips	See s.3	Check sensor-sensor bond
s.7	Strip in breakdown at V_{std}	High noise at V_{std}	Unbond?
s.8	Strip in breakdown at V_{max}	High noise at V_{max}	Unbond?

Table 7: list of module channels non-conformities

12 References

[1] Reference to FHIT set-up

[2] ARC system:
http://www.physik.rwth-aachen.de/group/IIIphys/CMS/tracker/index.htm

[3] Reference to CMS-like set-up

[4] APV25-S1 User Guide Version 2.2 by Laurence Jones, RAL Microelectronics Design Group. Available via www.te.rl.ac.uk/med

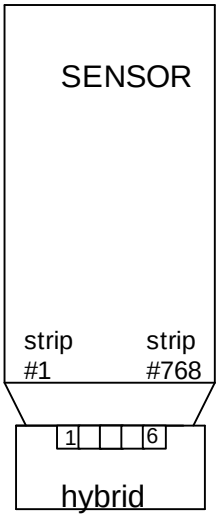
[5] MUX settings reference

[6] PLL settings reference

[7] Wien cold box:
wwwhephy.oeaw.ac.at/u3w/f/friedl/www/coolingbox/welcome.html

13 Appendix A: APV numbering scheme

The convention for channel numbering should follow the physical location of channels in the silicon sensors, starting from the left to the right, and should be the same for all module geometries. This implies that the sensor numbering might be different from the module channel numbering.



14 Appendix B: check sheet for the optical inspection (operator use)

Operator:	
Stage of assembly:	Institute:
Sensor ID1:	Sensor ID2:
Hybrid ID:	Module ID:

Defect types (examples):

Missing bond, ripped off bond, row of bonds (number), scratch (size), colouring, residuals, broken edge, broken (part), broken line, loose (part), dirt, etc..

Positions:

?? Hybrid
- ✍ APV#
- ✍ PLL
- ✍ MUX
- ✍ Ceramic

?? Frame
- ✍ Left leg
- ✍ Right leg
- ✍ Base

?? Cable
- ✍ HV
- ✍ Hybrid

?? Sensor
- ✍ Sensor 1
- ✍ Sensor 2

Detailed description: