Technical Information Manual

Revision n. 1

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MOD. A 509

CDF - SVXII
MULTISOURCE
PWS BOARD

NPO:
00102/98:**A509x.MUTx/01**

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1. General description

1.1. Functional description of the board

The Model A509 CDF – SVXII Power Supply Board has been specially designed for the CDF Silicon Vertex Detector at Fermilab.

The board is housed in an 8TE-wide, 6U-high mechanics to be inserted in the SY527 system mainframe. Its basic function is to deliver a set of floating voltages to drive a detector's sector which consists of a Port Card and five silicon ladders (Layer 0 through Layer 4). Moreover, the board has a monitoring circuit of output voltages, currents and status and associated control and protection circuits.

The board has been designed so that any fault in the supply of one layer will not affect the operation of any other layer. Similarly, failure in one sector of the detector will not affect the operation of any other sector.

To supply each sector of the detector the module delivers the following output floating voltages:

A) *To the Port Card*:

- **+5VDOIM**, differential low voltage with Line Drop Recover (SENSE line) and both voltage and current settings (<+8 V, <2.8 A);
- **+2VDOIM**, differential low voltage with Line Drop Recover (SENSE line), with both voltage and current settings (<+3.5 V, -1.7 A<ISET<0 A);
- **DTERM**, differential low voltage with Line Drop Recover (SENSE line), with both voltage and current settings (<+3.5 V, -0.15 mA<ISET<0.15 mA);

B) *To the Layer 0 through 4*:

- **DVDD**, differential digital low voltages to the front-end electronics of the Layer 0 through 4 with Line Drop Recover (SENSE line) and with both current and voltage settings (<+8 V, <0.6 A ÷ 2.0 A depending on the layer). The DVDD voltages and currents can be set independently for each of the five layers.
- **AVDD**, differential analog low voltages to the front-end electronics of the Layer 0 through 4 with Line Drop Recover (SENSE line) and with both current and voltage settings (<+10 V, <0.6 A ÷ 2.1 A depending on the layer). The AVDD voltages and currents can be set independently for each of the five layers.
- **VBIAS**, differential high voltages to bias the silicon detector ladder of Layer 0 through 4 with both voltage and current settings (<+250 V, <5 mA). The VBIAS voltages and currents can be set independently for each of the five layers.

In the whole, the module houses 18 independent floating power supply channels: 3 low voltage channels to supply the Port Card and 15 channels to supply the five layers. All VBIAS voltages are insulated up to 400 V from the ground of the mainframe, while AVDD and DVDD voltages are insulated up to 60 V.

Table 1.1 – Voltage and current values for the output channels

	Output	VSET (*)	Vres	VMAX	IMAX	Ires
To the Port Card	**+5VDOIM**	+5.0 V	> 8 bits	+8.0 V	2.8 A	> 8 bits
	+2VDOIM	+2.0 V	> 8 bits	+3.5 V	-1.7 A	> 8 bits
	DTERM	+2.5 V	> 8 bits	+3.5 V	±0.15 A	> 8 bits
To the Layers 0...4	**DVDD**	+5.0 V	> 8 bits	+8.0 V	0.6 A (layer 0)	> 8 bits
					0.9 A (layer 1)	
					1.5 A (layer 2)	
					1.5 A (layer 3)	
					2.0 A (layer 4)	
	AVDD	+7.0 V	> 8 bits	+10.0 V	0.6 A (layer 0)	> 8 bits
					0.9 A (layer 1)	
					1.5 A (layer 2)	
					1.5 A (layer 3)	
					2.1 A (layer 4)	
	VBIAS	0 ÷ +250 V	> 8 bits	+250 V	5 mA (layer 0…4)	> 12 bits

(*) for all the low voltages the voltage values shown in the Table are as measured at the remote sensing point.

Both the low voltage and high voltage channels have the maximum current **ISET** remotely programmable, while the maximum voltage (**VMAX hardware**) can be locally adjusted by means of trimmers placed on the Printed Circuit Board (PCB). The high voltage channels VBIAS have also the operating voltages **VSET** independently programmable in the range 0 ÷ +250 V for each of the five layers, while for the low voltage channels the operating voltages can be locally adjusted via the relevant trimmers on the PCB.
The ISET values of the channels, which are programmable, represent a "software controlled" hardware protection on the channel currents: the channel cannot draw a current higher than its programmed limit (**Board with programmable current hardware protections**).

The voltage and current values of both the low voltage and high voltage channels are summarised in Table 1.1, p.7. The local adjustment of the VMAX and VSET parameters via trimmers is described in § 3.2, p.19 (for the low voltage channels the VSET parameter is adjusted via trimmers, while for the VBIAS channels it can be programmed).

All output voltage channels, except for the VBIAS ones, have **Remote Sensing Lines** (SENSE lines) to take into account the voltage drop over the cable. For details please refer to § 4.6, p.32.

The power supply channels turn on and off in sequence one with respect to the other. The **Power-On Sequence** is as follows:

1. Turn on +5VDOIM and +2VDOIM with a <2-ms ramp;
2. Turn on a Layer in the following sequence:

- Turn on DVDD with a <10-ms ramp;
- Wait for 13 ms;
- Turn on AVDD with a <10-ms ramp;
- Turn on VBIAS. Program proper VBIAS voltage (ramp-up);

3. Turn on DTERM with a <10-ms ramp.

All ramp-down times depend on the load: the above ramp-down values were obtained with a load current equal to 80% of FSR.
This Power-On sequence is followed during normal operation, during fault trips (to the extent possible), and when the module is turned off in response to an external disable signal. The Power-Off sequence is in reverse order with respect to the Power-On sequence. For details please refer to § 4.3, p.29.

The **TRIP** of a supply channel can be caused by Over-Current, Over-Voltage or Under-Voltage conditions. The TRIP condition causes the channel to be switched off.
The Over-Current trip protection is of the constant current type, i.e. before being switched off the channel behaves like a current generator. The Over-Voltage trip protection is done by clamping to the maximum voltage VMAX and then turning off the channel. The Under-Voltage trip protection is done by turning off the channel.
TRIP condition is signalled via six TRIP output signals, corresponding to each of the five layers and to the Port Card. If a TRIP condition is detected, the exact condition which caused the TRIP is recorded in the status register until the module is reset.
If any power supply channel of one layer is tripped, all the power supply channels relative to that layer are shut-down sequentially. If any power supply channel of the Port Card is tripped, the complete module is shut-down according to the Power-Off sequence. Further details on the TRIP conditions can be found in § 4.7, p.33.

An active high REMOTE ENABLE input connector allows to enable remotely the power generation on the board. Manual ENABLE is also possible by inserting the relevant jumper on the circuit board. No power supply channel can be turned on unless the board is enabled either manually or remotely. If the board is remotely enabled, any supply channel which is ON is tripped as soon as the ENABLE signal is dropped.

1.2. Technical specification table

Table 1.2 - Technical specifications of the Mod. A509 CDF - SVXII Power Supply Board

Packaging	8TE-wide, 6U-high module
Power consumption (*)	270 W
Operating temperature	10°-45°C
Control mainframe	SY 527 system
Number of output channels	18
Polarity	Floating voltages
Output operating voltages (**)	• +5 V (+5VDOIM), locally adjustable via trimmer; • +2 V (+2VDOIM), locally adjustable via trimmer; • +2.5 V (DTERM), locally adjustable via trimmer; • +5 V (DVDD), locally adjustable via trimmer; • +7 V (AVDD), locally adjustable via trimmer; • 0 ÷ +250 V (VBIAS), remotely programmable.
Maximum Voltage (VMAX hardware)	See Table 1.1, p.7.
Maximum Current (ISET)	See Table 1.1, p.7.
Voltage ripple	10 mV_{pp}
Voltage set/monitor resolution (*)	• > 8 bits on low voltage channels • > 12 bits on high voltage channels (VBIAS)
Current set/monitor resolution (*)	> 8 bits on all channels
Remote sensing lines	On all low voltages
Output voltage stability	<1%

(*) maximum load on all channels.
(**) see Table 1.1, p.7 for further details on voltage and current settings.

2. Specifications

2.1. Packaging

The module is housed in a 8TE-wide, 6U-high mechanics.

2.2. Power requirements

Power consumption is 270 W with maximum load on all channels.

2.3. Front panel

The front panel of the A509 power supply board is shown in Fig. 2.1, p.13.
A detailed description of the its external components can be found in following subsections.

2.4. External connections

The location of all components of the front panel is shown in Fig. 2.1, p.13.
The function and electro-mechanical specifications of the external connectors are listed in the following subsections.

2.4.1. SENSES Connector

Function:
It delivers all the sensed voltages, i.e. the voltages measured directly on the load as shown in Fig. 4.2, p.32 so as to be not affected by voltage drops. Refer to § 4.6, p.32 for details on the Sensing lines.
Mechanical specifications:
36-pin Mini D Ribbon female connector (3M, DR 10236-6212JL).
Electrical specifications:

ASP_LY0…4/ ASN_LY0…4:	*differential signal*; sensing of the analog voltage AVLY0…4 to the front-end electronics for the layer 0 through 4.
DSP_LY0…4/ DSN_LY0…4:	*differential signal*; sensing of the digital voltage DVLY0…4 to the front-end electronics for the layer 0 through 4.
5VDOIMS_P/ 5VDOIMS_N:	*differential signal*; sensing of the +5V digital voltage to the port card.
2VDOIMS_P/ 2VDOIMS_N:	*differential signal*; sensing of the +2V digital voltage to the port card.
DTERMS_P/ DTERMS_N:	*differential signal*; sensing of the DTERM voltage to the port card.
ENABLE, EN_1:	ENABLE-loop input/output pins (refer to § 4.2, p.28).
SHIELD_1:	cable shield which can be optionally connected to the common terminal (COMMON).
EARTH:	terminal connected to the earth.

Pin assignment is given in Fig. 2.2, p.14.

2.4.2. LOW VOLTAGE Connector

Function:
It provides all the low voltages both for the Port Card and for the layers.
Mechanical specifications:
78-pin, subminiature-D female connector (Positronic, ODD 78F3S600X); to be matched with a 78-pin subminiature-D male connector (Positronic, ODD 78M20Z0Z).
Electrical specifications:

AVP_LY0…4/AVN_LY0…4: *differential output voltage*; analog voltage to the layer 0 through 4.

DVP_LY0…4/DVN_LY0…4: *differential output voltage*; digital voltage to the layer 0 through 4.

5VDOIM_P/5VDOIM_N: *differential output voltage*; +5 V voltage to the Port Card.

2VDOIM_P/2VDOIM_N: *differential output voltage*; +2 V voltage to the Port Card.

DTERM_P/DTERM_N: *differential output voltage*; DTERM voltage to the Port Card.

EN_1, EN_2: ENABLE loop input/output pins (refer to § 4.2, p.28).

SHIELD_2: cable shielding to be optionally connected to the common terminal COMMON (not accessible from the front panel).

EARTH: terminal connected to the earth.

Pin assignment is given in Fig. 2.3, p.15.

2.4.3. HIGH VOLTAGE Connector

Function:
It provides the silicon detector bias differential voltages VBPLY0…4/VBNLY0…4 to the layer 0 through 4. The bias voltages are programmable from 0 to 250 V and are set symmetrically about a reference voltage VRFLY0…4 which can be externally supplied.
Mechanical specifications:
25-pin Subminiature D type female connector (AMP, 1-745967-9))
Electrical specifications:

VBP_LY0…4/VBN_LY0…4: *differential output voltage*; bias voltage to the layer 0 through 4; it can programmed from 0 to 250 V and during normal operation is set symmetrically about a reference voltage VRF (see next entry) by using a resistive divider; the symmetrical position with respect to the VREF can be varied by changing the resistors of the divider which are accessible to the user. For details please refer to § 3.2.4, p.21.

VRF_LY0…4: reference voltage for the bias differential voltage of the layer 0 through 4; it can be externally supplied by connecting the relevant pins to the chosen reference voltage.

EN_2, EN_BOARD: ENABLE loop input/output pins (refer to § 4.2, p.28).

SHIELD_3: cable shielding to be optionally connected to the common terminal COMMON (not accessible from the front panel).

EARTH: terminal connected to the earth.

Pin assignment is given in Fig. 2.2, p.14.

2.4.4. TRIP Connector

Function:
It delivers the TRIP signals relative to the Layers 0 through 4 and to the Port Card. Moreover, the pin 7 is assigned to the ENABLE input signal as specified below. Refer to § 4.7, p.33 for details on the TRIP conditions.
Mechanical specifications:
15-pin Subminiature D type female connector (AMP, 1-747299-6)
Electrical specifications:

TRP_LY0…4: *active-low TTL output signal*; TRIP signals for the layer 0…4; this signal is asserted high as long as the supplies of the relevant layer are on; it is asserted low as soon as the supplies are tripped.

TRP_PC: *active-low TTL output signal*; TRIP signal for the Port Card; this signal is asserted high as long as the supplies of the Port Card are on; it is asserted low as soon as the supplies are tripped.

ENABLE: *active-high TTL input signal*; remote ENABLE input signal. This pin of the TRIP connector is ORed with the REM ENABLE connector. Refer to § 4.2, p.28 for details.

SHIELD_4: cable shielding to be optionally connected to the common terminal COMMON (not accessible from the front panel).

EARTH: terminal connected to the earth.

Pin assignment is given in Fig. 2.2, p.14.

2.4.5. REM ENABLE Connector

Function:
It allows to enable remotely the module via a suitable input signal. Refer to § 4.2, p.28 for details on the ENABLE of the board.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications:

ENABLE: *active-high TTL input signal*; remote ENABLE input signal. It is ORed with the signal of the ENABLE pin of the TRIP connector. Refer to § 4.2, p.28 for details.

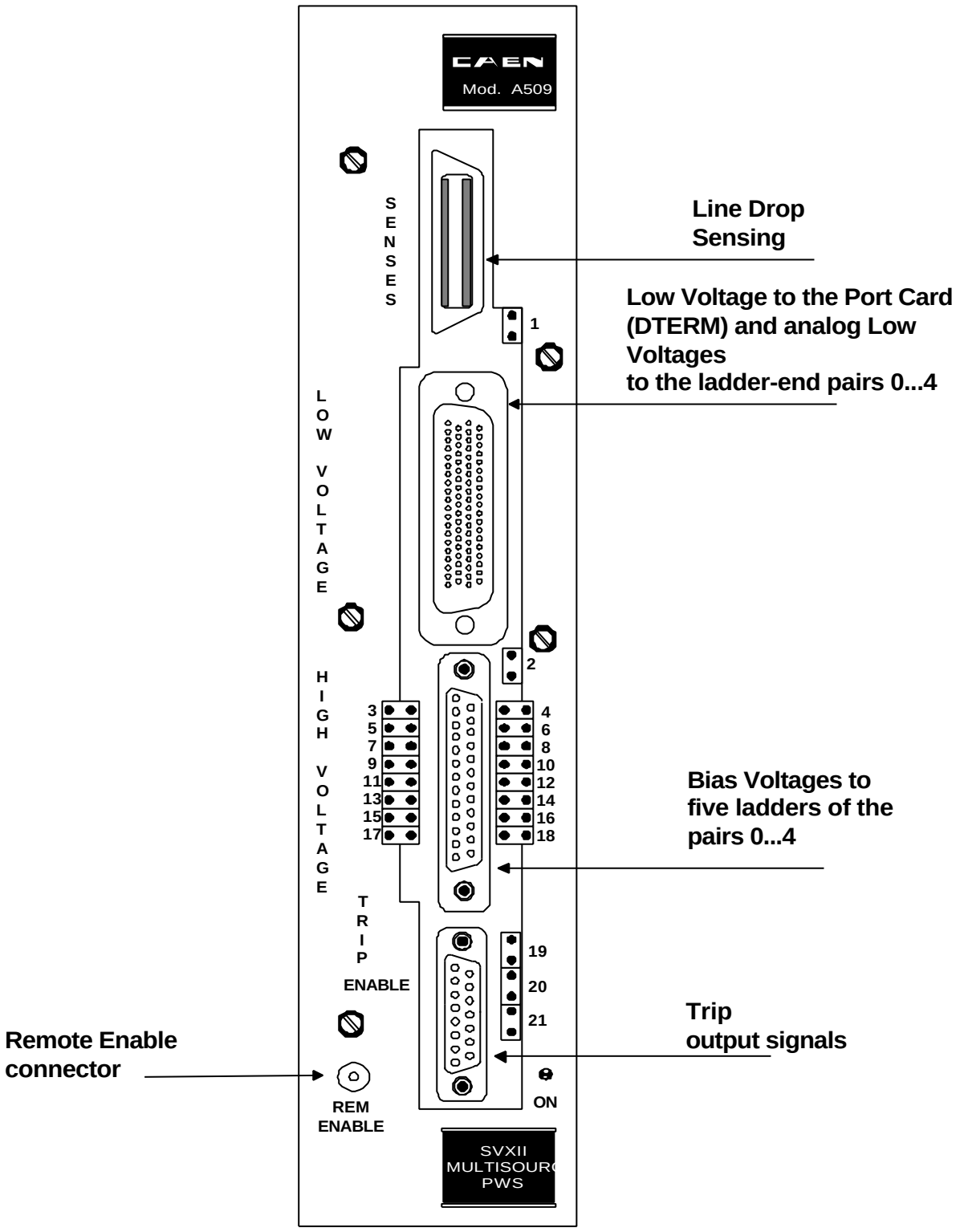
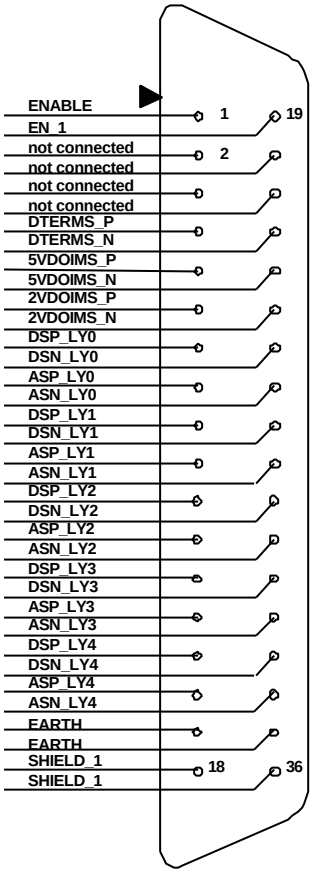
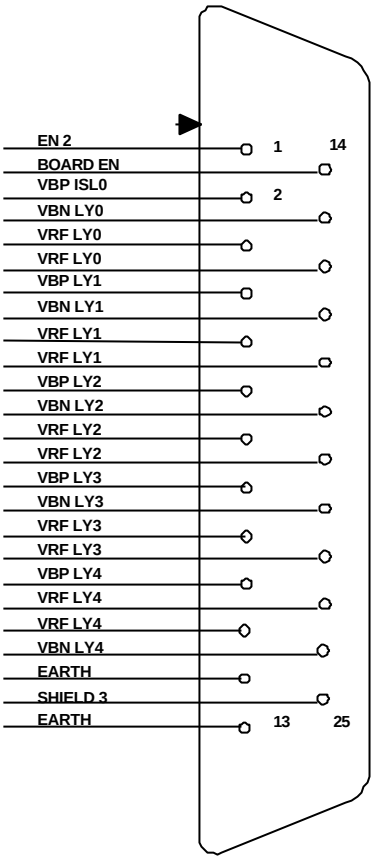


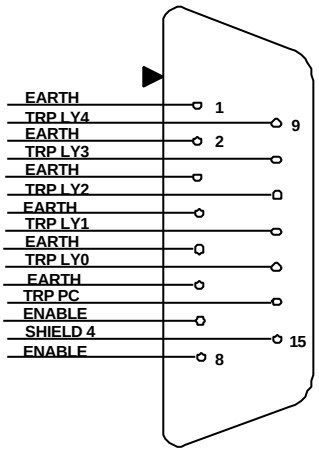
Fig. 2.1 – Front panel of the Mod. A509 Power Supply Board



SENSES CONNECTOR



HIGH VOLTAGE CONNECTOR



TRIP CONNECTOR

Fig. 2.2 – Pin assignment of the Senses, Trip and High Voltage connectors

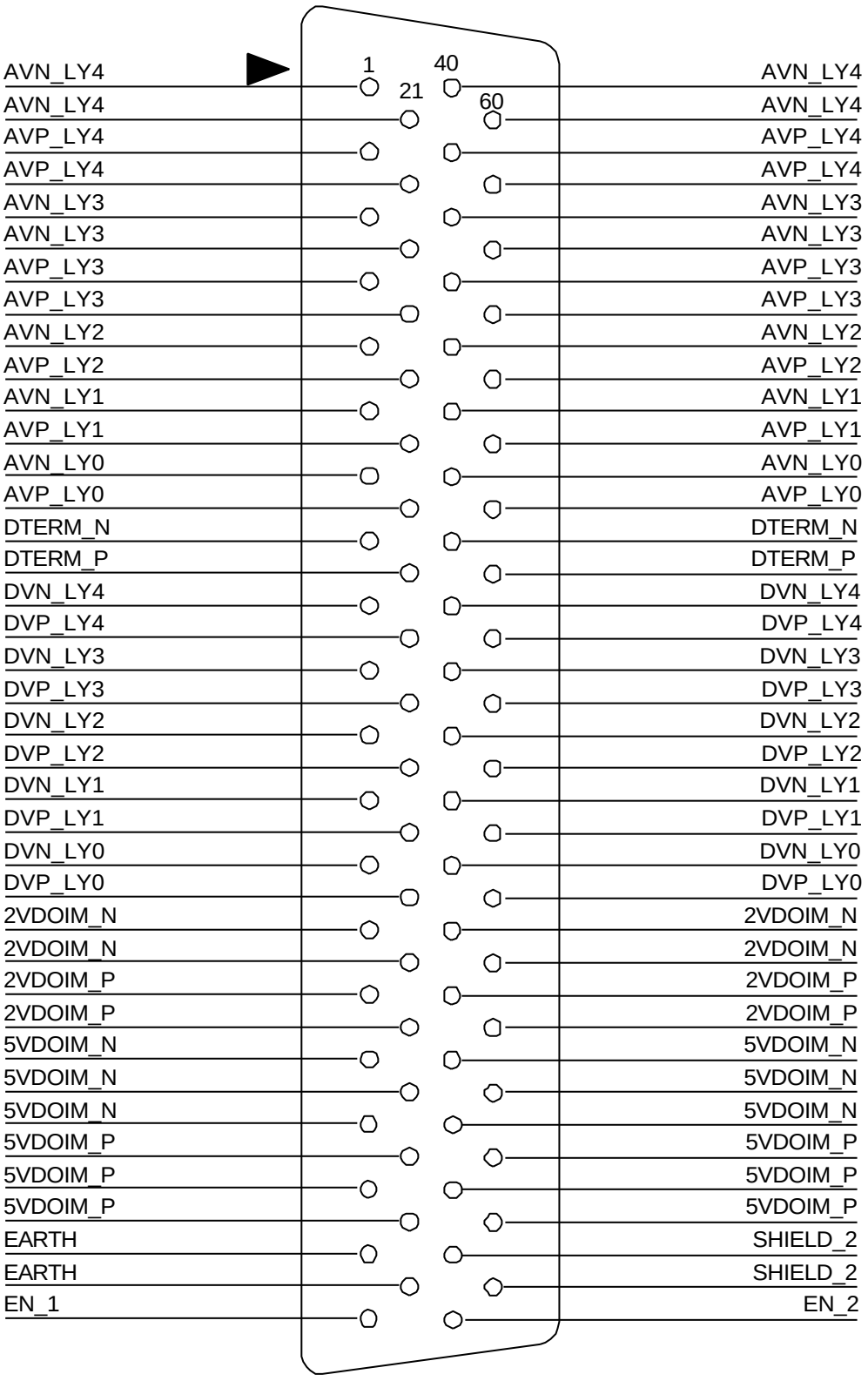


Fig. 2.3 – Pin assignment of the Low Voltage connector

2.5. Other components

2.5.1. Displays

PWR ON: *Type:* red LED.
Function: it lights up when at least one channel is ON.

Refer to Fig. 2.1, p.13 for its location on the front panel.

2.5.2. Jumpers

N.B.: THESE JUMPERS ARE LINKED DIRECTLY TO HV PARTS OF THE BOARD

Front panel jumpers *(plexiglass protection covers are placed above these jumpers refer to Fig. 2.1, p.13 and to § 3.3, p.23 for settings):*

J3…J17: *Function:* they optionally allow the VBIAS high voltages VBP_LY0…4/ VBN_LY0…4 and the relevant reference voltages VRF_LY0…4 to be connected to the common terminal COMMON.

J1, J2, J18, J19: *Function:* they optionally allow the SHIELD_1…4 cable shields to be connected to the common terminal COMMON.

J20: *Function:* it optionally allows the common terminal COMMON to be connected to the earth (EARTH).

J21: *Function:* if inserted, it allows to disable the ENABLE-loop, i.e. the board can be enabled via the ORed remote ENABLE input signal independently from the fact that the other Sense, Low Voltage and High Voltage connectors are inserted or not. Refer to § 4.2, p.28 for further details on the ENABLE-loop.

PCB jumpers *(refer to Fig. 3.2, p.22, Fig. 3.3, p.23 and to § 3.2, p.19 for settings):*

J18: *Function:* it allows to select the monitoring full scale (either 0÷0.05 mA or 0÷5 mA) of the maximum current ISET for each VBIAS_LY0…4 high voltage channel. It is placed on the High Voltage board (see Fig. 3.2, p.22).

J72: *Function:* it allows to enable the board manually. This jumper overrides the ORed remote ENABLE signals from the REM ENABLE and TRIP connectors. Refer to Fig. 3.3, p.23 and to § 4.2, p.28 for further details on board enable.

2.5.3. Resistors

(Refer to Fig. 3.2, p.22 for the exact location of these resistors on the PCB and to §3.2, p.19 for their settings).

R88, R101: *Function:* they allow to arrange differently, with respect to the default configuration, the resistive dividers which set the bias differential voltages VBP_LY0…4 and VBN_LY0…4 about the relevant reference voltage VRF_LY0…4. In the default configuration the bias voltages are set symmetrically about the relevant reference voltages. These resistors are placed on the High Voltage board (see Fig. 3.2, p.22).

2.5.4. Trimmers

(Refer to Fig. 3.1, p.21 for the location of these trimmers on the PCB and to §3.2, p.19 for their settings).

Trimmers on the Low Voltage boards and VDOIM board *(refer to Fig. 3.1, p.21)*

P1, P2: *Type:* 12 screwdriver trimmers with relevant test points.
Function: they allow to adjust the hardware maximum voltage VMAX for the relevant channel (DVDD 0…4, AVDD 0…4, +2VDOIM or +5VDOIM), according to Fig. 3.1, p.21.

P3, P4: *Type:* 12 screwdriver trimmers with relevant test points.
Function: they allow to adjust the VSET for the relevant channel (DVDD 0…4, AVDD 0…4, +2VDOIM or +5VDOIM), according to Fig. 3.1, p.21.

Trimmers on the High Voltage boards and DTERM board *(refer to Fig. 3.1, p.21)*

P8: *Type:* 6 screwdriver trimmers with relevant test points.
Function: they allow to adjust the hardware maximum voltage VMAX for the relevant bias channel (trimmers on the five High Voltage boards) and for the DTERM channel (trimmer on the Port Card board), according to Fig. 3.1, p.21.

P9: *Type:* 1 screwdriver trimmer, located on the DTERM board, with relevant test points.
Function: it allows to adjust the VSET of the DTERM channel, according to Fig. 3.1, p.21.

3. Hardware installation and set-up

3.1. Safety information

This section contains the fundamental safety rules for the installation and operation of the A509 board.
Read thoroughly this section before starting any procedure of installation or operation of the product.

3.1.1. General safety precautions

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use the product only as specified. Only qualified personnel should perform service procedures.

3.1.1.1. Injury Precautions

N.B.: THIS MODULE CAN BE EMPLOYED ONLY WITHIN A SY 527 CRATE HAVING ALL SLOTS FILLED BY BOARDS OR BLANK PANELS.

Use Proper Power Cord and HV Cables.
To avoid fire hazard, use only the power cord and HV cables specified for this product.

Avoid Electric Overload.
To avoid electric shock or fire hazard, do not apply a voltage to a load that is outside the range specified for that load.

Avoid Electric Shock.
To avoid injury or loss of life, do not connect or disconnect cables while they are connected to a voltage source.

Ground the Product.
This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to any input or output terminals of the product, ensure that the product is properly grounded.

Do Not Operate Without Covers.
To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Use Proper Fuse.
To avoid fire hazard, use only the fuse type and rating specified for this product.

Do Not Operate in Wet/Damp Conditions.
To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere.
To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

3.1.1.2. Product Damage Precautions

Use Proper Power Source.
Do not operate this product from a power source that applies more than the voltage specified.

Provide Proper Ventilation.
To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures.
If you suspect there is damage to this product, have it inspected by qualified service personnel.

3.1.1.3. EC Certifications and Compliance

Use in conformity of the definition with fully equipped mainframe with fully closed slots by boards or dummy panels. Sufficient cooling and mains connection must be secured according to regulations. Admitted for powering by industrial mains only.

3.1.1.4. Terms in this Manual

These terms may appear in this manual:
WARNING:
Warning statements identify conditions or practices that could result in injury or loss of life.
CAUTION:
Caution statements identify conditions or practices that could result in damage to this product or other property.

3.1.2. Terms and Symbols on the Product

These terms may appear on the product:

- **DANGER** indicates an injury hazard immediately accessible as you read the marking.
- **WARNING** indicates an injury hazard not immediately accessible as you read the marking.
- **CAUTION** indicates a hazard to property including the product.

The following symbols may appear on the product:

DANGER

High Voltage

ATTENTION

Refer to Manual

3.2. Hardware settings

DANGER

CALIBRATION PROCEDURE REQUIRES ACCESSING TO HV PARTS OF THE BOARD. TO AVOID SEVERE INJURY HAZARDS THESE OPERATIONS MUST BE PERFORMED BY QUALIFIED PERSONNEL ONLY EMPLOYING INSULATED (³ 1000V) GLOVES.

3.2.1. Adjusting the VMAX hardware maximum voltages

All the hardware maximum voltages VMAX relative to each output channels can be adjusted via screwdriver trimmers located on the PCB. The trimmers are equipped with test points to monitor the voltage values.
Fig. 3.1 shows the location on the PCB for the VMAX trimmer of each channel. The trimmers located in the VDOIM and Low Voltage board areas are in fact accessible via through-holes. For each channel the range of values covered by the relevant trimmer is reported in Table 4.1, p.31.

3.2.2. Adjusting the VSET voltages of the low voltage channels

The VSET voltages relative to the low voltages (specifically +5VDOIM, +2VDOIM, DTERM, AVDD and DVDD voltages) can be adjusted via the relevant screwdriver trimmers. The trimmers are equipped with test points to monitor the voltage values.
Fig. 3.1 shows the location on the PCB of the VSET trimmer of each channel. The trimmers located in the VDOIM and Low Voltage board areas are in fact accessible via through-holes. For each channel the range of values covered by the relevant trimmer is reported in Table 4.1, p.31.

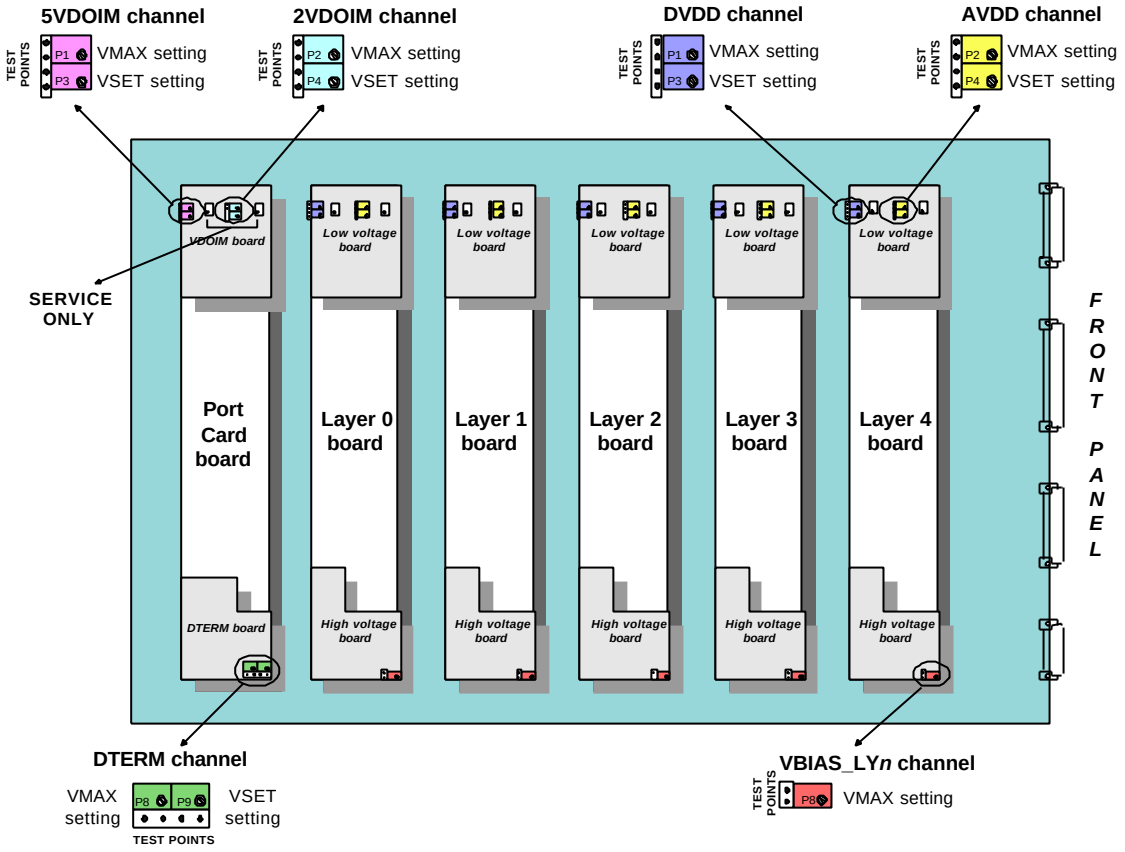


Fig. 3.1 –Trimmer settings for the low voltage channels and the VBIAS_LY channels

3.2.3. Selecting the ISET monitoring full scale for the VBIAS channels

The selection of the monitoring full scale for the maximum current ISET of the bias high voltage channels is made through the relevant two-position jumper located on the High Voltage board relative to each layer.
The location of the jumper on the PCB and its setting are shown in Fig. 3.2, p.22.

Jumper inserted in Position A → **0 ¸ 0.05 mA** monitoring scale;
Jumper inserted in Position B → **0 ¸ 5 mA** monitoring scale.

Since the position of this jumper is NOT tested by the board circuitry, the software will show ALWAYS the same monitoring scale, specifically the default one which is 0 ÷ 5 mA. Consequently, it is up to the user to divide the readout by 10 if the jumper is in position A.

3.2.4. Setting the VBIAS voltages asymmetrically about the VREF voltages

In the default configuration the VBIAS differential voltages (VBP_LY0…4 and VBN_LY0…4) are set symmetrically about the relevant reference voltage VRF_LY0…4 by means of a resistive divider. The resistors which constitute the divider have been left accessible to the user in order to change them in case the user wants to set the bias voltages differently with respect to the reference voltage. In order to access to the resistors the user must remove the dissipator plate: then the resistors can be replaced by using a soldering iron.

Fig. 3.2, p.22 shows the location of the resistors on the PCB. Refer to §2.5.3, p.17 for resistor specifications.

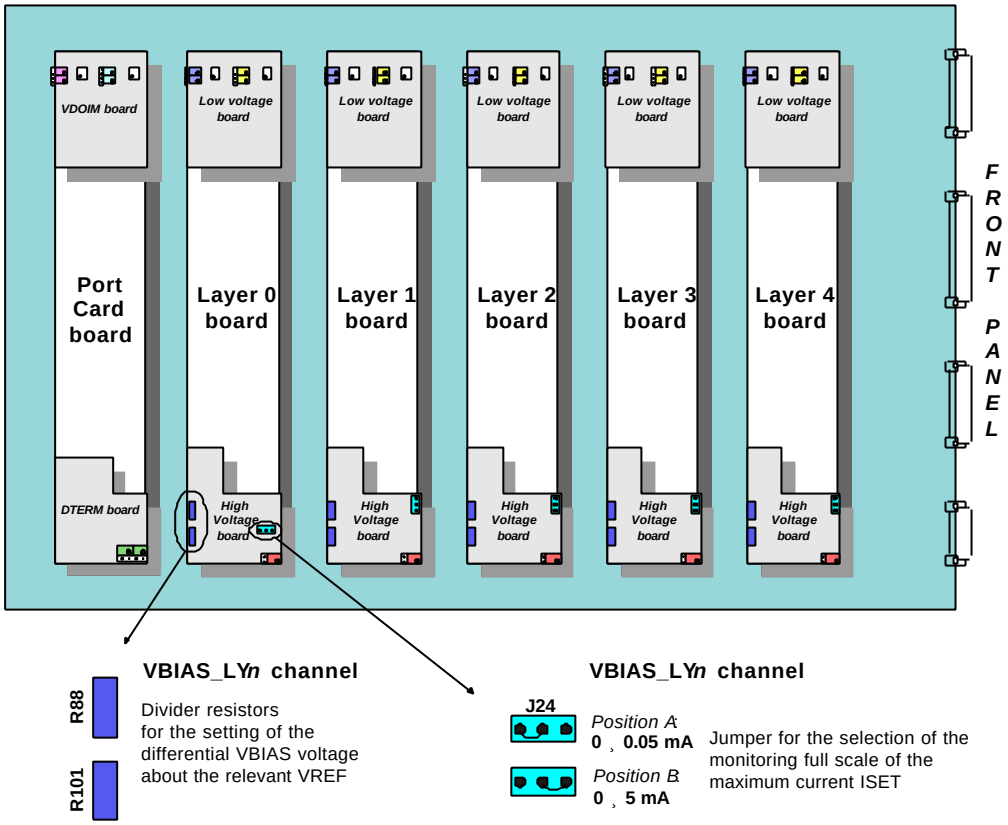


Fig. 3.2 – Divider resistors and jumper settings for the VBIAS_LY0…4 channels

3.2.5. Local, fixed ENABLE of the board

The board can be enabled locally by inserting the relevant jumper (J72) located on the PCB, as shown in Fig. 3.3, p.23. In this way the board will be enabled anyway, independently from the level of the ENABLE signals coming from the front panel connectors. It means that this jumper overrides the remote ENABLE signals, as illustrated in Fig. 4.1, p.28.

Jumper inserted	→	**local enable mode**: if the jumper is inserted, the board is always enabled, independently from the level set on the remote ENABLE signals;
Jumper NOT inserted	→	**remote enable mode**: the board can be enabled by sending one of the remote ENABLE signals.

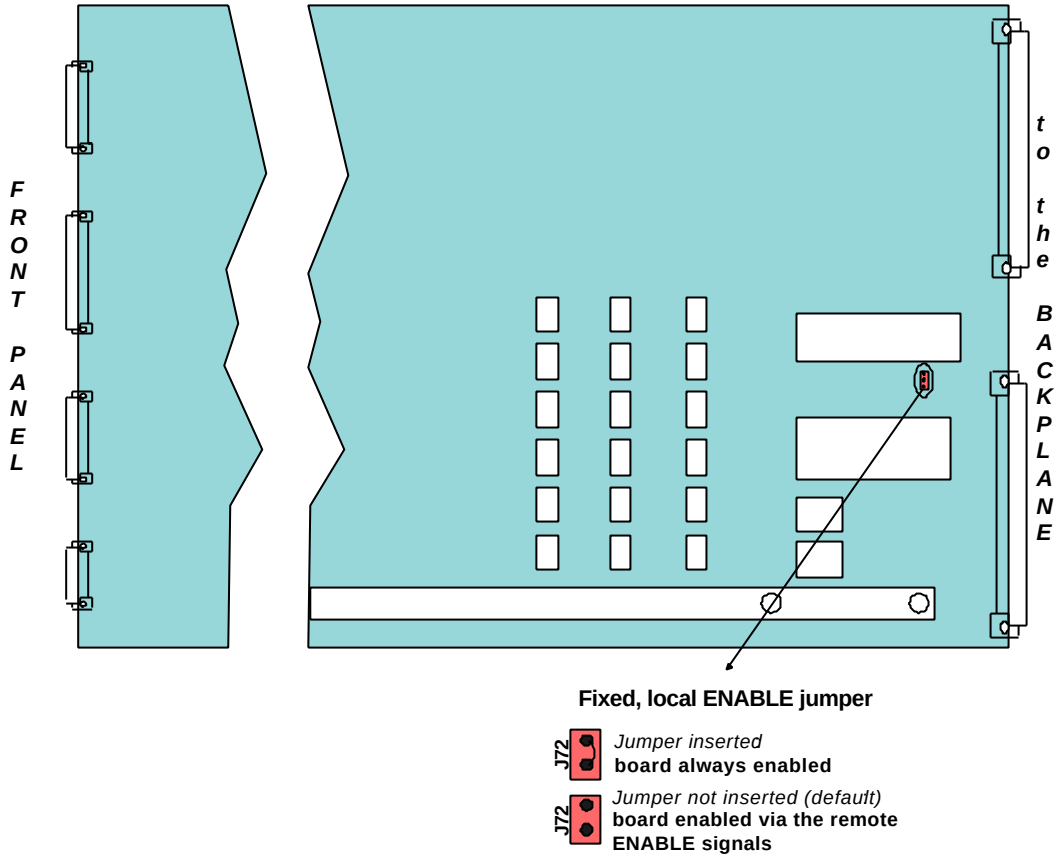


Fig. 3.3 – Main printed circuit board: jumper setting for local fixed ENABLE mode

3.3. Jumper settings on the front panel

DANGER

REMOVING PLEXIGLASS PROTECTION COVERS GIVES ACCESS TO HV PARTS OF THE BOARD. TO AVOID SEVERE INJURY HAZARDS JUMPERS SETING MUST BE PERFORMED BY QUALIFIED PERSONNEL ONLY EMPLOYING INSULATED (³ 1000V) GLOVES.

N.B.: IT IS STRONGLY RECOMMENDED TO PERFORM JUMPERS SETTING WHEN THE SY 527 SYSTEM IS TURNED OFF.

3.3.1. Connecting VBIAS or VREF to earth

A set of 15 jumpers optionally allow the VBIAS high voltages VBP_LY0…4/ VBN_LY0…4 and the relevant reference voltages VRF_LY0…4 to be connected to earth.
The jumper are located on the front panel on the rear part of the front panel (Fig. 2.1, p.13), while their setting is described in Table 3.1, p.26.

Jumper inserted	→	the relevant VBIAS+ or VBIAS- or VREF is grounded;
Jumper NOT inserted	→	the relevant VBIAS+ or VBIAS- or VREF is not grounded.

WARNING: The user must pay attention not to insert both the jumper relative to the positive VBIAS and that relative to the negative VBIAS for the same channel: the insertion of both these jumpers will cause a short circuit.

WARNING

DO NOT INSERT BOTH THE VBIAS+ AND THE VBIAS- JUMPER OF THOSE RELATIVE TO THE SAME CHANNEL!

3.3.2. Connecting cable shielding to the common terminal COMMON

A set of 4 jumpers (J1, J2, J18, J19) optionally allow the shielding of each cable (SHIELD_1…SHIELD_4) to be connected to the COMMON. The latter is a common terminal which is not accessible from the front panel.
The jumpers are located on the front panel (Fig. 2.1, p.13), while their setting is described in Table 3.2, p.26.

Jumper inserted	→	the relevant shield is connected to the common terminal (COMMON);
Jumper NOT inserted	→	the relevant shield is not connected to the common terminal (COMMON).

3.3.3. Connecting the common terminal COMMON to the earth

The J20 jumper optionally allows to connect the common terminal COMMON to the earth.
The jumper is located on the front panel (Fig. 2.1, p.13), while its setting is described in Table 3.2, p.26.

Jumper inserted	→	the common terminal COMMON is connected to the earth (EARTH);
Jumper NOT inserted	→	the common terminal COMMON is not connected to the earth (EARTH).

3.3.4. Disabling the ENABLE-loop

The J21 jumper, if inserted, allows board enabling via the front panel ENABLE input signals (REM ENABLE connector or pin 7 of the TRIP connector), independently from the fact that the other front panel connectors are inserted or not.
This jumper overrides the ENABLE-loop. The ENABLE-loop is a protection foreseen in case a cable may be accidentally removed from the front panel: each front panel connector has two ENABLE pins (refer to § 2.4, p.10) which, if not inserted, cut the loop off and disable the board.
The jumper is located on the front panel (Fig.2.1, p.13), while its setting, described also in Table 3.2, p.26 is as follows:

Jumper inserted	→	**ENABLE-loop disabled**: if the jumper is inserted, the board can be enabled via the front panel ENABLE signals even if a front panel connector is not inserted;
Jumper NOT inserted	→	**ENABLE-loop enabled**: the board can be enabled via the front panel ENABLE signals only if the *SENSES, LOW VOLTAGE* and *HIGH VOLTAGE* connectors are inserted. If a connector is accidentally removed from the front panel, the board is automatically disabled.

Refer to § 4.2, p.28 for further details on the enable of the board.

Table 3.1 – Front panel jumper settings: VBIAS_LY and VREF_LY grounding

Jumper	Function
J3	Its insertion grounds VBP_LY0
J4	Its insertion grounds VBN_LY0
J5	Its insertion grounds VRF_LY0
J6	Its insertion grounds VBN_LY1
J7	Its insertion grounds VBP_LY1
J8	Its insertion grounds VRF_LY1
J9	Its insertion grounds VBP_LY2
J10	Its insertion grounds VBN_LY2
J11	Its insertion grounds VRF_LY2
J12	Its insertion grounds VBN_LY3
J13	Its insertion grounds VBP_LY3
J14	Its insertion grounds VRF_LY3
J15	Its insertion grounds VBP_LY4
J16	Its insertion grounds VBN_LY4
J17	Its insertion grounds VRF_LY4

Table 3.2 – Front panel jumper settings: ENABLE-loop, shield-common and common-earth connections

Jumper	Function
J1	Its insertion connects the SHIELD_1 (Senses connector) to the common terminal (COMMON)
J2	Its insertion connects the SHIELD_2 (Low Voltage connector) to the common terminal (COMMON)
J18	Its insertion connects the SHIELD_3 (High Voltage connector) to the common terminal (COMMON)
J19	Its insertion connects the SHIELD_4 (Trip connector) to the common terminal (COMMON)
J20	Its insertion connects the common terminal (COMMON) to the earth
J21	Its insertion allows board enabling via the front panel ENABLE input signals, independently from the fact that the other connectors are inserted or not (see also § 4.2, p.28)

3.4. Installation

The A509 board can be inserted in any of the slots of the SY527 system.
At Power-ON the SY527 system processor will scan all the slots inserted in the SY527 crate to find out where the module is plugged in and what kind of module it is.

Please note that the board can be inserted into or removed from the crate only after the system has been turned off. To extract the board from the crate, follow these steps:

1. Turn the crate off,
2. Remove all the cables from the front panel;
3. Extract the board from the crate.

CAUTION

BEFORE INSERTING OR REMOVING THE BOARD

TURN THE SY527 SYSTEM OFF AND REMOVE ALL CABLES

FROM THE BOARD FRONT PANEL!

4. Operating mode

The following Sections contain a description of the most peculiar operating features of the A509 board. For details on the operating modes of the SY527 system, please refer to the *User's Manual* of this product.

4.1. Software version for the SY527 system

The A509 board can be used **only with the Software Version 4.01 or later** for the SY527 system. Please refer to the *Software Version 4.01 Release Note* in the *User's Manual* of this product for details on the added features.

CAUTION

THE BOARD CAN BE USED ONLY WITH THE SOFTWARE VERSION 4.01 OR LATER FOR THE SY527 SYSTEM!

4.2. ENABLE of the board

The board can be enabled either locally via the relevant jumper on the PCB (see §3.2.5, p.22) or remotely by sending an active high TTL input signal either to the REM ENABLE input connector or to the relevant pin (pin 7, ENABLE) of the TRIP connector (see §2.4.4 and 2.4.5, p.12).
No power supply channel can be turned on unless the board is enabled. On the other hand, any supply channel which is On is tripped as soon as the board is disabled.
Fig. 4.1 shows an electrical diagram which explains the function of the various ENABLE components. If the ENABLE jumper is inserted, the board is enabled independently from the ENABLE signals send through the TRIP and REM ENABLE connectors. If the ENABLE jumper is not inserted, no power supply channel can be turned on unless the ENABLE signal (either on the REM ENABLE connector or on the TRIP one) is asserted. On the other hand, any supply channel which is On is tripped as soon as the ENABLE signal is dropped.

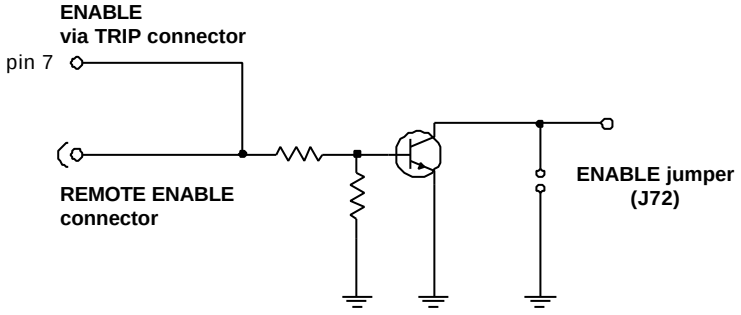


Fig. 4.1 – Electrical diagram of the ENABLE circuitry

The board is also equipped with an ENABLE-loop which acts as protection in case a connector may be accidentally removed from the front panel. Each front panel connector (except for the REM ENABLE and TRIP ones) has two pins (EN_n pins, see connector pin-outs in Fig. 2.2, p.14 and Fig. 2.3, p.15) which are looped with the ORed ENABLE signals from the REM ENABLE connector and the pin 7 of the TRIP connector. As a consequence, if any connector is removed from the front panel, the loop is cut off and the board is automatically disabled. This option (ENABLE-loop) can be disabled by inserting the relevant front panel jumper (J21). Refer to § 3.3.4, p.25 for details on its setting.

4.3. Power-ON/OFF Sequencing

The board has been designed so that the power supply channels turn on/off in sequence one with respect to the other. The Power-On Sequence is as follows:

1. Turn on +5VDOIM and +2VDOIM with a <2-ms ramp;
2. Turn on a Layer in the following sequence:
   - Turn on DVDD with a <10-ms ramp;
   - Wait for 13 ms;
   - Turn on AVDD with a <10-ms ramp;
   - Turn on VBIAS. Program proper VBIAS voltage (ramp-up);
3. Turn on DTERM with a <10-ms ramp.

All ramp-down times depend on the load: the above ramp-down values were obtained with a load current equal to 80% of FSR.
THIS SEQUENCE IS FOLLOWED INDEPENDENTLY FROM THE VALUE SET FOR THE TRIP PARAMETER VIA SOFTWARE.

The Power-On sequence listed above is followed during normal operation, during fault trips (to the extent possible), and when the module is turned off in response to an external disable signal. The Power-Off sequence is in reverse order with respect to the Power-On sequence.
Each ladder can be powered On/Off independently from the other ladders. If a ladder supply does not reach the nominal voltage value within 1 second, the sequence is disabled and the ladder goes through a Power-Off sequence.
The VBIAS, DVDD and AVDD channels, relative to one layer, are controlled together: a set of ON/OFF commands causes the three voltages to be turned on or off in sequence. Similarly, the +5VDOIM and the +2VDOIM channels are controlled together.

4.4. Set-up of the channel parameters

For all the output channels the VMAX parameter can be locally adjusted via the relevant trimmers as explained in § 3.2, p.19. The VMAX parameter can be set within a range of values which depends on the output channel, as shown in Table 4.1, p.31. Moreover, test points, accessible to the user, allow to monitor the VMAX settings via a Digital VoltMeter (DVM).

For all the low voltage channels the VSET parameter can be locally adjusted via the relevant trimmers as explained in § 3.2, p.19. The trimmers are equipped with test points for the monitoring of the VSET settings.

For the bias high voltage channels VSET can be remotely programmed by using the software interface of the SY527 system. Refer to the *User's Manual* of this product for details.
Fig. 3.1, p.21 shows the location of both the VMAX trimmers and the VSET ones, together with the relevant test points, on the PCB.

The ISET parameter is remotely programmable for all the output channels by using the software interface of the SY527 system. Refer to the *User's Manual* of this product for details. The ISET maximum currents for the bias channels have two different monitoring full scales (0 ÷ 0.05 mA and 0 ÷ 5 mA) which can be selected via the relevant jumper located on the PCB (see Fig. 3.2, p.22).

Table 4.1, p.31 summarises the setting ranges, which depend on the type of output channel, for the VMAX, VSET and ISET parameters.

Table 4.2, p.31 summarises both the channel parameters which can be adjusted locally via trimmer and the parameters which can be programmed remotely by using the SY527 system software interface.

Table 4.1 – Setting range for the VMAX, VSET and ISET parameters

	Output	VMAX	VSET (*)	ISET
To the Port Card	+5VDOIM	0 ÷ +8.0 V	0 ÷ +8.0 V	0 ÷ 2.8 A
	+2VDOIM	1.5 ÷ +3.5 V	1.5 ÷ +3.5 V	0 ÷ 1.7 A (**)
	DTERM	0 ÷ +3.5 V	0 ÷ +3.5 V	0 ÷ 0.15 A (**)
To the Layers 0…4	DVDD	0 ÷ +8.0 V	0 ÷ +8.0 V	0 ÷ 0.6 A (layer 0)
				0 ÷ 0.9 A (layer 1)
				0 ÷ 1.5 A (layer 2)
				0 ÷ 1.5 A (layer 3)
				0 ÷ 2.0 A (layer 4)
	AVDD	0 ÷ +10.0 V	0 ÷ +10.0 V	0 ÷ 0.6 A (layer 0)
				0 ÷ 0.9 A (layer 1)
				0 ÷ 1.5 A (layer 2)
				0 ÷ 1.5 A (layer 3)
				0 ÷ 2.1 A (layer 4)
	VBIAS	0 ÷ +250 V	0 ÷ +250 V	0 ÷ 5 mA (layer 0…4)

(*) for all the low voltages the voltage values shown in the Table are as measured at the remote sensing point.

(**) note that the values set via software are absolute values, while the sign of the actual currents is as indicated by the IMON parameters; for details refer to the User's Manual of the SY527 system.

Table 4.2 – Setting mode for the channel parameters

	Output	VMAX	VSET	ISET
To the Port Card	+5VDOIM	Trimmer	Trimmer	Programmable
	+2VDOIM	Trimmer	Trimmer	Programmable
	DTERM	Trimmer	Trimmer	Programmable
To the Layers 0…4	DVDD	Trimmer	Trimmer	Programmable (independently for each layer)
	AVDD	Trimmer	Trimmer	Programmable (independently for each layer)
	VBIAS	Trimmer	Programmable (independently for each layer)	Programmable (independently for each layer)

4.5. Control and Monitoring of the channel status

Please refer to the *User's Manual* of the SY527 system for the control and monitoring of the status of the output channels.

4.6. Voltage Sensing

All the low voltage channels, nominally the AVDD and the DVDD voltages to the Layers 0…4 and the DTERM, +5VDOIM and +2VDOIM voltages to the Port Card, have a remote sensing line to compensate for the voltage drop over the cable.

The remote sensing lines have a dynamic 50 Ω series termination at the sensing point. The remote signal is received differentially by an amplifier with input impedance $Rin \geq 1\ M\Omega$. If the remote sensing line fails, the power supply has an internal connection which prevents the voltage from running away.

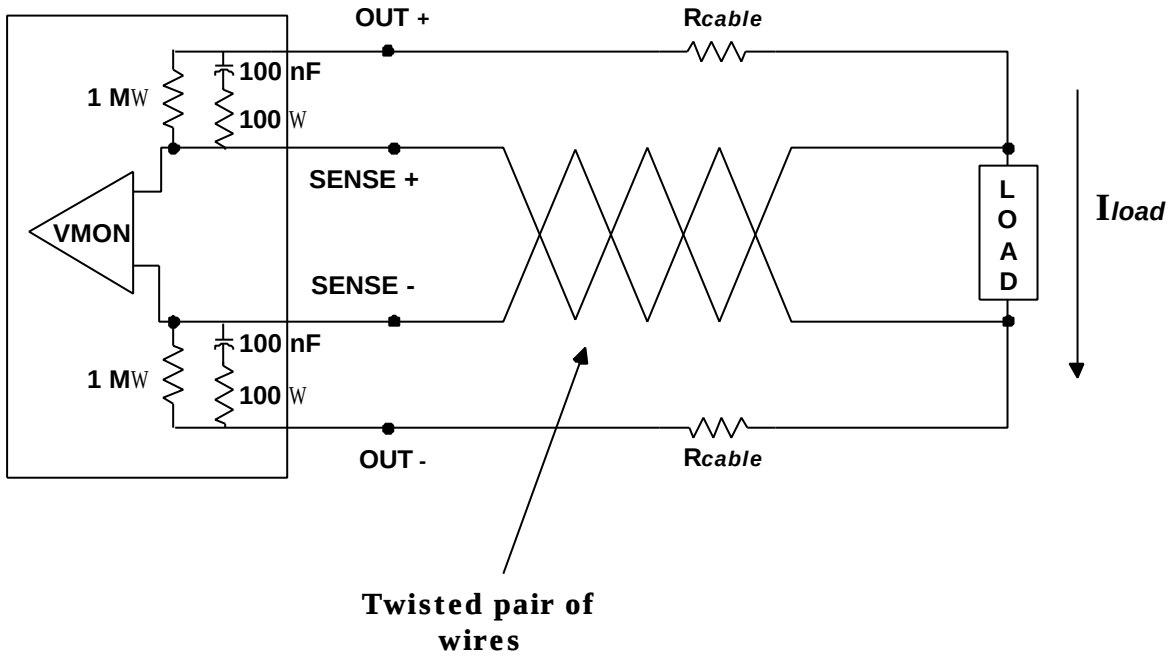


Fig. 4.2 – Voltage Sensing lines

4.7. Trip

The TRIP of a power supply channel can be caused by Over-Current, Over-Voltage or Under-Voltage conditions.
The TRIP condition causes the channel to be switched off.

The Over-Current trip protection is of the constant current type, i.e. before being switched off the channel behaves like a current generator. The Over-Voltage trip protection is done by clamping to the maximum voltage VMAX and then turning off the channel. The Under-Voltage trip protection is done by turning off the channel.
Over-current trip values for all the power supply channels are remotely programmable between 0-100% of the maximum current ISET shown in Table 1.1, p.7. An Over-Current trip will occur as the channel reaches the programmed ISET value.
Over-Voltage trip values for the channels can be adjusted between 0 and the relevant VMAX value by using the proper trimmers.
Under-Voltage trip values are fixed at between 500 and 700 mV below the VSET value indicated for each channel in Table 1.1, p.7.

For any TRIP the power-off sequencing is as described in § 4.3, p.29 to the extent possible. In fact, the channel experiencing a trip condition is turned off immediately and then the Power-Off sequence is followed as usual for the remaining associated channels.

CAUTION

FOLLOWING ANY TRIP, THE AFFECTED SUPPLIES ARE DISABLED FROM BEING POWERED ON FOR 10 SECONDS!

The TRIP condition is signalled via six TRIP output signals on the TRIP connector (refer to § 2.4.4, p.12 for specifications), corresponding to each of the five layers and to the Port Card. These signal are active low TTL signals: it means that if the power supply channel is On (not tripped), it will assert the TTL high signal, while a tripped power supply channel will assert the TTL low signal.
If any power supply channel (DVDD, AVDD or VBIAS) of one layer is tripped, all the power supply channels relative to that layer are shut-down sequentially. If any of the 5VDOIM and +2VDOIM power supply channels of the Port card is tripped, the complete module is shut-down according to the Power-Off sequence. In the latter case the port card channels can not be switched on until the module Power-Off sequence is complete.

If a TRIP condition is detected, the exact condition which caused the TRIP is recorded in the status register until the module is reset.

Finally, any power supply channel that is powered on, will trip if the ENABLE signal is dropped. Refer to § 4.2, p.28 for details.

N.B.: The above, and particularly the Power-Off sequencing, is true independently from the value set via software for the TRIP parameter.