Trigger Application for the Heavy Photon Search Test Run

6 February 2012

Introduction

The Heavy Photon Search collaboration is planning a Hall B test run in spring 2012. This document is a specification for using the Jefferson Lab FADC250 VXS module for the readout and triggering required for the Heavy Photon Search test run in spring of 2012. The latest production revision of the FADC250 has many powerful features for triggering and readout, and in the following sections we describe modifications to the existing firmware to support the triggering requirements of the HPS calorimeter.

Application

The Electro-Magnetic Calorimeter detectors that will be used to form the Level 1 trigger are an array of PbWO4 crystal blocks. Each crystal block is instrumented with an Avalanche Photo Diode (APD) and preamplifier that drive a pulse signal to the coaxial input of the Jefferson Lab FADC250 module. The array of crystal blocks will be arranged in two sections, with each section comprised of 230 output channels. Each FADC250 is sixteen channels, so at least 16 FADC modules will be used for each section of the EM Calorimeter, or two full VXS crates for the entire EM calorimeter.

The APD preamplifier output signal will produce a nominal pulse width of <N ns and the individual channel output rates have been simulated for given beam energies and beam current that is planned for the spring test run. The APD preamplifier pulse amplitudes will require that the input to the FADC250 modules be set for the -2V input range.

Brief review of FADC250 Trigger and Readout Features

The complete details of the latest FADC250 firmware features will not be listed in this document, but the firmware modifications required for the HPS spring run will focus on how the FADC250 processes the trigger information from each ADC channel.

Brief outline of present production firmware

After power-up, software programming configuration, and synchronization, the FADC250 is continuously sending a 16-bit sum value to the Crate Trigger Processor through the high speed

gigabit serial interface. This sum value is the total sum of all sixteen front end ADC chips for every 4ns sampling period. The high speed gigabit interface is capable of transferring 4Gb/s or 2 bytes/4ns. Figure 1 shows a block diagram of the 16-bit sum process.

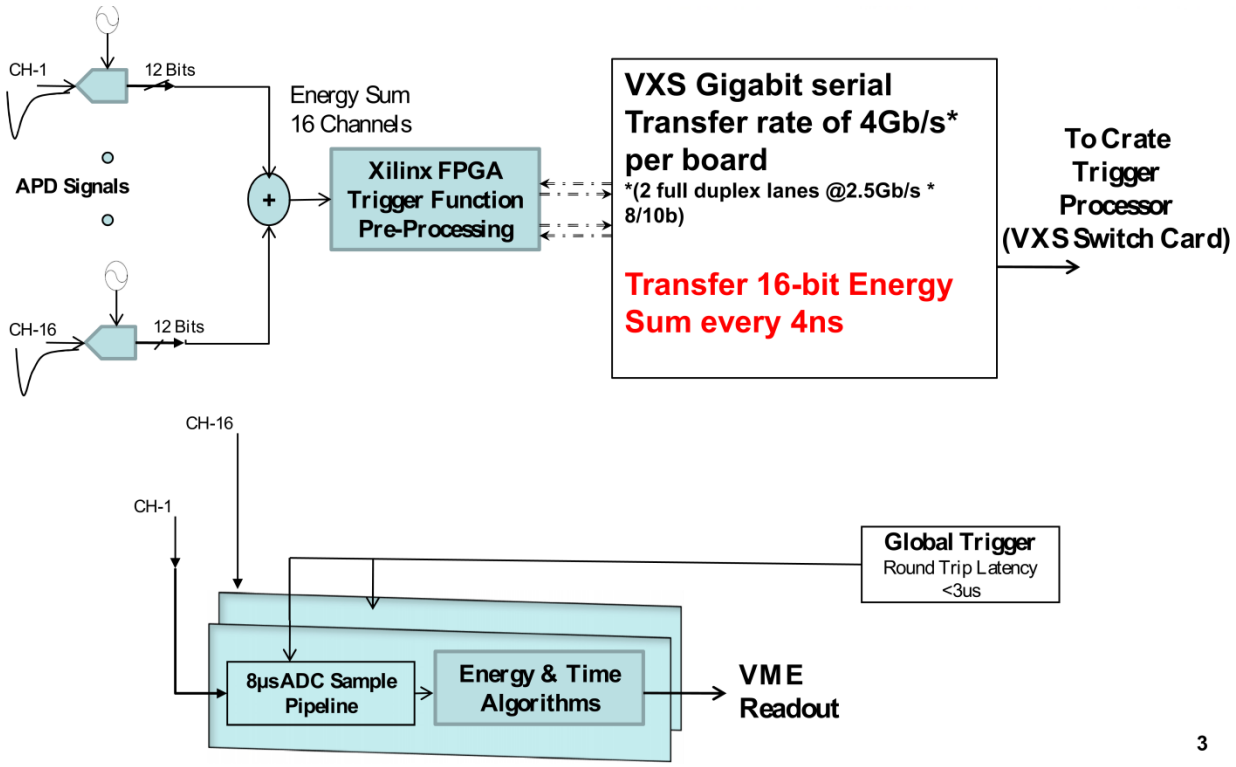


Figure 1: 16-bit "Board Sum" value reported every 4ns to CTP

Figure 1 also shows that each channel of the FADC250 is processed according to User programmed selections when an experiment trigger is received. These readout features are not covered in this document, and will be retained in the existing firmware.

Trigger Requirements – HPS Test Run

- ***Firmware***

Figure 2 shows a block diagram of the proposed trigger processing required for the HPS test run. Note that the same gigabit bandwidth will be used to transport all the individual FADC250 channel sums and clock encoding bits to resolve a 4ns period within a 32ns frame. The clock encoding bits report the time when the input signal crosses the programmable threshold within the 32ns frame. If the input signal does not cross threshold for a given 32ns frame, then the channel data is reported as zero.

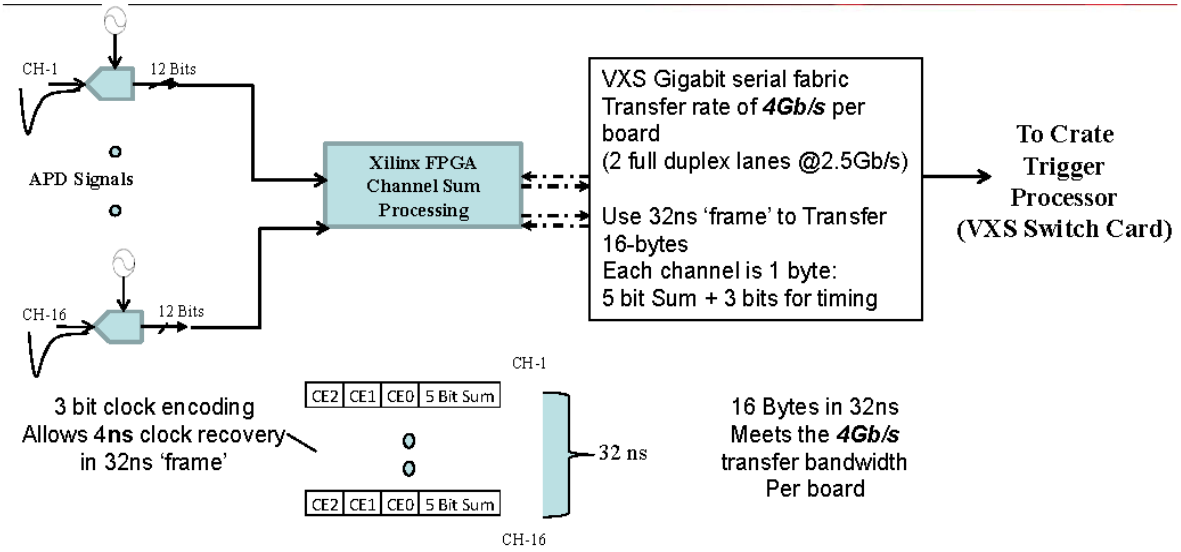


Figure 2 Individual channel sum and 4ns resolution for signal threshold crossing

The reported 5-bit channel sum value is extracted from the 17-bit register that contains the integrated (sum) of the input channel. The channel integration occurs only if the input signal crosses the programmable threshold level. The samples that are included in the channel integration are those that are above threshold. The number of samples for a given channel integration will not be larger than the frame report latency time (MAX=128ns or 32 samples).

Figure 4 shows several examples of input signal pulses in relation to the synchronous 32ns frame and frame report times.

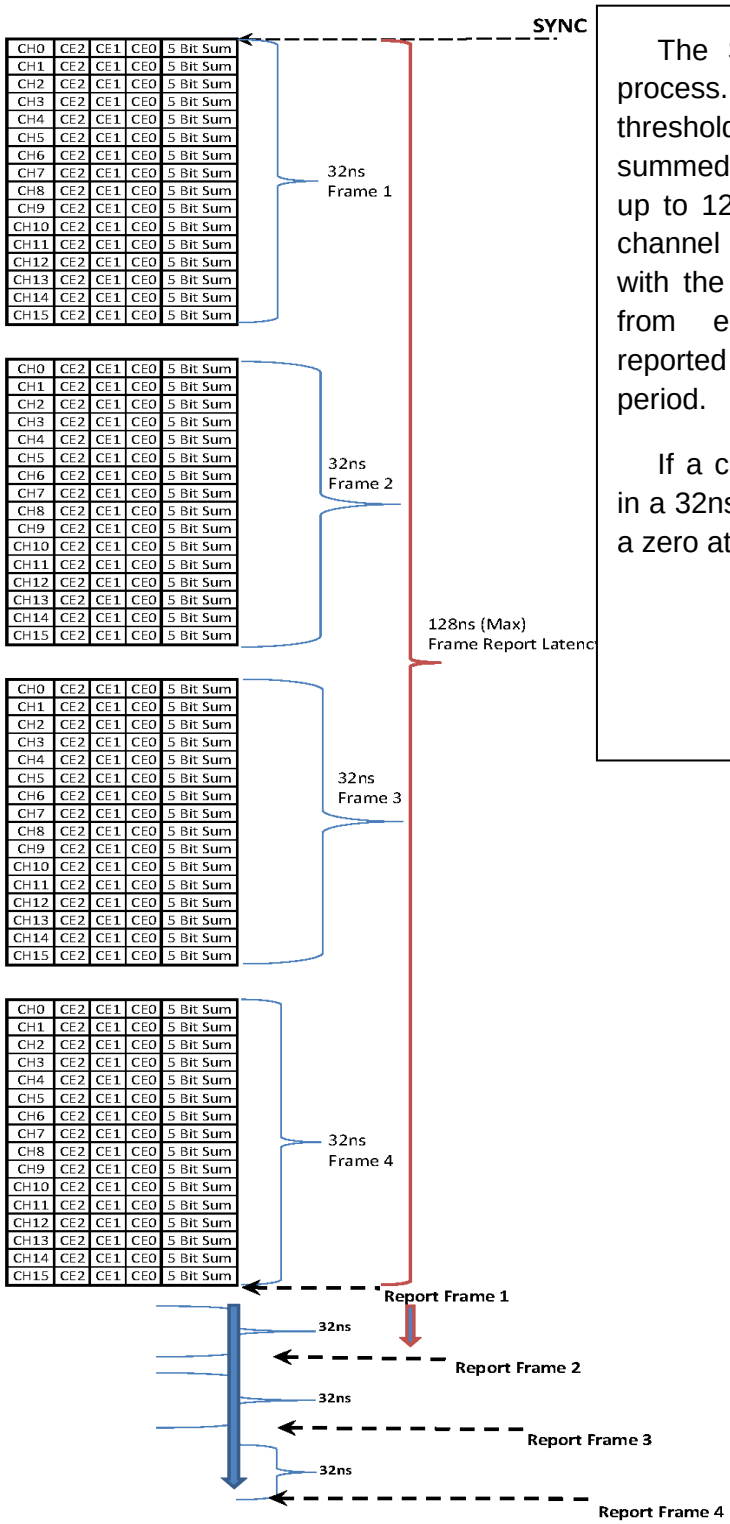
- ***Programmable values***

- Trigger processing threshold: 12 bits (ADC counts); Common threshold for all 16 FADC250 channels per board.

- Channel sum value: At least 17-bits are required to store the sum (integration) value for each channel for all sample points above threshold. This programmable register allows Users to select 5-bits of the 17-bit channel sum value. The 5-bits value will be extracted and concatenated with the clock encoding bits, and transferred to the high speed gigabit interface for frame processing.

- Frame report Latency: Programmable with three choices; 64ns, 96ns or 128ns

- ***Processing examples***



The SYNC signal starts the trigger process. Each channel that crosses threshold within a 32ns 'frame' is summed for all samples over threshold up to 128ns MAX. The time where the channel crosses threshold is recorded with the clock encoding bits, and 5 bits from each channel 'integration' is reported at the end of the frame report period.

If a channel does not cross threshold in a 32ns frame, then the channel reports a zero at the frame report cycle.

Figure 3: Trigger processing example.

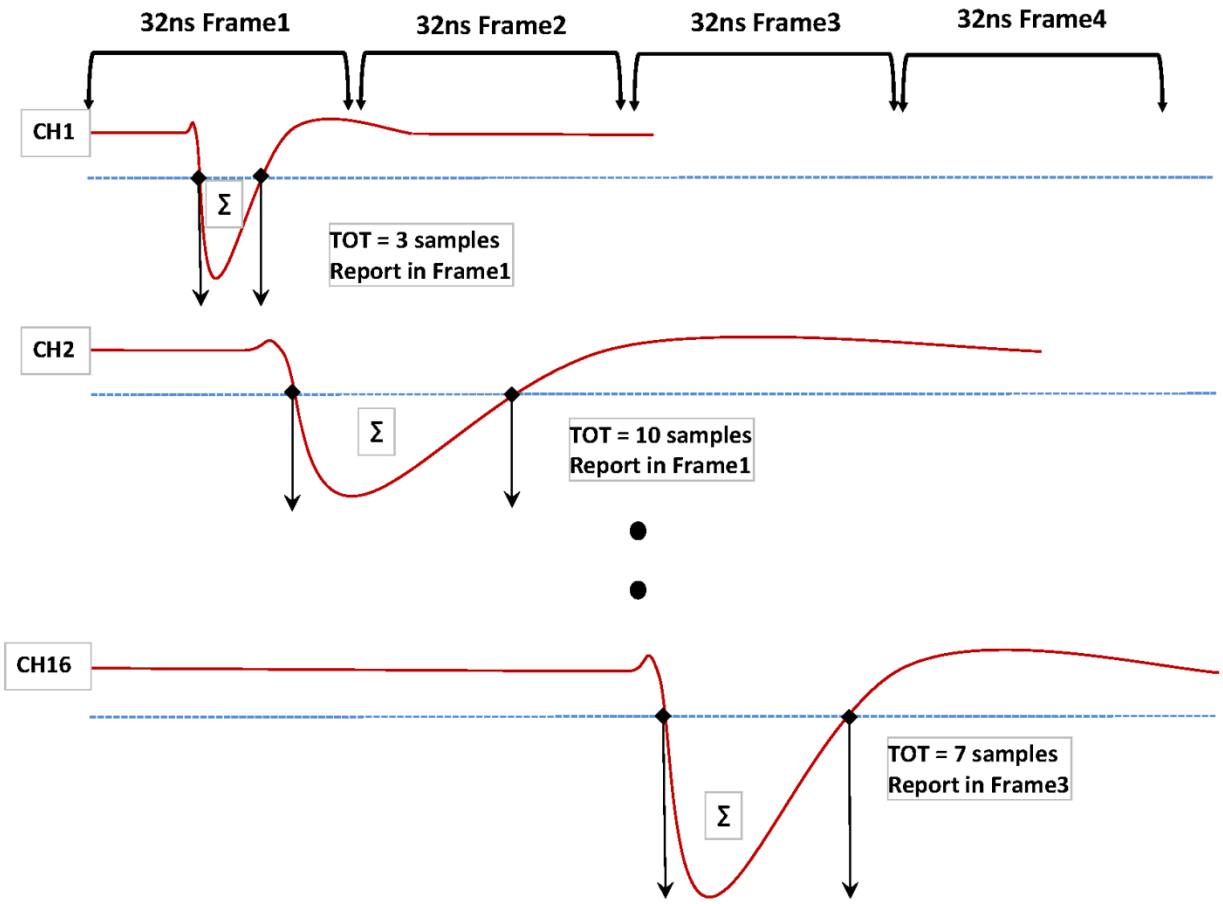


Figure 4: Input signal examples

Figure 4 shows input channel examples with pulses that are above threshold within a single frame and pulses that cross frames. The point where the input signal crosses threshold determines which frame the integrated value is reported. The time where the input signal crosses threshold is captured within the frame and reported with the three clock encoding bits to a 4ns time stamp of the threshold crossing time.

Note in the example that the pulse signal width for channel 2 crosses multiple frames. The point where the signal crosses threshold determines the frame where the integration value will be reported for the given channel. The number of points that are over threshold will be limited to 32.

Multiple pulses within a 32 ns frame will occur and is defined as pulse pile-up. The trigger application will only process a single falling edge or single rising edge per 32ns frame. Multiple pulse signals may be recoverable from the readout data offline.

Implementation and Test Plans

Firmware development will begin immediately and will require significant modifications to the existing firmware revision. Verification that the new trigger processing will not exceed the FPGA resources will need to be confirmed as soon as possible, and other existing firmware features may need to be removed to guarantee that the new trigger processing firmware will fit within the resources of the FPGA and still meet critical timing criteria.

A single FADC250 module can be used for a test, and the initial firmware will need to be operated in conjunction with a Crate Trigger Processor (CTP), Trigger Interface (TI) module and Signal Distribution(SD) module to verify operation within a VXS readout crate.

Firmware for the CTP and Sub-System Processor (SSP) can be started as soon as the firmware for the FADC250 has been functionally simulated.

Crate Trigger Processor – Firmware requirements

The CTP will receive Gigabit serial data streams from each of the sixteen FADC250 modules. The serial data stream from each FADC250 payload module is comprised of two full duplex differential connections running at 2.5Gb/s. The data stream format is given in the processing section, figure 3.

The CTP must be synchronized to the crate system clock and commands to configure the CTP registers will use the I^2C communication link to the Trigger Interface board.

The sixteen serial data streams will be processed on a frame by frame basis, and the cluster finding algorithm will produce a serial data stream that will be processed by the Sub-System Processor (SSP) to create a readout trigger signal that can be distributed to the front end FADC250 for a Physics event readout.

- Input data stream definition
- Overall Channel input map
- Cluster finding explanation and method
- CTP Output Data Format (4 Fiber Optic Transceiver lanes)

Existing CTP firmware aligns data based on Sync across all transceiver lanes in order to produce crate energy sums. This firmware will be modified to preserve that alignment so all incoming channel information can be processed for cluster finding. The new data format including three bits for timing and five bits for energy sum per FADC channel is shown in figure 2 on page 3.

The new calorimeter mapping is shown below in Figure 5. The top and bottom halves each consist of five rows and 46 columns with nine channels removed for a total of 221 channels per CTP. The numbering convention is derived from the HPS Test Run Proposal. The mapping is symmetric about the X axis allowing the same firmware to be used in both CTPs.

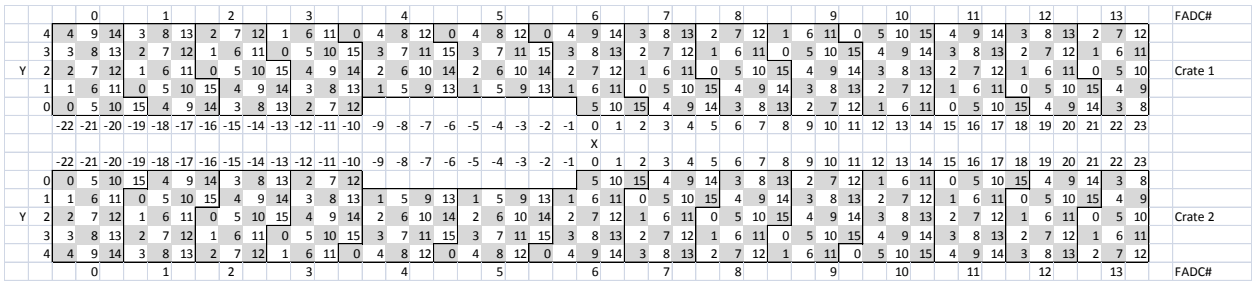


Figure 5: FADC to Calorimeter map

Cluster Finding Algorithm

The algorithm used for cluster finding in the HPS experiment makes use the parallel processing nature of FPGAs by simultaneously searching for 125 clusters up to 3x3 in size across the calorimeter crystal array. A Cluster Processor (CP) is centered on each of the crystals if another cluster does not cover all of its same channels. In Figure 6 below, each 1 indicates that a cluster processor is centered at that location. For example, at (-22, 4), all four of its channels are included in the cluster calculation centered on (-21, 3). This creates a "sliding window" of overlapping clusters.

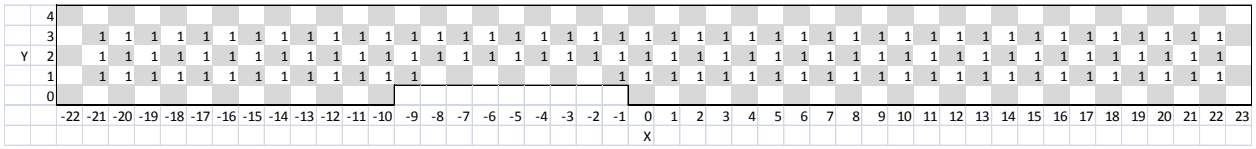


Figure 6: Cluster Processor Locations

Depending on its position on the array, each cluster processor receives up to nine energy sums and their associate time stamps every 32 ns. During the eight 4ns clock cycles between frames, the cluster processor examines all time stamps and compares them to a counter running zero to seven. The energy values of all channels associated with the current time are loaded into a processor register bank for computation of the total cluster energy. The energy values persist in the processing registers for two clock cycles giving a cluster time window of 8 ns.

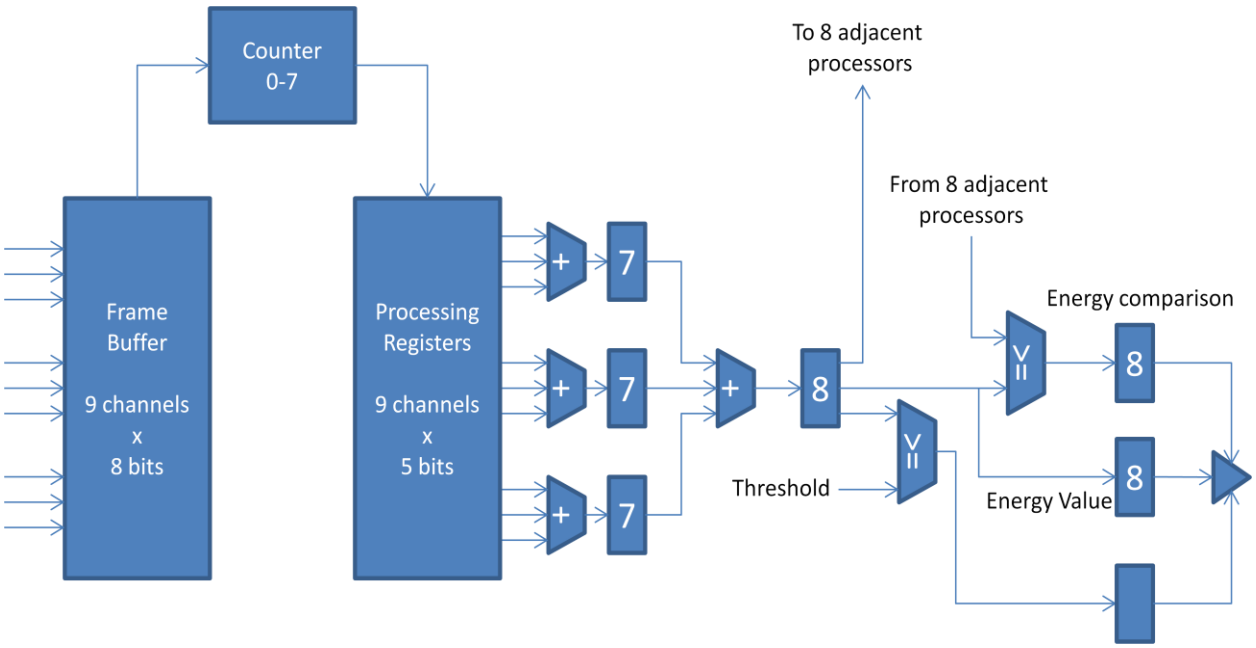


Figure 7: Cluster Processor

This energy sum is computed continuously and compared with the programmable cluster threshold. The energy is sent to adjacent cluster processors to determine whether or not it has the greatest energy sum. If it has the highest energy of its neighbors and exceeds the threshold, it is the cluster center and the energy and time are reported. This allows the rejection of many of the clusters that may be reported from a single event.

Data Consolidation

The task of funneling cluster data occurs over a series of FIFOs that ultimately serialize the data for transmission to the SSP via the four-channel Fiber transceiver. See figure 8.

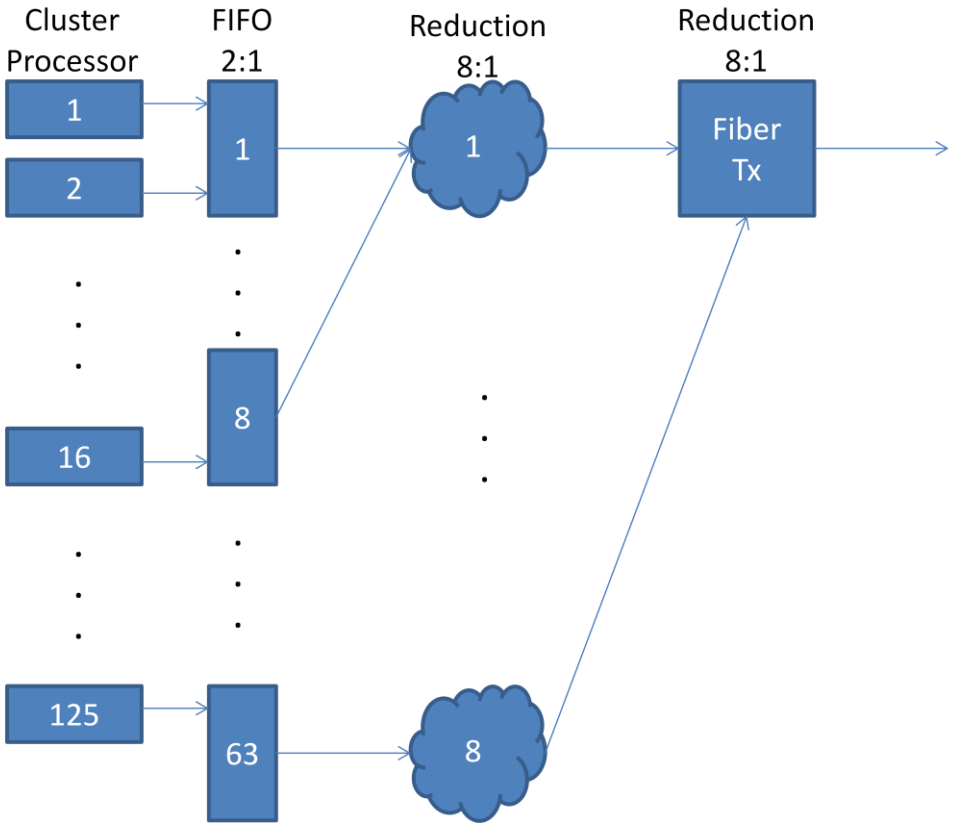


Figure 8: Consolidation of data from Cluster Processors to Fiber

To help balance the memory usage required, two cluster processors feed a single FIFO, halving the number of memory blocks needed to handle all 125 cluster processors. This tradeoff means that location information is appended afterward by using the fixed FIFO mapping to determine the cluster position. As a result, the current implementation will not allow the calculation of a cluster's centroid position, only the center of the 3x3 window containing the highest energy sum of its neighbors. Priority is given to clusters with older time stamps using a round-robin read of the FIFOs in order to reduce latency. The CTP to SSP data format is shown in Figure 9 below.

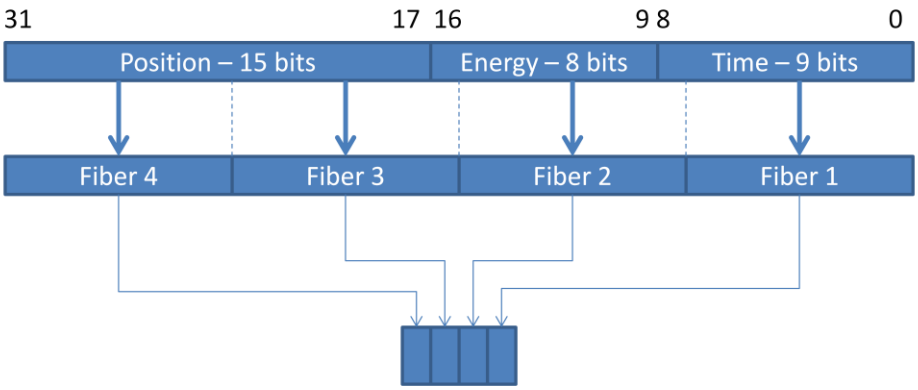


Figure 7: CTP to SSP Fiber channel mapping