ePixM: a CMOS monolithic sensor for LCLS II

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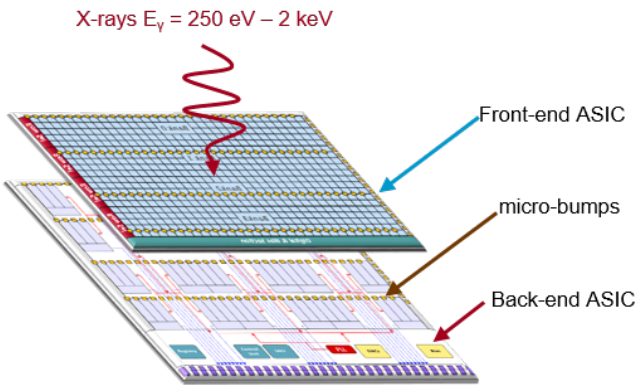

Fig. 1. ePixM core module concept.

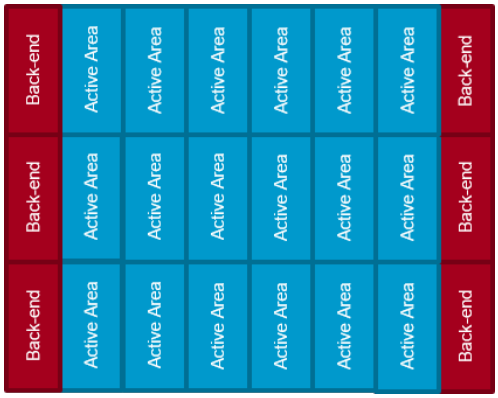

Fig. 2. ePixM camera: front view.

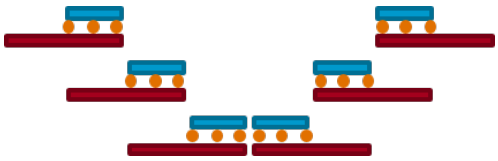

Fig. 3. ePixM camera: side view.

I. Introduction

THE SLAC Linac Coherent Light Source (LCLS) upgrade, known as LCLS-II, will provide extremely bright X-ray laser light at higher rate, moving from the actual 120 pulses per second (120 Hz) to 1 million pulses per second (1 MHz). The facility will operate in a soft X-ray range (250 eV - 2 keV), performing experiments in a wide range of fields that are now impossible.

ePixM project aims at developing a high-rate 1Mpix camera for soft X-ray experiments at SLAC. Fig. 1 shows the concept behind the core module, composed of a back-illuminated fully depleted monolithic active pixel sensor (DMAPS) connected to a back-end ASIC for readout by bump-bonding and flip-chip technique. Following an incremental and risk mitigating approach, the present prototype has been designed to work at a frame rate of 7.5 kHz.

Fig. 2 and Fig. 3 show the shingled assembly approach required to maximize the fill factor. Core modules will be tiled in a 6 x 3 array to build the full 1152 x 1152 pixels camera.

Combining the sensing element and the front-end electronics on the same substrate, offers several benefits like lower noise and interconnection capacitance, improved resolution, costs and material reduction [1]. The front-end has been designed in 0.15 µm CMOS technology on high-resistivity substrate (>2000 Ω cm) to allow full depletion of the sensor, resulting in a lower detector capacitance of the order of 70 fF and a charge collection time of few nanoseconds [2]. Wafers will be thinned down to 50 µm to facilitate full depletion and backside illumination. Sensors will be post-processed to add a shallow entrance window, a crucial step to achieve high quantum efficiency for low energy X-rays [3].

Back-end ASIC includes 768 Sigma-Delta (ΣΔ) ADCs necessary for the readout functionality [4]. The ASIC has been designed in standard 0.25 µm CMOS technology, as a part of the ePix family, a common platform optimized to build modular scalable detectors for LCLS, resulting in a simpler and more robust integrated system [5].

II. Image sensor

Fig. 4 shows a simplified block diagram of the front-end ASIC. It consists of a fully depleted back-illuminated DMAPS arranged in a matrix of 192 x 384 global shutter pixels. Each pixel has a size of 50 µm × 50 µm for a total sensitive area of approximately 20 mm x 10 mm. The ASIC is optimized for low noise applications with energy resolution of 15 e^- rms, single photon detection at 250 eV and dynamic range of 1000 photons at 500 eV.

Matrix is divided in four subgroups of 48 x 384 pixels to allow row-by-row parallel readout by use of four row selectors and thus achieve higher frame rate.

Bottom edge of the chip contains the analog bias reference section and the digital section including the clock trees for uniform distribution of the control signals required for both

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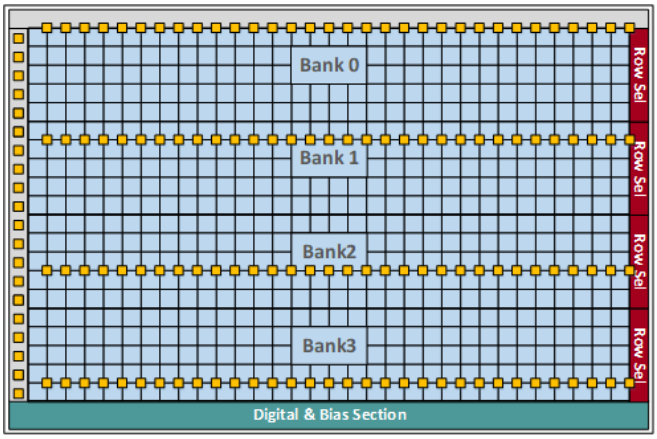

Fig. 4. ePixM front-end block diagram.

integration and acquisition phases. An array of microbumps on the left side is used to provide supplies, digital signals and bias references coming from the back-end ASIC. Edge pads and row selectors form extra row and column lines that minimize the matrix performance degradation due to boundaries effects. All the edges are filled with decoupling capacitors to reduce supply and bias ripple.

Fig. 5 shows a simplified architecture of the global shutter pixel. Sensor is directly coupled to the charge sensitive amplifier (CSA) implemented with auto-ranging gain capability to afford the high signal range. Integration phase starts in high gain mode: when the output of the CSA reaches a certain threshold due to a high input charge, a comparator triggers, switching the gain to low. Switching point can be controlled by a programmable threshold voltage.

CSA is followed by a buffer and a correlated double sampling stage (CDS). It reduces any common temporal and fixed pattern noise source on the reset and signal level, including KTC noise and low frequency noise sources, supply ripple or interferences. KTC noise contribute is also reduced by the use of big capacitors of the order of $1\,\mathrm{pF}$ [2].

Charge information is stored into a capacitor until readout phase is ended as well as the gain information. Integration time is in the order of $3\,\mu\mathrm{s}$ due to the fast settling time of the reset operation. All the operations are synchronous in every pixel.

Pixels contains also a test injection circuitry driven by a pulser present in the back-end [6].

Fig. 6 shows a post layout simulation of the pixel response for different integrated energies. A linear fit is also plotted as a dashed line. The curve results linear for energies up to $600\,\mathrm{keV}$. Pedestal of the low gain region can be tuned too. Noise is well below the Poisson limit over the whole range 250 – $2\,\mathrm{keV}$: simulated equivalent noise charge (ENC) is $11.3\,\mathrm{e}^-$ in high gain and $90.8\,\mathrm{e}^-$ in low gain.

Fig. 7 shows the pixel cross-section. Substrate is depleted by applying a negative high voltage from the backside. Based on the measured depletion depth, wafer will be thinned and then processed at SLAC to form a thin-entrance window to achieve high quantum efficiency for low energy X-rays [3]. Electronics is inside a deep N-well (DNW) implant that acts as collecting

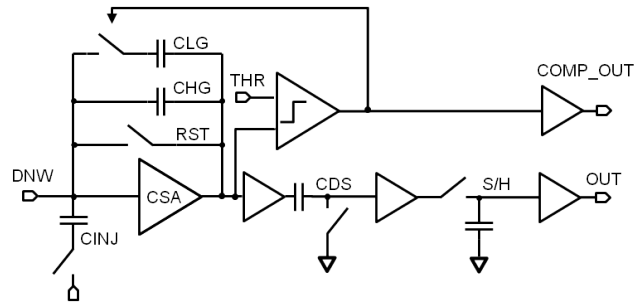

Fig. 5. Pixel architecture.

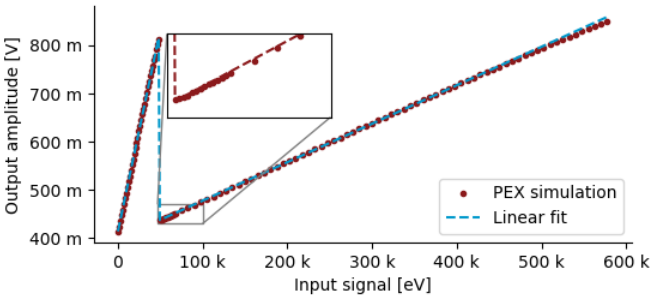

Fig. 6. Post layout simulation: gain curve.

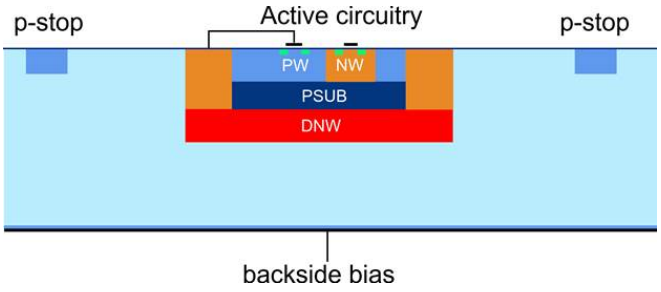

Fig. 7. Pixel cross-section.

node for the charges generated by incoming radiation in the sensitive volume. An additional deep P-well (DPW) is required to isolate the DNW from the transistors N-wells, allowing the use of both pmos and nmos.

Detector capacitance value is crucial for noise performances. It is determined by the sum of two contributions: the reverse biased junction capacitance between DNW and substrate and the one between DNW and DPW. Based on the circuitry complexity the occupied area can increase, resulting in a bigger detector capacitance and higher noise. If the area is too small the electronics architecture could be too simple to accomplish the desired functionality and respect the specifications. In ePixM the circuitry occupies an area of $10\,\mu\mathrm{m}$ x $10\,\mu\mathrm{m}$ only, thus the trade-off between the area of electronics and the ENC results optimized [2].

Several precautions have been adopted to guarantee the proper electrical field and potential distribution based on TCAD simulations and test on previous prototypes. P-stop structures with metal overhangs isolate each pixel from the neighbours. Chip periphery is surrounded by guard rings to minimize the sensor leakage current. All the substrate

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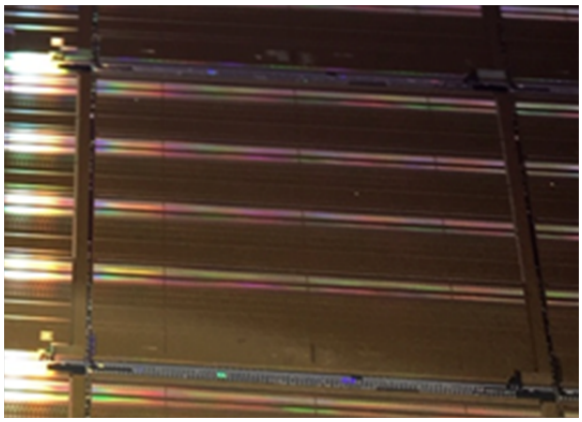

Fig. 8. ePixM back-end die.

junctions have been drawn with rounded edges to reduce the electrical field at the corners and increase the breakdown voltage.

III. Readout

Back-end shown in Fig. 8 is used for the analog-to-digital conversion and stream out of the pixels information and to provide all the necessary signals, supply and bias to the matrix. The core element of the readout chip is the ΣΔ ADC, based on a novel 2-stage MASH architecture. The ADC has a pitch of 100 µm and it has already been used in other variants of the ePix family with a measured ENOB of 13 bits [4].

Fig. 9 shows a simplified block diagram of the interface between the image sensor and the readout ASICs. Parallel readout is necessary to achieve the 7.5 kHz frame rate requirement. On front-end side, subgroups of 48 x 2 pixels share the same output lines and microbump pads fitting the area of one single ADC. In this way it is possible to reach the expected frame rate as well as to reduce the number of microbump pads, resulting in a simpler assembly. Only two microbumps for subgroup are required: one for the pixel analog output and one for the gain-range bit information. All the microbumps have a size of 18 µm x 18 µm, reducing the area occupied in the sensing area.

On back-end side, the basic readout bank is composed of 32 multiplexed ΣΔs, followed by a 16b/20b encoder and a double data rate (DDR) serializer. Fig. 10 shows a simplified block diagram of the ePixM back-end ASIC. An array of 4 x 6 readout banks is used for the full matrix readout. Clock tree distribution schemes minimize the signal skew at bank level. Data are sent out by the use of 24 parallel LVDS transmitters.

Back-end has a size of approximately 20 mm x 15 mm, resulting longer than the front-end ASIC to include the periphery circuitry necessary for the overall ePixM module functionality. The ASIC is equipped with a serial interface with handshaking protocol to configure the entire camera, control unit that decodes and execute the commands, registers, internal DACs, analog and digital monitoring systems. Input clock is provided to the ASIC through a LVDS receiver and fed to the internal PLL. An analog section is also present including the BGR and bias references.

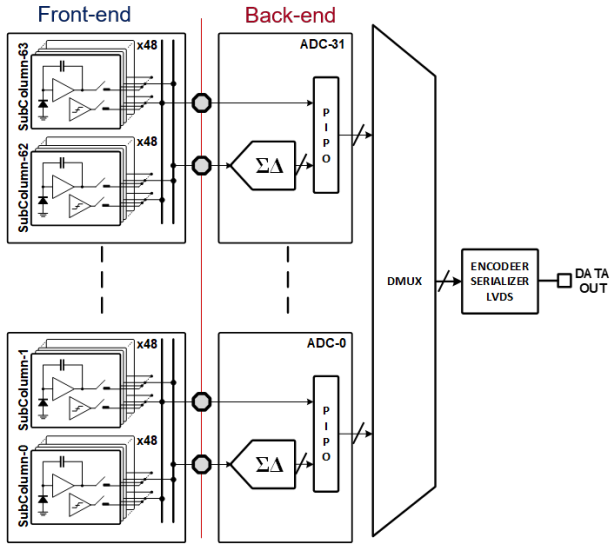

Fig. 9. ePixM interface.

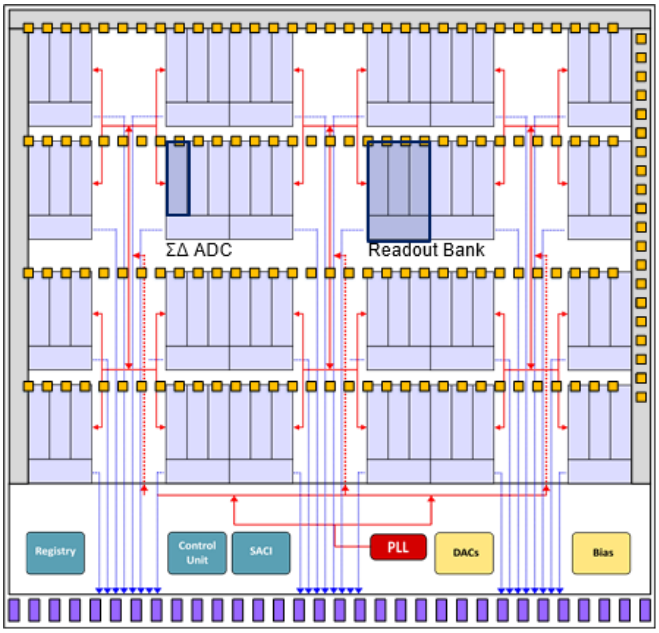

Fig. 10. ePixM back-end block diagram.

IV. Conclusion

ePixM is a high-rate back-illuminated fully depleted image sensor for soft X-rays experiments.

Core module is composed of two separated ASICs. Front-end is currently under fabrication. Several variants and test structures with wire bonding pads have been included to independently characterize the matrix performances. Post layout simulations have been shown, meeting all the requirements in terms of noise and dynamic range. Initial tests have been started for the back-end ASIC.

A completely scalable approach is being developed to move toward the full camera, in terms of power, control and data acquisition.

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