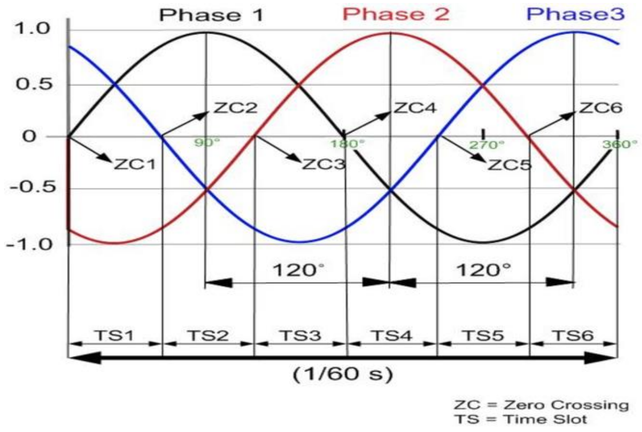
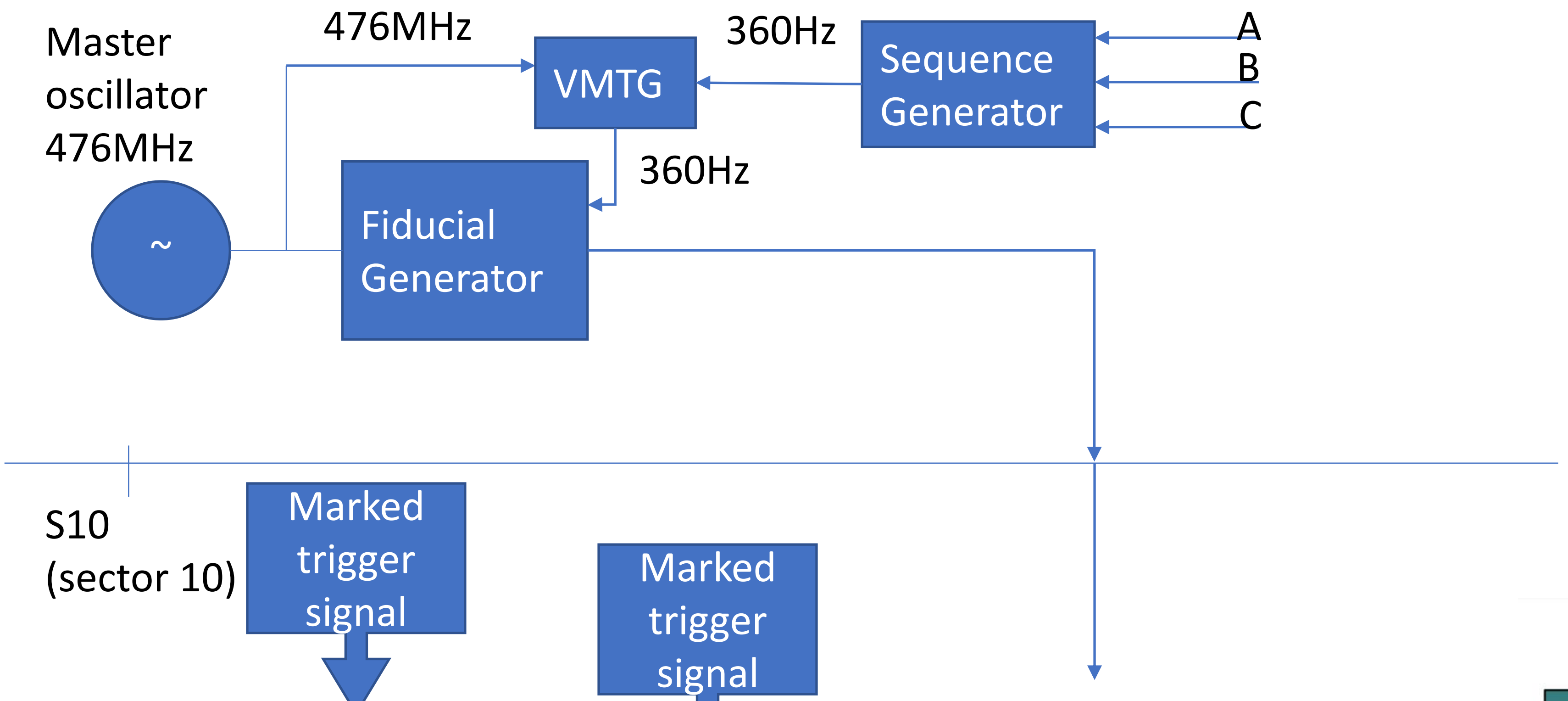
Timing for LCLS

VMTG is to sync the RF with PG&E signal to define timeslots

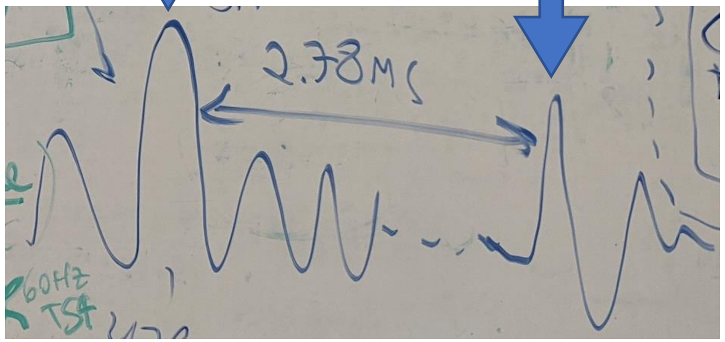
A, B, C are the three 60Hz from PG&E with different phase to generate 6 time slots



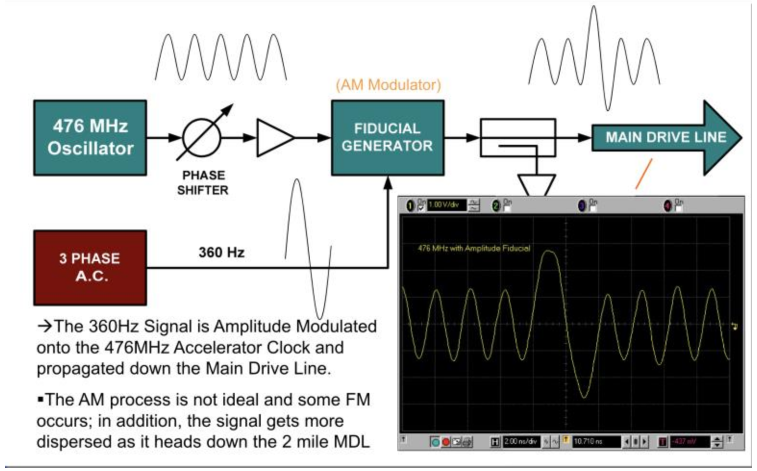
LCLS use timeslots 1&4



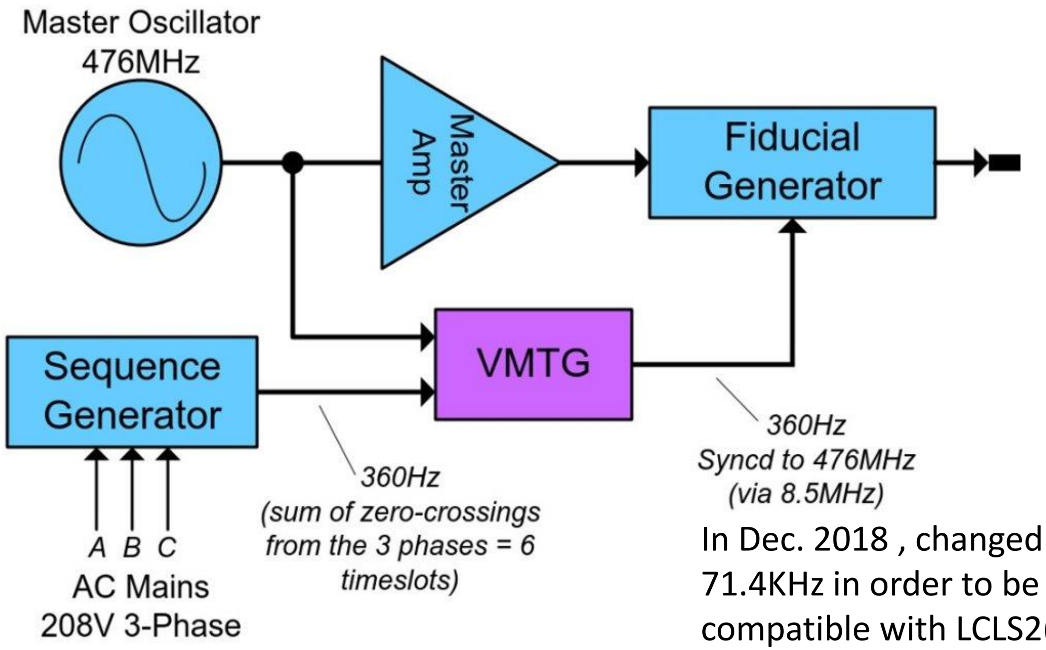
In sector 10 is where is timing trigger signal is generated and be used at all other sectors and buildings.



The 360Hz signal is Amplitude Modulated onto the 476MHz Accelerator Clock and propagated down the Main Drive Line(2.78ms is the timing between two triggers)



A Sequencer chassis derives a 360 Hz signal coincident with the zero crossing of the 3 phase AC power. This is combined with 476 MHz from a precision COTS Master Oscillator. These signals are combined in a VME-based Master Trigger Generator which fires the Fiducial Generator which combines with the 476 MHz for distribution on the Main Drive Line.

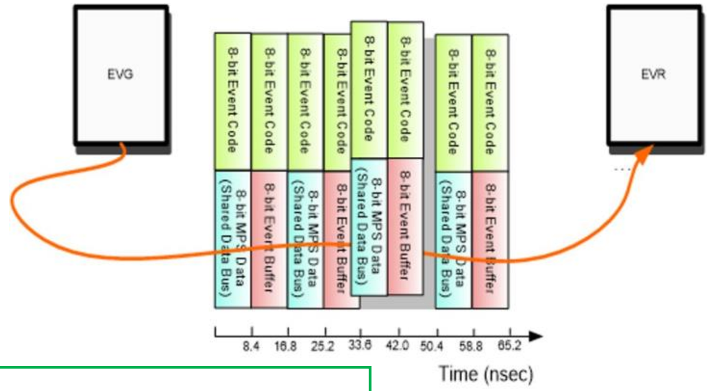


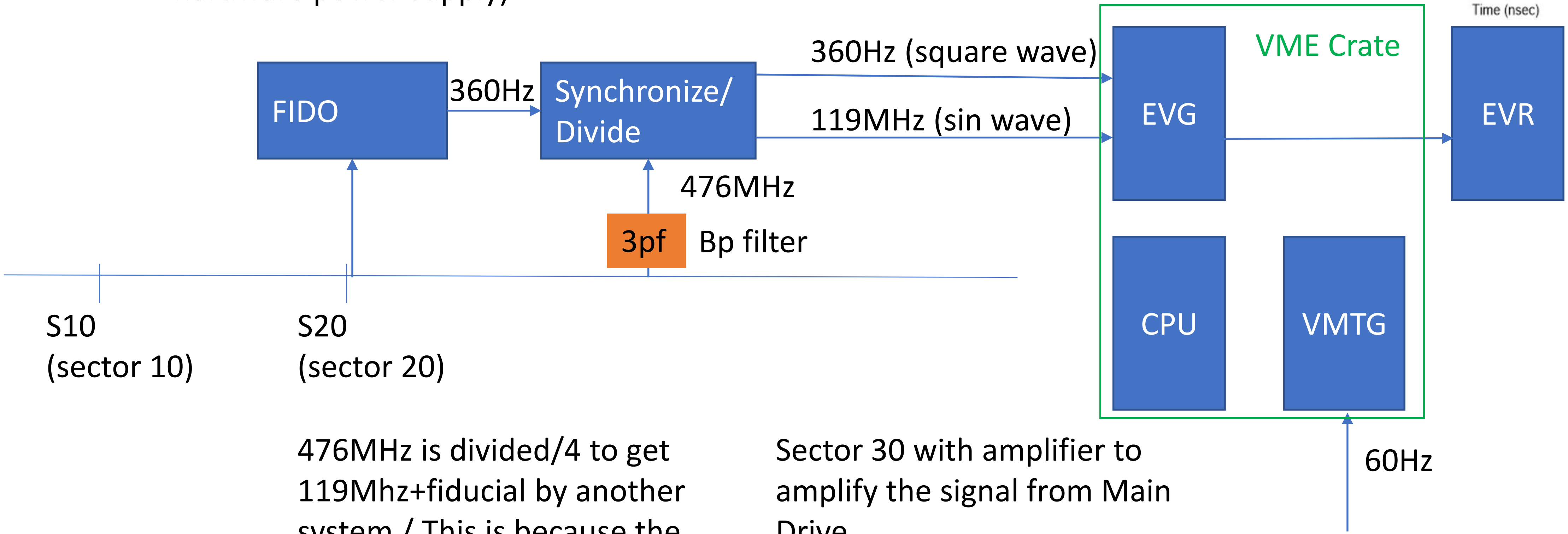
In Dec. 2018 , changed to 71.4KHz in order to be compatible with LCLS2(Master oscillator 1300MHz)

LI00 Master RF Phase Ref & Timing Fid Source

Moved from LI00 to IN10 (2017)

LCLS runs at a maximum rate of 120 Hz (Each timeslot represent 60 Hz signal, ex. LCLS timeslot 1 and 4 which is 120 Hz which is the maximum rate of RF hardware power supply)

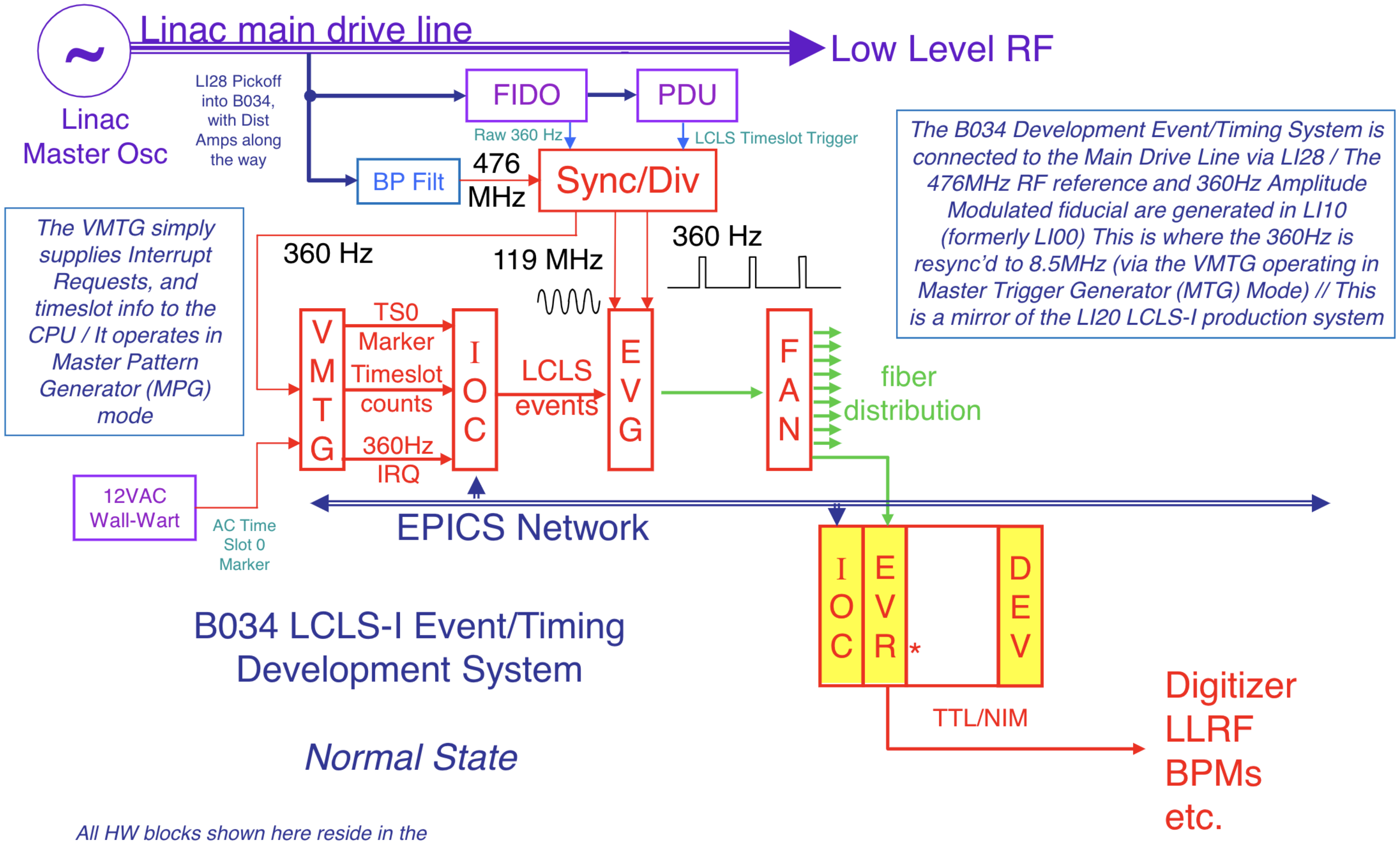




476MHz is divided/4 to get 119Mhz+fiducial by another system / This is because the older technology HW could not run at 476MHz

Sector 30 with amplifier to amplify the signal from Main Drive

60Hz Fiducial act as the mark on the trigger form to indicate 0 crossing of ts1



B034 LCLS-I Event/Timing Development System

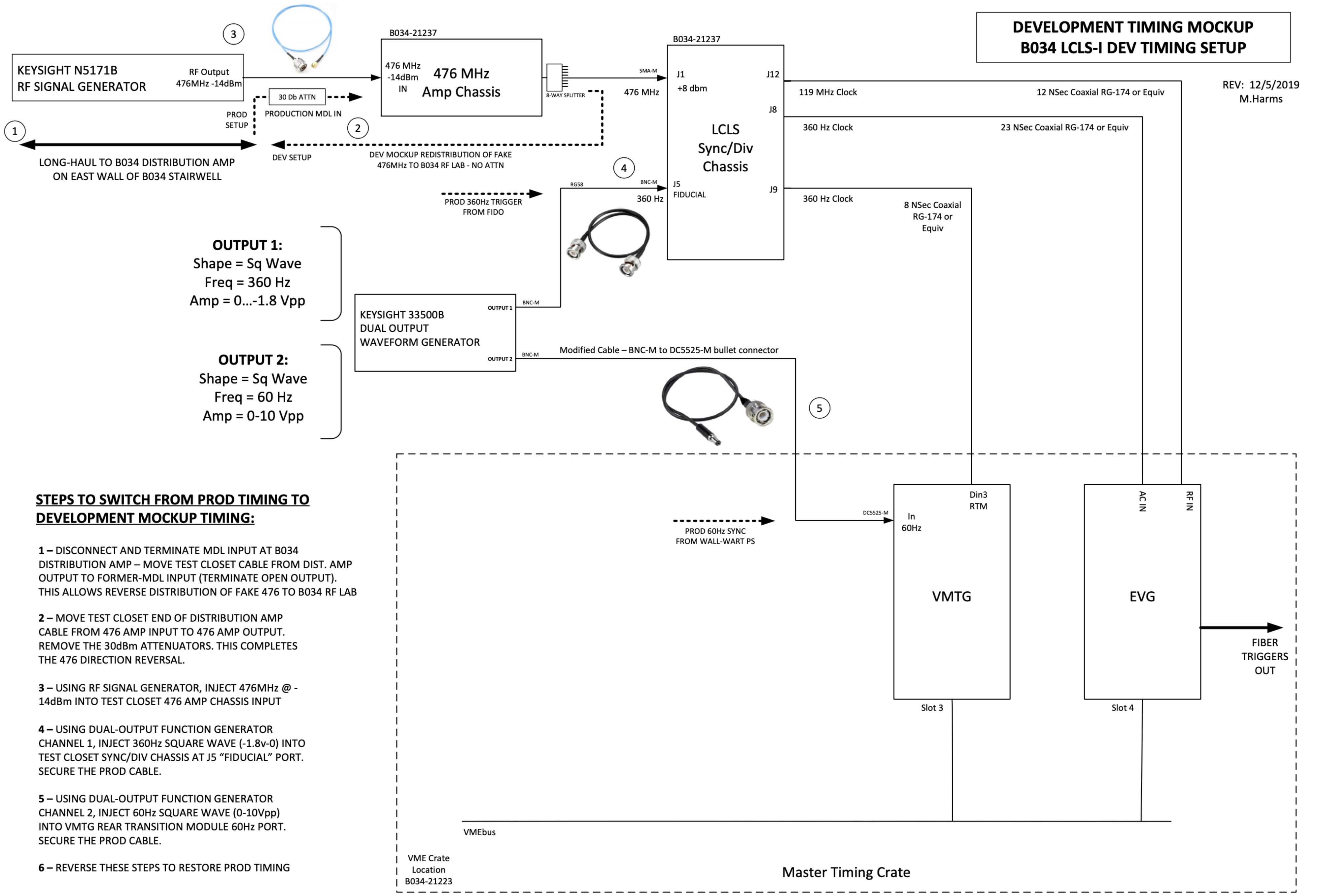
Normal State

All HW blocks shown here reside in the B034 test room (apart from Linac Master Osc & MDL)

Updated 06-5-2018

DEVELOPMENT TIMING MOCKUP
B034 LCLS-I DEV TIMING SETUP

REV: 12/5/2019
M.Harms



STEPS TO SWITCH FROM PROD TIMING TO DEVELOPMENT MOCKUP TIMING:

1 – DISCONNECT AND TERMINATE MDL INPUT AT B034 DISTRIBUTION AMP – MOVE TEST CLOSET CABLE FROM DIST. AMP OUTPUT TO FORMER-MDL INPUT (TERMINATE OPEN OUTPUT). THIS ALLOWS REVERSE DISTRIBUTION OF FAKE 476 TO B034 RF LAB

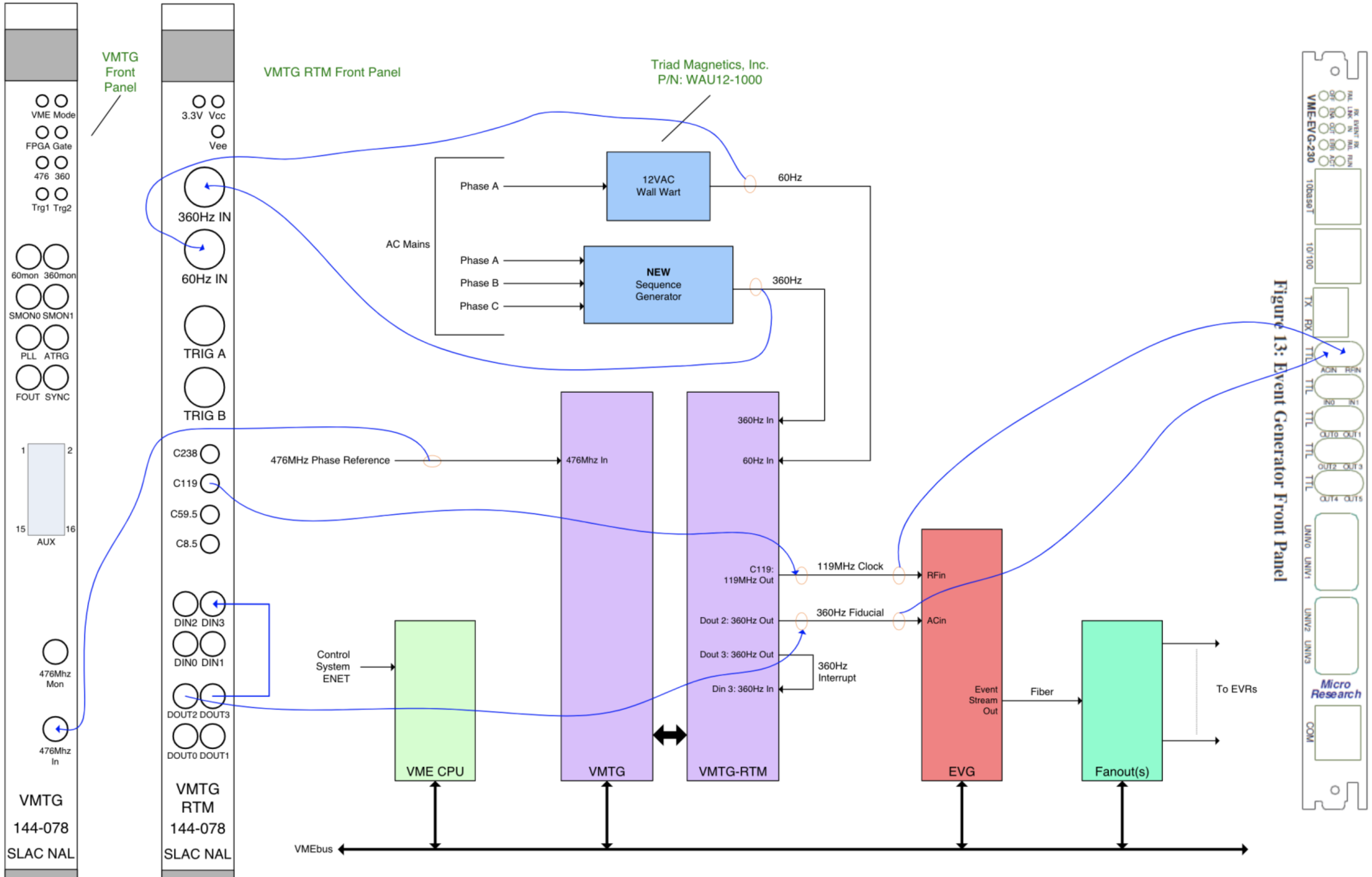
2 – MOVE TEST CLOSET END OF DISTRIBUTION AMP CABLE FROM 476 AMP INPUT TO 476 AMP OUTPUT. REMOVE THE 30dBm ATTENUATORS. THIS COMPLETES THE 476 DIRECTION REVERSAL.

3 – USING RF SIGNAL GENERATOR, INJECT 476MHz @ -14dBm INTO TEST CLOSET 476 AMP CHASSIS INPUT

4 – USING DUAL-OUTPUT FUNCTION GENERATOR CHANNEL 1, INJECT 360Hz SQUARE WAVE (-1.8v-0) INTO TEST CLOSET SYNC/DIV CHASSIS AT J5 "FIDUCIAL" PORT. SECURE THE PROD CABLE.

5 – USING DUAL-OUTPUT FUNCTION GENERATOR CHANNEL 2, INJECT 60Hz SQUARE WAVE (0-10Vpp) INTO VMTG REAR TRANSITION MODULE 60Hz PORT. SECURE THE PROD CABLE.

6 – REVERSE THESE STEPS TO RESTORE PROD TIMING



New B034 Dev Timing/Event System
Signal Interconnect Detail

SLAC National Accelerator Laboratory Accelerator Controls	
Date:	March 16, 2017
Created By:	J. Dusatko
Page:	5 of 5

NC Timing

- Cu BSA provides scalar data that is time stamped by the Timing (Event) System.
- Cu BSA provides data filtering according to user needs.
- Cu BSA provides pulse-by-pulse data buffers up to the beam rate.
  - Maximum of 2800 data points.
  - Each data point can be an average of up to 1000 beam pulses
  - Maximum rate of 120 Hz.
  - ~1700 Cu BSA signals.

EVG ioc name

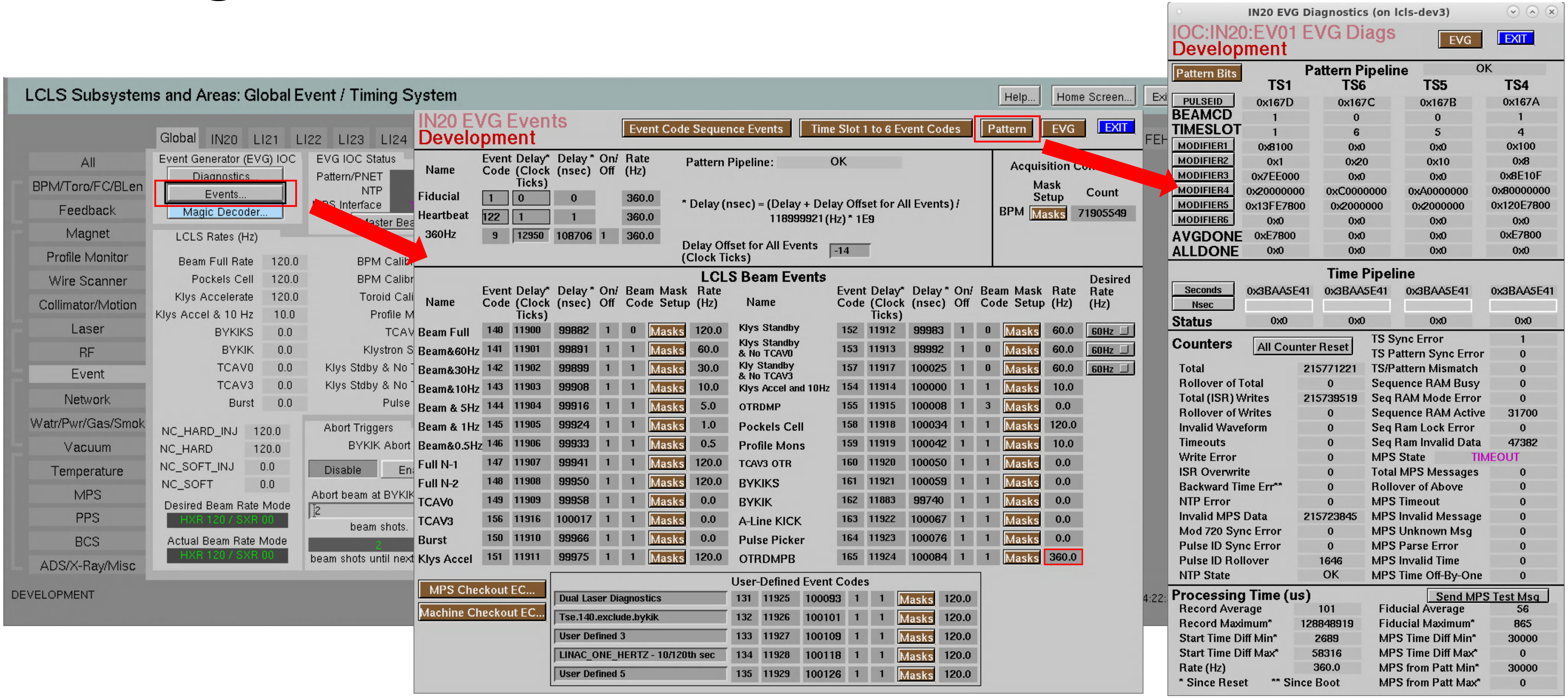
- EVG-Event Generator
  - EVG is an IOC
  - Ioc-in20-ev01 for LCLS -(PV SYS0)
  - Ioc-sys1-ev01 for FACET
  - Ioc-xt01-ev01 for XTA -(PV SYS6)
  - Ioc-b34-ev01 for Development -(PV SYS0)
  - Ioc-as01-ev01 for ASTA (Test Facility) -(PV SYS7)
  - Runs epics/ioc/MpgApp (CVS module is Mpg)

NC Timing Frame

- The **timing frame** contains the information regarding the current operating mode:
  - Time
  - PulseID
  - Beam Code (BC) (0=Any, 1=Cu to HXR, 2= Cu to SXR –see next slide)
  - Modifier bits: time slot; kicker trigger mask presence; beam presence; subset of lower rate trigger mask per destination; etc..
  - Event Codes
  - BSA fields
- N timing frame : 1 Timing Pattern
- The **timing pattern** is used by the receiver to:
  - Trigger devices
  - Trigger Data acquisition using Beam Synchronous Acquisition (BSA)

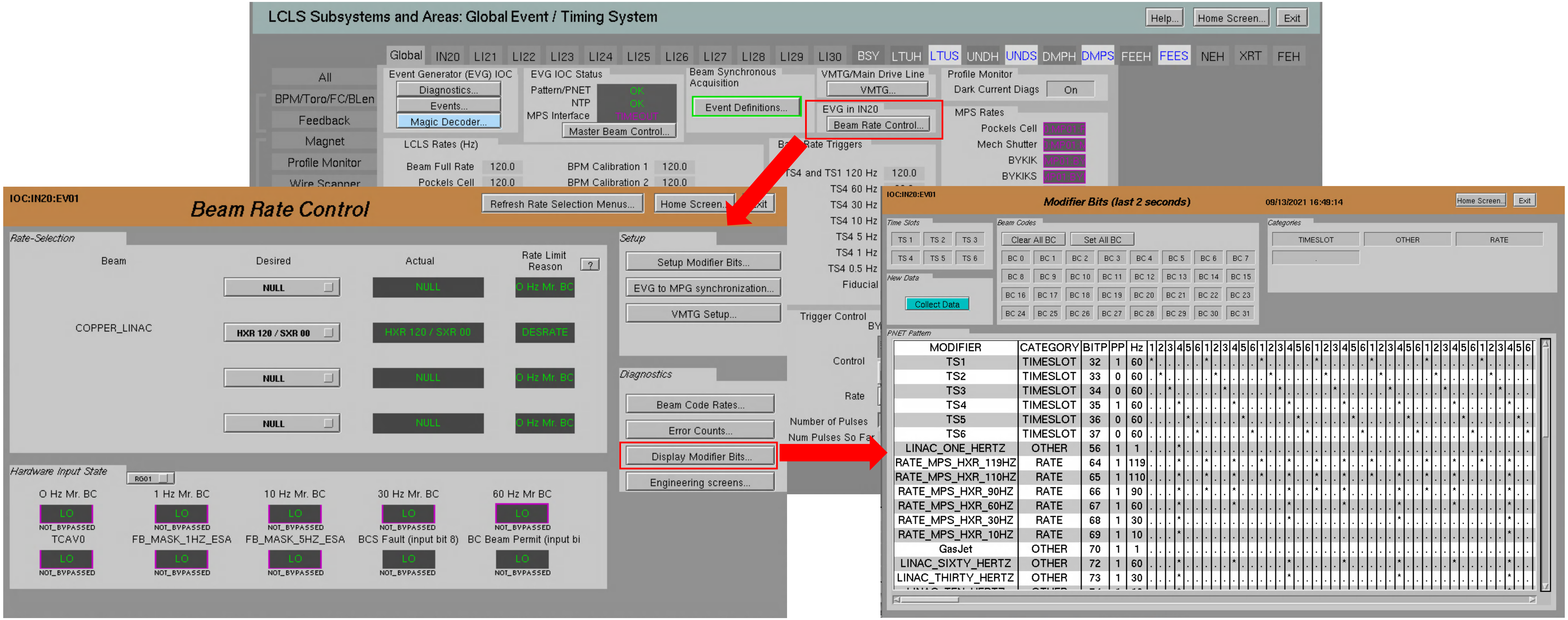
- An IOC is equipped with an EVR.
- Timing Fiber is run from EVG, most likely through a Fanout module.
- Special software is installed in the IOC that knows how to talk to the EVR.
- Assuming the requested signals can be read out within 1/120th sec from the hardware, EPICS Databases are created for the Cu BSA PV.

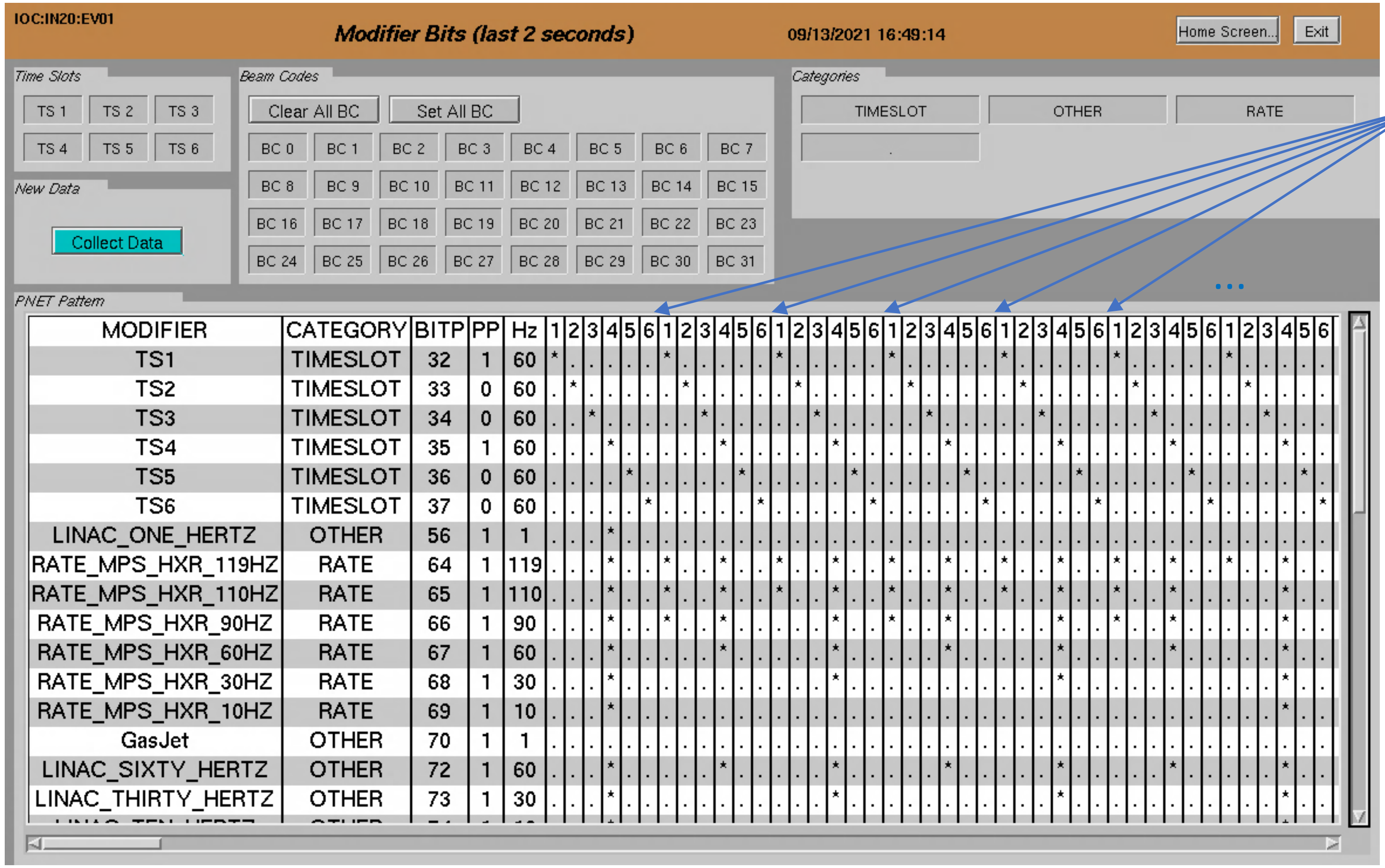
Timing Pattern




IN20 EVG Diagnostics (on lcls-dev3)
IOC:IN20:EV01 EVG Diags
Development
EVG
EXIT
Pattern Bits
Pattern Pipeline
OK
TS1 TS6 TS5 TS4
PULSEID 0x167D 0x167C 0x167B 0x167A
BEAMCD 1 1 0 1
TIMESLOT 1 6 5 4
MODIFIER1 0x8100 0x0 0x100
MODIFIER2 0x1 0x20 0x10
MODIFIER3 0x7EE000 0x0 0x0
MODIFIER4 0x20000000 0xC0000000 0xA0000000 0x80000000
MODIFIER5 0x13FE7800 0x2000000 0x2000000 0x120E7800
MODIFIER6 0x0 0x0 0x0 0x0
AVGDONE 0xE7800 0x0 0x0 0xE7800
ALLDONE 0x0 0x0 0x0 0x0
Time Pipeline
Seconds 0x3BAA5E41 0x3BAA5E41 0x3BAA5E41 0x3BAA5E41
Nsec
Status 0x0 0x0 0x0 0x0
Counters
All Counter Reset
Total 215771221
Rollover of Total 0
Total (ISR) Writes 215739519
Rollover of Writes 0
Invalid Waveform 0
Timeouts 0
Write Error 0
ISR Overwrite 0
Backward Time Err** 0
NTP Error 0
Invalid MPS Data 215723845
Mod 720 Sync Error 0
Pulse ID Sync Error 0
Pulse ID Rollover 1646
NTP State OK
TS Sync Error 1
TS Pattern Sync Error 0
TS/Pattern Mismatch 0
Sequence RAM Busy 0
Seq RAM Mode Error 0
Sequence RAM Active 31700
Seq Ram Lock Error 0
Seq Ram Invalid Data 47382
MPS State TIMEOUT
Total MPS Messages 0
Rollover of Above 0
MPS Timeout 0
MPS Invalid Message 0
MPS Unknown Msg 0
MPS Parse Error 0
MPS Invalid Time 0
MPS Time Off-By-One 0
Processing Time (us)
Send MPS Test Msg
Record Average 101
Record Maximum* 128848919
Start Time Diff Min* 2689
Start Time Diff Max* 58316
Rate (Hz) 360.0
* Since Reset
** Since Boot
Fiducial Average 56
Fiducial Maximum* 865
MPS Time Diff Min* 30000
MPS Time Diff Max* 0
MPS from Patt Min* 30000
MPS from Patt Max* 0
Timing Pattern Bi
Timing Pattern Bits (PNBN)
EXIT
Units 1 to 20
Units 61 to 80
Units 21 to 40
Units 41 to 60
Units 101 to 120
Units 121 to 140
Timing Pattern Bi
Timing Pattern Units 1 to 20
EXIT
Bit Posn | # of Bits | Name
0 8 YY
8 5 PP
14 1 MPG_IPLING
15 1 MOD720RESYNC
16 4 PULSIDRESYNC
21 1
22 1
23 1
24 1
25 1
26 1
27 1
28 1
29 1
30 1
20 12 PSK_CONTROL
32 6 TSLOT_U6
32 1 TS1
33 1 TS2
34 1 TS3

Modifier bit





MODIFIER	CATEGORY	BITP	PP	Hz	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6	1	2	3	4	5	6
TS1	TIMESLOT	32	1	60	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.
TS2	TIMESLOT	33	0	60	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.
TS3	TIMESLOT	34	0	60	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.
TS4	TIMESLOT	35	1	60	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.
TS5	TIMESLOT	36	0	60	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.
TS6	TIMESLOT	37	0	60	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*
LINAC_ONE_HERTZ	OTHER	56	1	1	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
RATE_MPS_HXR_119HZ	RATE	64	1	119	.	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.
RATE_MPS_HXR_110HZ	RATE	65	1	110	.	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	*	.	.	.	.	.	*	.	.
RATE_MPS_HXR_90HZ	RATE	66	1	90	.	.	.	*	.	.	*	.	.	*	.	.	.	.	.	*	.	.	*	.	.	*	.	.	.	.	.	*	.	.	*	.	.	*	.	.	.	.	.	*	.	.
RATE_MPS_HXR_60HZ	RATE	67	1	60	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.
RATE_MPS_HXR_30HZ	RATE	68	1	30	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.
RATE_MPS_HXR_10HZ	RATE	69	1	10	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	*	.	.
GasJet	OTHER	70	1	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
LINAC_SIXTY_HERTZ	OTHER	72	1	60	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.	.	.	.	*	.	.
LINAC_THIRTY_HERTZ	OTHER	73	1	30	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.	.	.	.	.	.	.	.	.	.	*	.	.

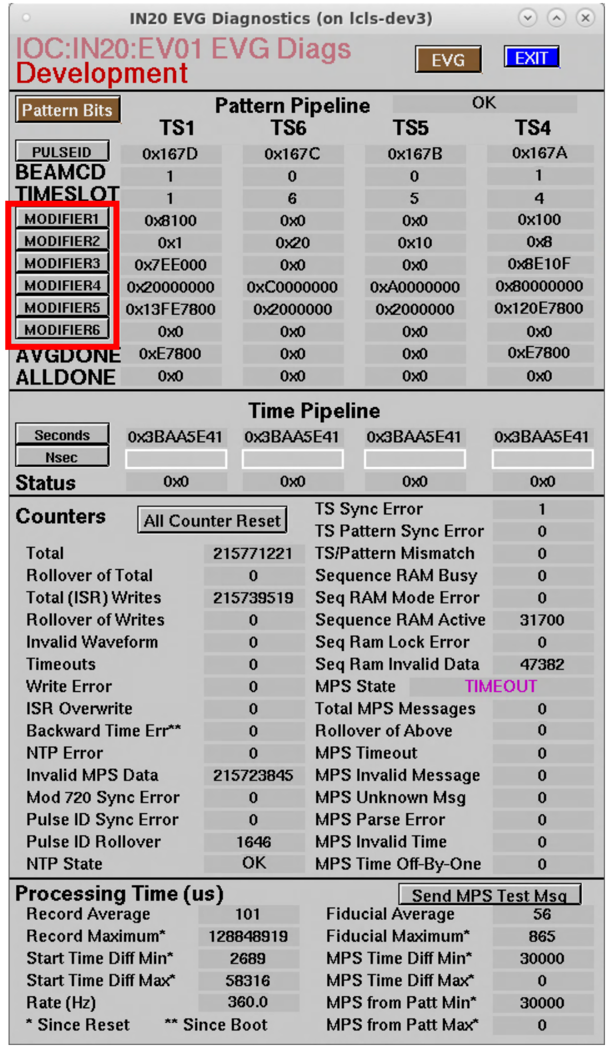
Each timeslot can hold
timing frame shown in p.11

The pattern repeat every 360 cycles (360Hz) --> 60(each time slot is 60Hz)*6(6 time slots)=360Hz
For LCLS the maximun rate is 120Hz since it uses S1 & S4 (60+60=120Hz)
LCLS can have timing send out timing pattern frame in 120Hz

Each pattern contain 60 times 6 time slots, ex, TS1 send out 60 times of data in one pattern.

The slowest rate it can send is 1bit per 360 cycles
-->1Hz

Modifier section



Modifier section is separated into 6 sections as MOD1, MOD2, …, MOD6

MOD1 is the lowest 32 (0-31 bit) bit of the timing pattern which is for EVG internal usage.

MOD6 is the highest 32 (160-191 bit) bit of the timing pattern which is for MPS data (excluded by the pipeline)

MOD2-5 are for EVG event code

```
/* Bits in modifier 3                                                    */
#define MOD3_IDX                  2
#define POCKCEL_PERM              (0x00080000)  /* Pockels cell permit    */
#define TCAV0_PERM                (0x80000000)  /* TCAV0                  */
//CLTS Project MPS Modifier Bits to set rates to two destinations:
/* Masks defined for CLTS timing MPS communication */
#define RATE_MPS_HXR_119HZ      (0x00000001)  /* RATE_MPS_HXR_119HZ  BITP 64   */
#define RATE_MPS_HXR_110HZ      (0x00000002)  /* RATE_MPS_HXR_110HZ  BITP 65   */
#define RATE_MPS_HXR_90HZ       (0x00000004)  /* RATE_MPS_HXR_90HZ   BITP 66   */
#define RATE_MPS_HXR_60HZ       (0x00000008)  /* RATE_MPS_HXR_60HZ   BITP 67   */
#define RATE_MPS_HXR_30HZ       (0x00000010)  /* RATE_MPS_HXR_30HZ   BITP 68   */
#define RATE_MPS_HXR_10HZ       (0x00000020)  /* RATE_MPS_HXR_10HZ   BITP 69   */
#define RATE_MPS_HXR_05HZ       (0x00000800)  /* RATE_MPS_HXR_05HZ   BITP 75   */
#define RATE_MPS_HXR_01HZ       (0x00001000)  /* RATE_MPS_HXR_01HZ   BITP 76   */
#define RATE_MPS_SXR_119HZ      (0x00002000)  /* RATE_ MPS_SXR_119HZ BITP 77   */
#define RATE_MPS_SXR_110HZ      (0x00004000)  /* RATE_ MPS_SXR_110HZ BITP 78   */
#define RATE_MPS_SXR_90HZ       (0x00008000)  /* RATE_ MPS_SXR_90HZ  BITP 79   */
#define RATE_MPS_SXR_60HZ       (0x00020000)  /* RATE_ MPS_SXR_60HZ  BITP 81   */
#define RATE_MPS_SXR_30HZ       (0x00040000)  /* RATE_ MPS_SXR_30HZ  BITP 82   */
#define RATE_MPS_SXR_10HZ       (0x00100000)  /* RATE_ MPS_SXR_10HZ  BITP 84   */
#define RATE_MPS_SXR_05HZ       (0x00200000)  /* RATE_ MPS_SXR_05HZ  BITP 85   */
#define RATE_MPS_SXR_01HZ       (0x00400000)  /* RATE_ MPS_SXR_01HZ  BITP 86   */
#define BKRCUS                  (0x00800000)  /* BKRCUS scheduled by EVGUI BITP 87*/
```

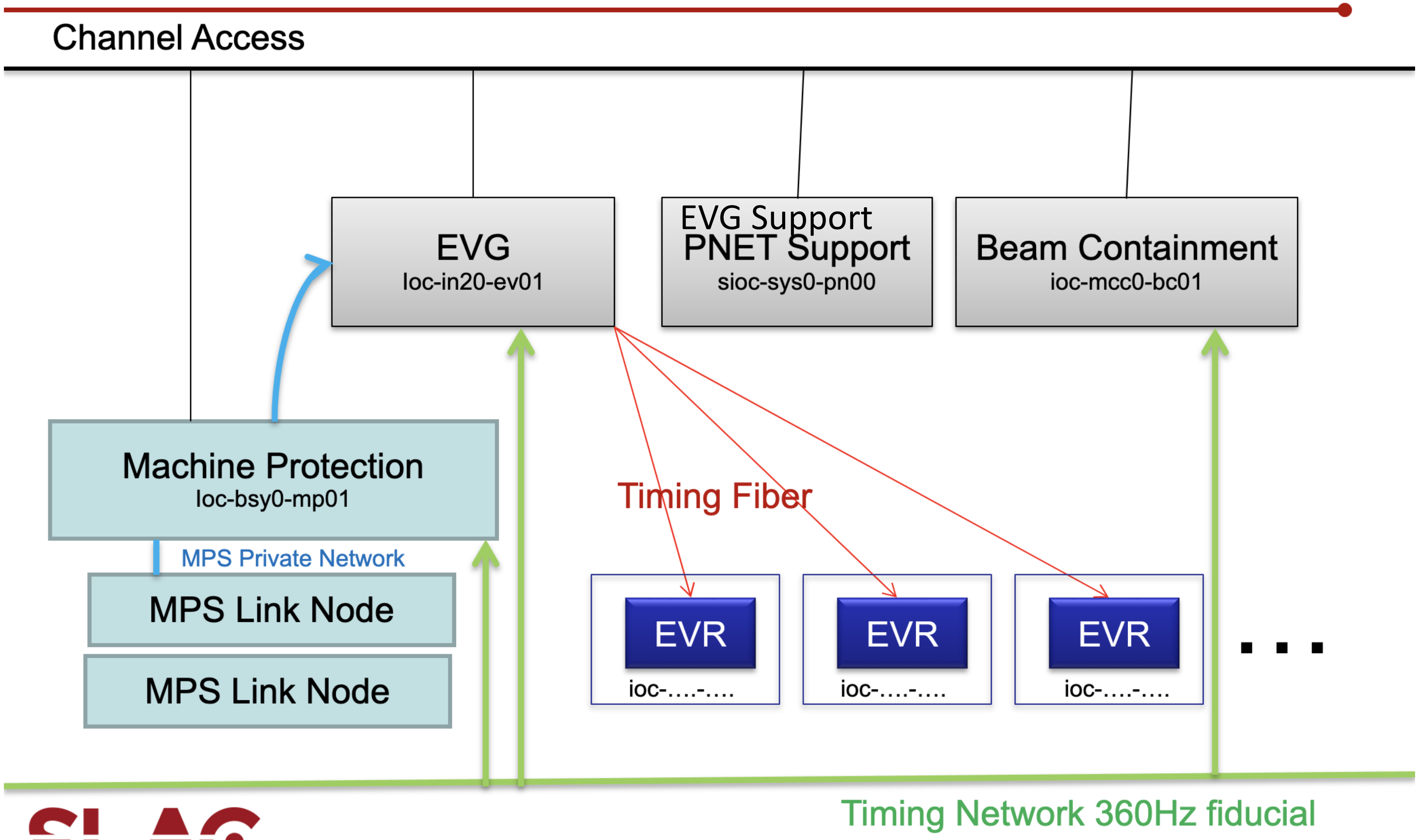
Take "RATE_MPS_HXR_05HZ" as example, (0x00000800), in hex, there are 32 bit for MOD3 section. Therefore, 0x00000800 = 0000100000000000. Which is 32*2-1+12 = 75; 32bit*(MOD#-1(=2))+Section BITP(0x00000800, position 12 in binary)-1(0-31, 32-63, 64-95,...) = Modifier BITP

EVG Note

- Modifier bit is 192 bit long that separated into 6 sections as MOD1-6
- Modifier bit repeat every 2 seconds as 720Hz
- Modifier bit is configurable
- Modifier bit and EVG event code both live in EVG
- Event code search from modifier bit for matching bit that fit the configuration of the event code
- Hence the event code could have its own frequency based on how often the matching condition shows up
- EVR receive the event code from EVG

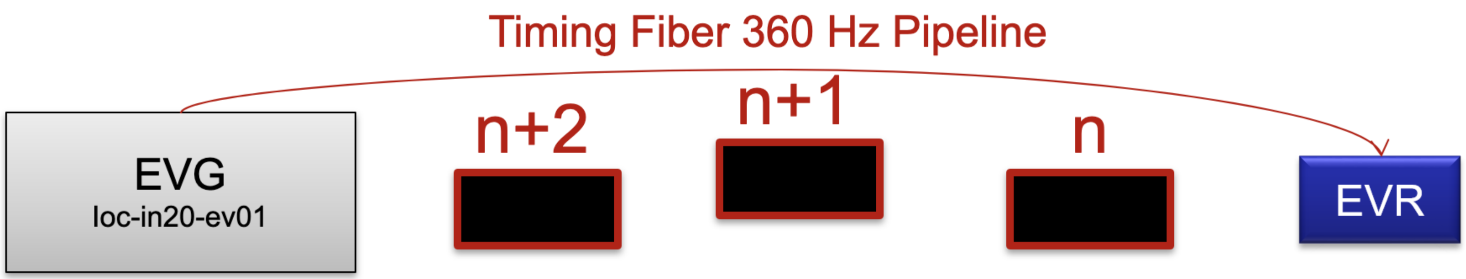
Timing pattern change

- There are only three scenario that change the timing pattern
  - MPS --> rate reduction
  - Manually shut off the beam
  - Hatch operator modify the pattern to lower the beam rate (kicker for rate reduction)
    - When changing pattern, the even code will change at the same time since the pattern got changed



Channel Access
EVG
Ioc-in20-ev01
EVG Support
PNET Support
sioc-sys0-pn00
Beam Containment
ioc-mcc0-bc01
Machine Protection
Ioc-bsy0-mp01
MPS Private Network
MPS Link Node
MPS Link Node
Timing Fiber
EVR
ioc-….-….
EVR
ioc-….-….
EVR
ioc-….-….
. . .
Timing Network 360Hz fiducial

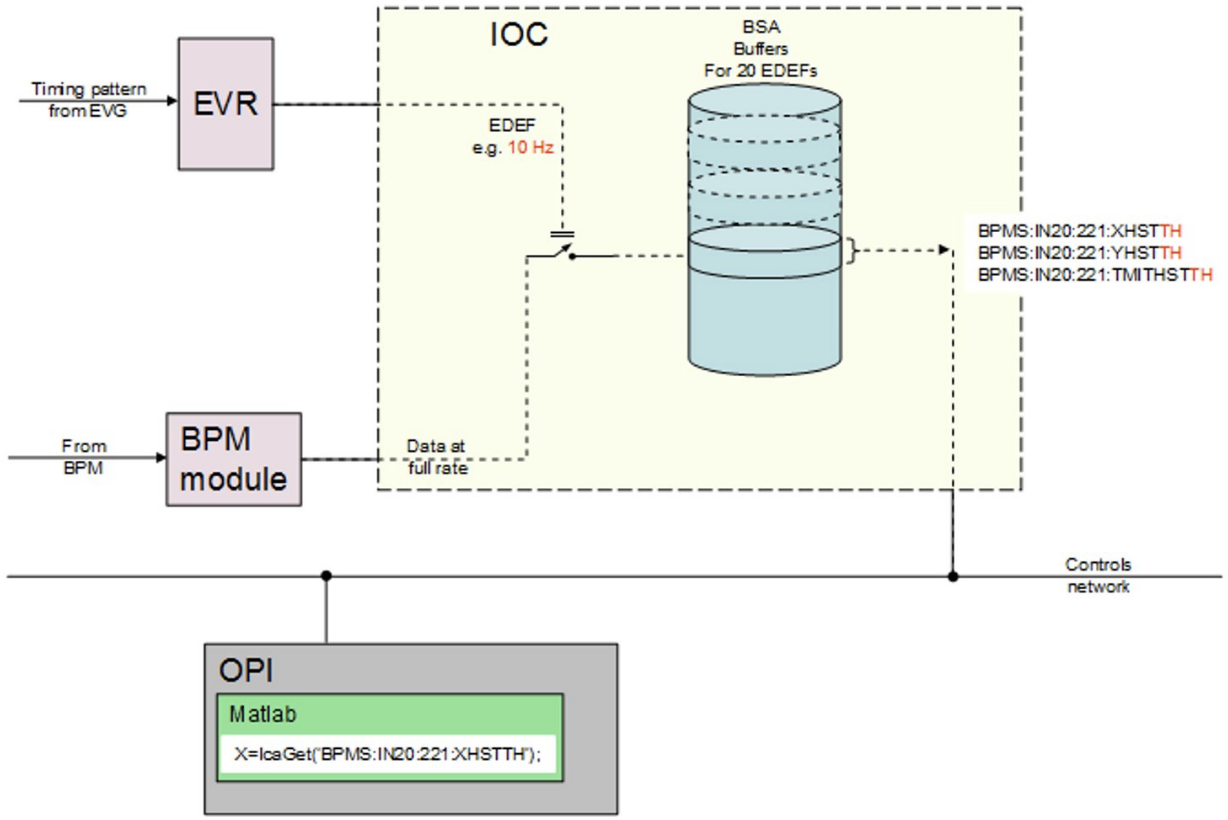
What does EVG send to EVR?



EVR receive three timing frame from EVG as called "**pipeline**". As EVR can see the next three timing frame from the pipeline, EVR can start pipeline, EVR can start preparation of the device so it can match up the time when there is a beam

For example,EVR can see n, n+1 and n+2. EVR knows the device ready time is two timing frame, once EVR sees n+2 is with beam and need the device to activate, at n it will start the preparation so when n+2 arrive it can perform in time.

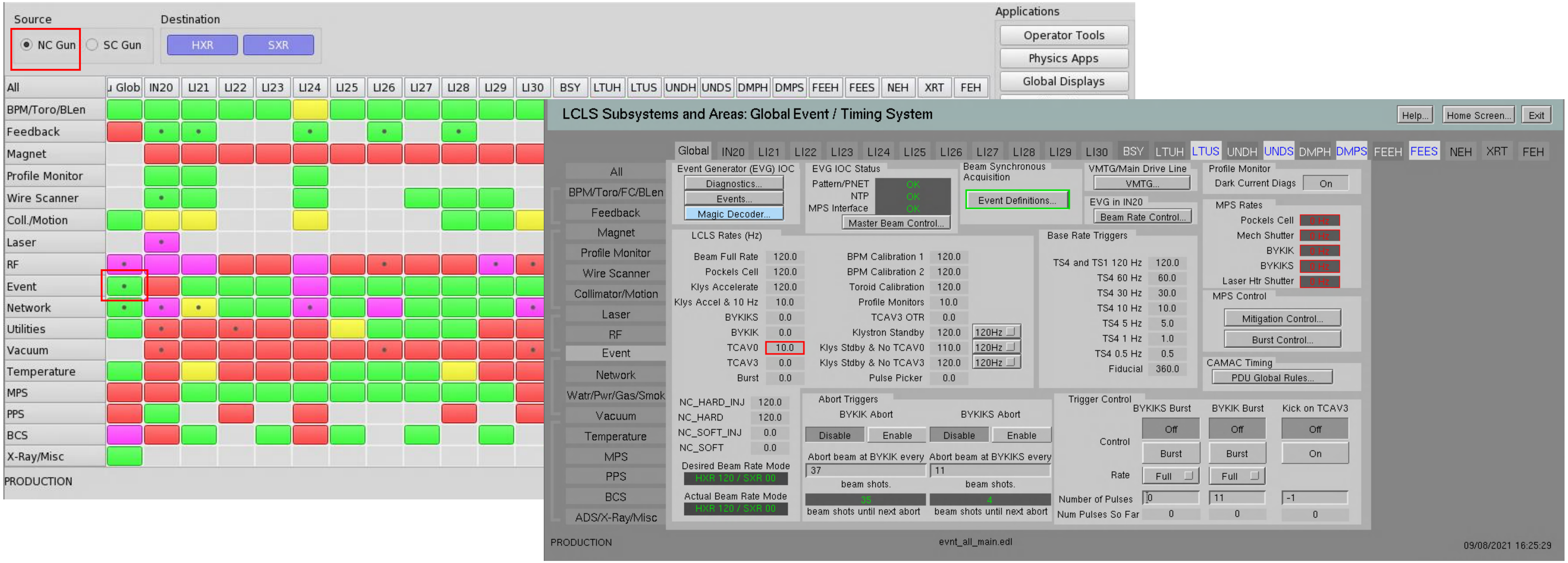
BSA (Beam Synchronous Acquisition)



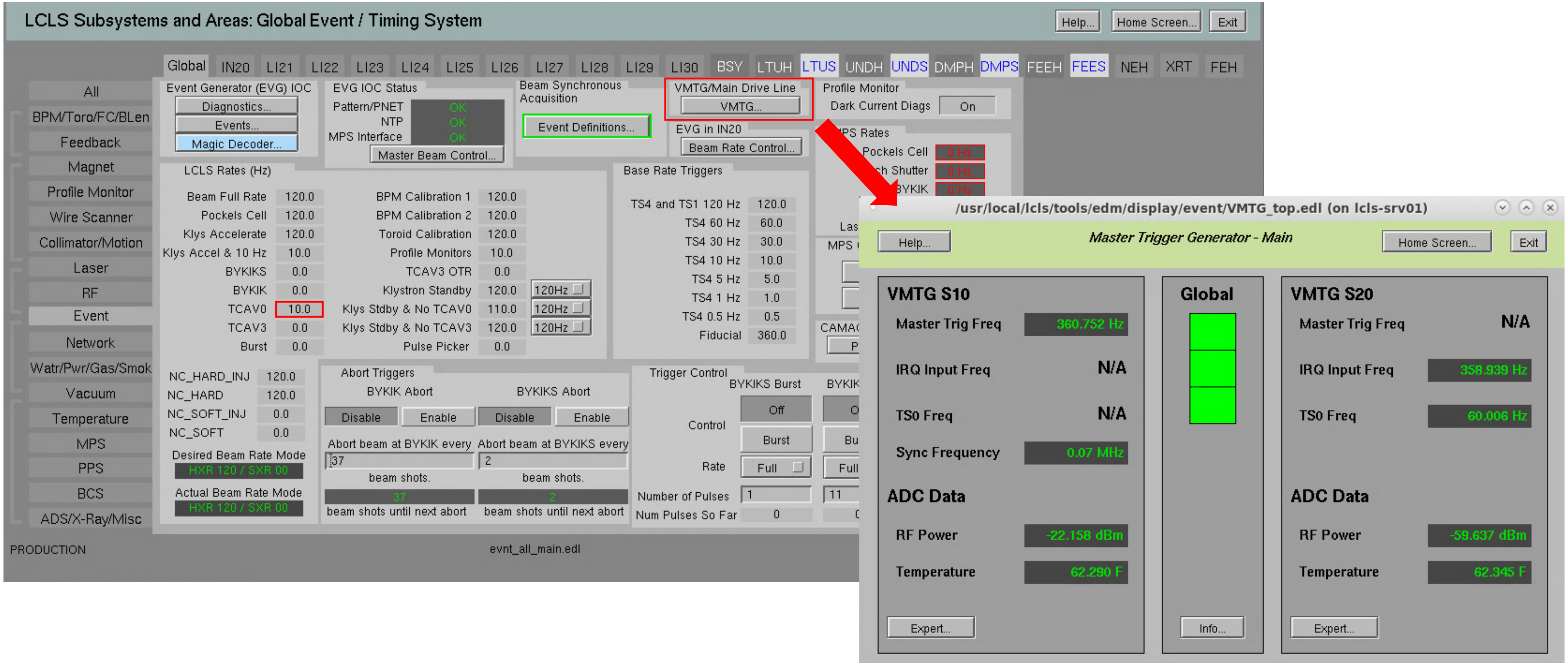
How to access NC EVG

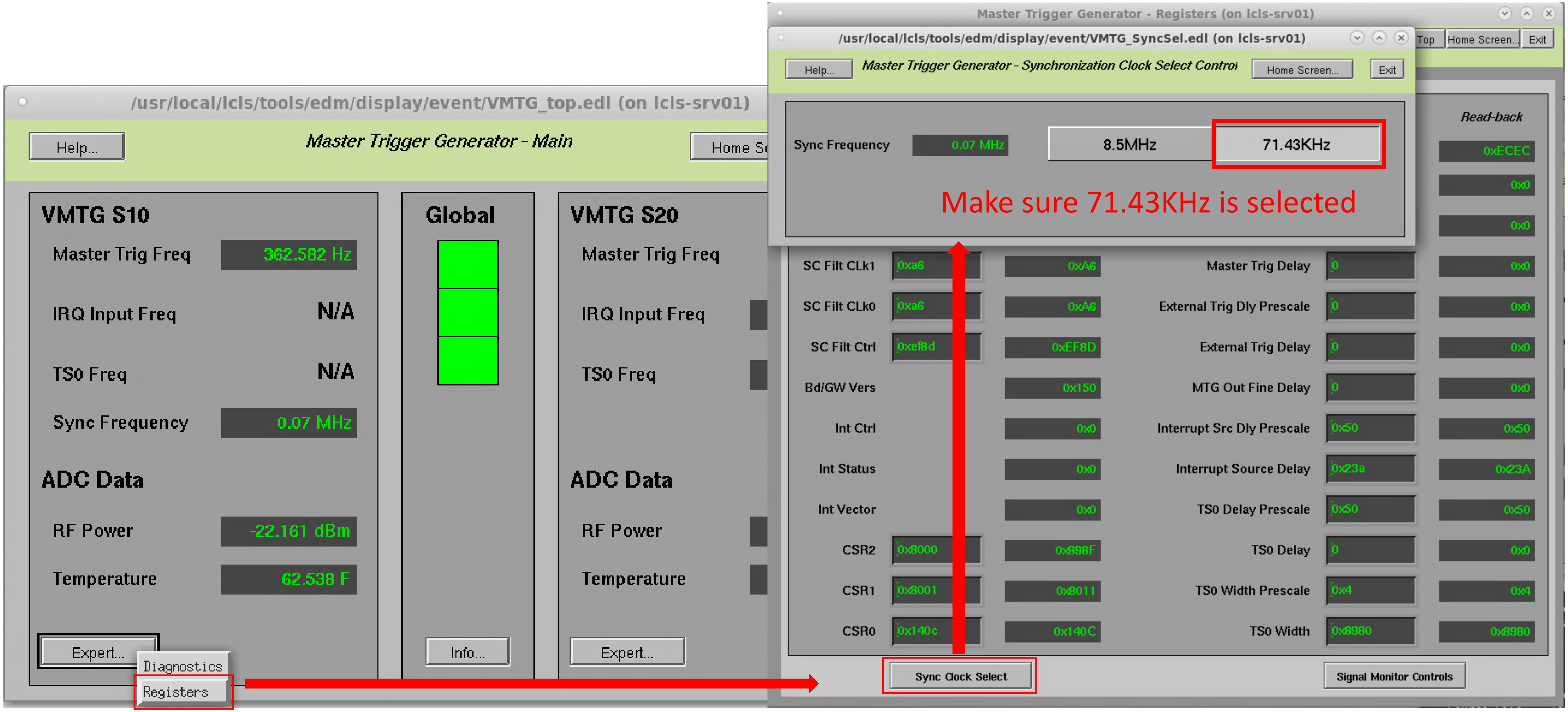
For further detail of EVG EDEF, see slide Cu-BSA.pptx

From *physics* account on Prod (lcls-srv01):
Reserve an *EDEF* with lclshome -> NC Gun -> Event / NC Global



EVG note when reboot





/usr/local/lcls/tools/edm/display/event/VMTG_top.edl (on lcls-srv01)
Help...
Master Trigger Generator - Main
VMTG S10
Master Trig Freq
362.582 Hz
IRQ Input Freq
N/A
TS0 Freq
N/A
Sync Frequency
0.07 MHz
ADC Data
RF Power
-22.161 dBm
Temperature
62.538 F
Expert...
Diagnostics
Registers
Global
Info...
VMTG S20
Master Trig Freq
IRQ Input Freq
TS0 Freq
ADC Data
RF Power
Temperature
Expert...
Master Trigger Generator - Registers (on lcls-srv01)
Top
Home Screen...
Exit
/usr/local/lcls/tools/edm/display/event/VMTG_SyncSel.edl (on lcls-srv01)
Help...
Master Trigger Generator - Synchronization Clock Select Control
Home Screen...
Exit
Sync Frequency
0.07 MHz
8.5MHz
71.43KHz
Make sure 71.43KHz is selected
Read-back
SC Filt CLk1
SC Filt CLk0
SC Filt Ctrl
Bd/GW Vers
Int Ctrl
Int Status
Int Vector
CSR2
CSR1
CSR0
Master Trig Delay
External Trig Dly Prescale
External Trig Delay
MTG Out Fine Delay
Interrupt Src Dly Prescale
Interrupt Source Delay
TS0 Delay Prescale
TS0 Delay
TS0 Width Prescale
TS0 Width
Sync Clock Select
Signal Monitor Controls

SC Timing

SC Timing

- SC BSA provides data buffers time stamped by the SC Timing System (Timing Pattern Generator – TPG).
- SC BSA provides data filtering according to user needs.
- SC BSA provides pulse-by-pulse data buffers up to 1KHz.
  - Maximum of 20000 data points.
  - Each data point can be an average of up to 1000 beam pulses
  - Maximum rate of 1KHz

- Difference NC BSA:

  -It is not a scaler acquisition

  -The acquisition cannot be run at beam rate but only up to 1KHz

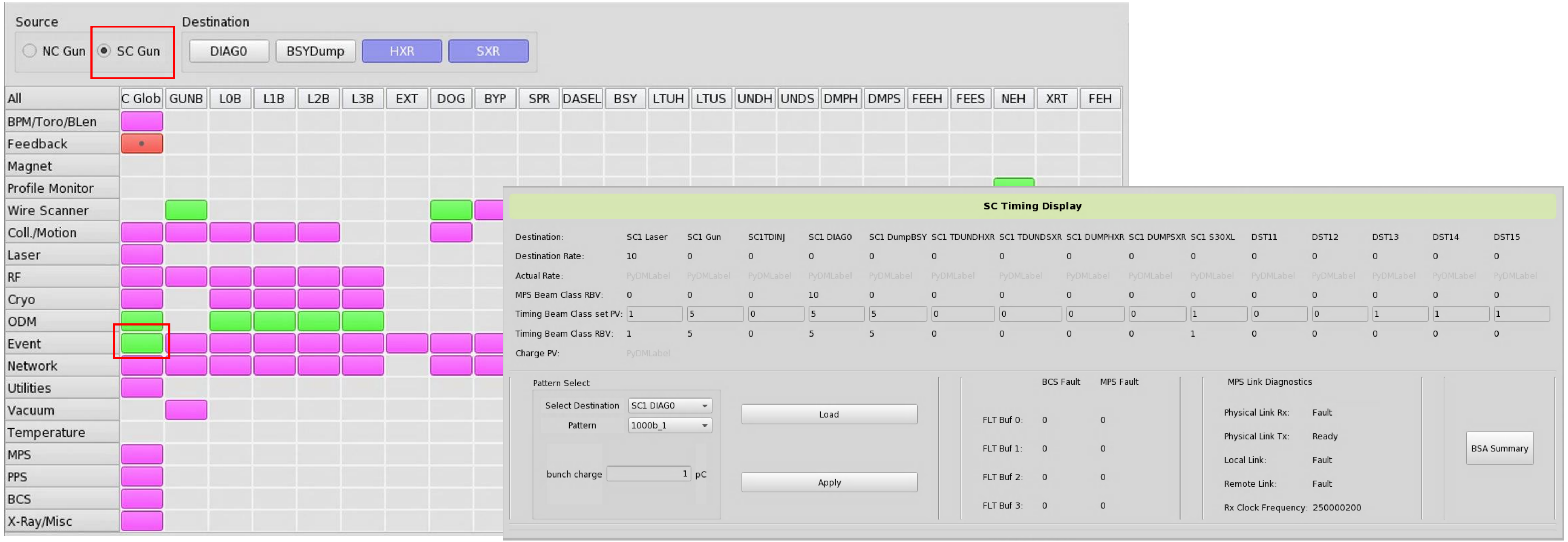
- Timing Pattern Generator (TPG) sends Timing Frames to each Timing Pattern Receiver (TPR) over a dedicated fiber network at 1MHz.
- PVs that participate in SC BSA have Pulse Id encoded into the nanoseconds part of their time stamp.

- An IOC is equipped with an TPR.
- Timing Fiber is run from TPG, most likely through a Fanout module.
- Special software is installed in the IOC that knows how to talk to the TPR.
- Assuming the requested signals can be read out within 1/120th sec from the hardware, EPICS Databases are created for the SC BSA PV.

How to access SC TPG?

For further detail of TPG BSA, see slide "SC-BSA.pptx"

From *physics* account on Prod (lcls-srv01):
Reserve an *BSA* with lclshome -> SC Gun -> Event / SC Global



- MPS issues permits for each destination

- Cu MPS permits are Rate based, max 120 Hz
- Each "mitigation device" (destination) has a maximum rate permit PV published as an enum *and* as a double. Note these are PERMITs, not actual rates

- SC MPS permits are Beam Class based
- Beam classes are defined as (1) integrated charge in (2) time window with some (3) minimum bunch spacing
- Each destination will publish the current beam class PERMIT as an enum and three PVs to provide the three parameters that define a beam class

- In both cases, timing system will publish the actual rate to a destination

Sc Timing pattern frame:

- Time
- PulseID
- Destination
- Fixed Rates
- AC Rates
- Beam Request
- Requested Charge
- MPS Valid
- BCS Fault
- MPS Limiting
- MPS Limits
- BSA fields (Init; Active: AvgDone; Update)

Cu Timing pattern frame:

- Time
- PulseID
- Beam Code (BC) (0=Any, 1=Cu to HXR, 2= Cu to SXR –see next slide)
- Event Codes
- Modifier bits: time slot; kicker trigger mask presence; beam presence; subset of lower rate trigger mask per destination; etc..
- BSA fields

Note: The information is packaged / called a little bit different, but it is similar concept.

BSA and TPG

- TPG generate timing pattern where BSA acquire along with other device signals (MPS, BPM etc..) or signal (PID, TS, etc..)
- As the result BSA generate PV record with device signal and TPG signal
  - Ex, TPG:SYS0:1:TSPIDHST21

Device name or Signal name

BSA data that aquire with the device signal

BSA

- When BSA acquistion start, BSA acquire data from TPG timing pattern. Under "view data" is where the device signal tie to the BSA acquired data to output data graph
- In this case each data capture from the device or signal will have BSA timing pattern attached to it for further experiment.
- Each data point have corresponding BSA data singal to it like example below where they have same length of array representing each data point

```
justinc@lcls-dev3[~]: caget TPG:SYS0:1:TSCNTHST21
TPG:SYS0:1:TSCNTHST21 100 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
justinc@lcls-dev3[~]: caget TPG:SYS0:1:TSRMSHST21
TPG:SYS0:1:TSRMSHST21 100 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Note

- LCLS1:0…120Hz
- LCLS2:0…1MHz
  - **PDU = Programmable Delay Unit**
- The PDU is where timing and pattern information meets the fiducial and the 8.4 ns clock from the FIDO and triggers with appropriate delays are output on the CAMAC upper backplane.
- PDU outputs 16 triggers of 67.2 ns width at ECL levels (~-0.8V to 1.8V)

Troubleshoot for LCLS EVG

```
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
```

The error shown the wall wart is still on with generator or regular power supply without the wall wart

Q&A

- Why the signal needs to be amplified at sector 30 since only 30 sectors exist
- 3pf