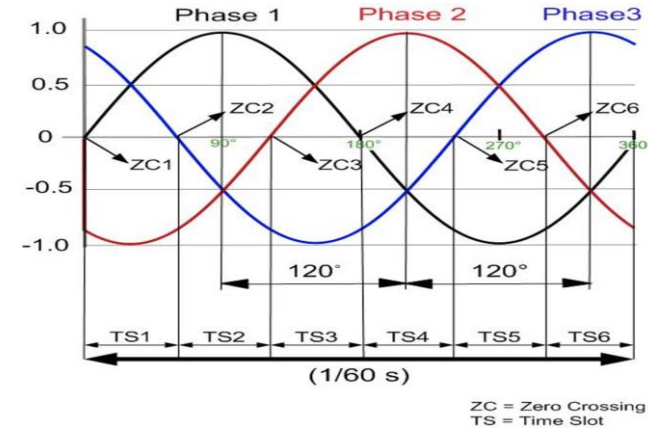
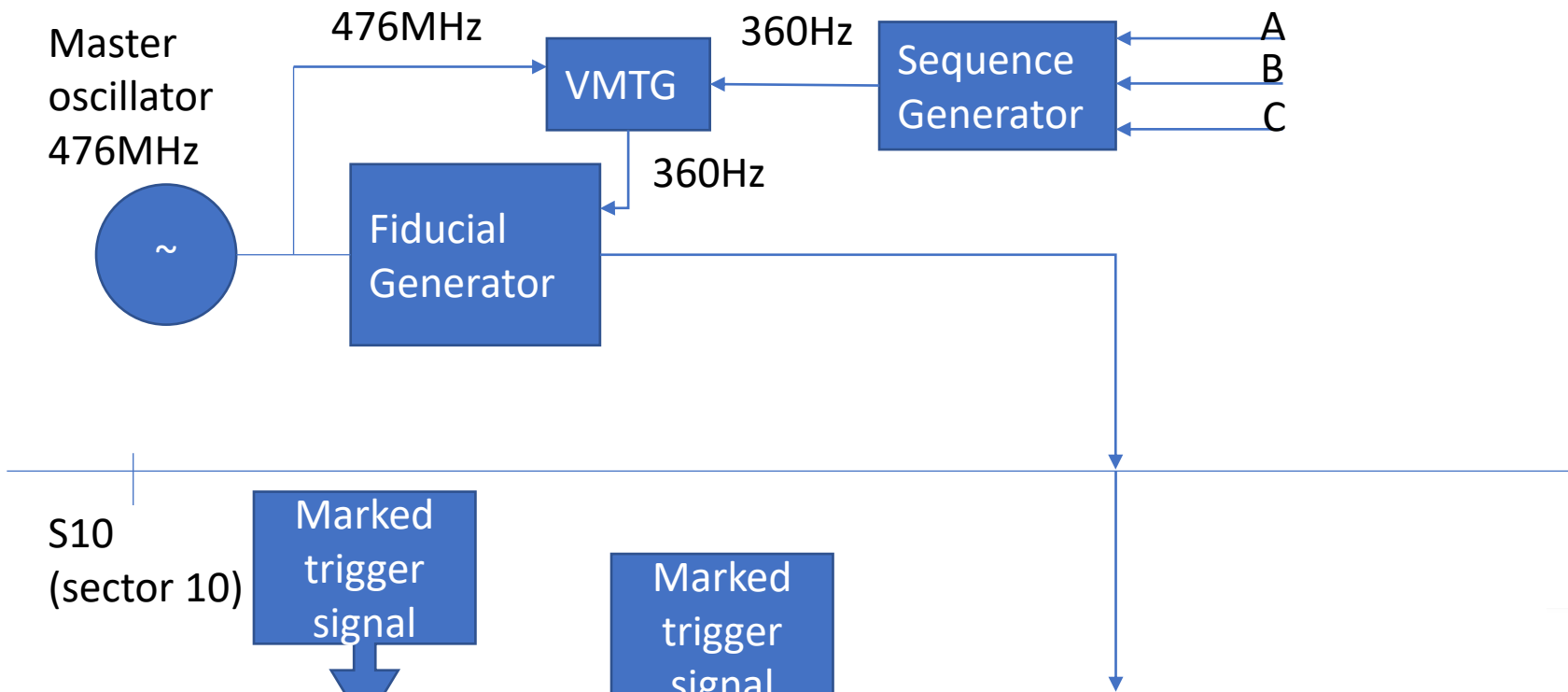


# Timing for LCCLS

VMTG is to sync the RF with PG&E signal to define timeslots

A, B, C are the three 60Hz from PG&E with different phase to generate 6 time slots



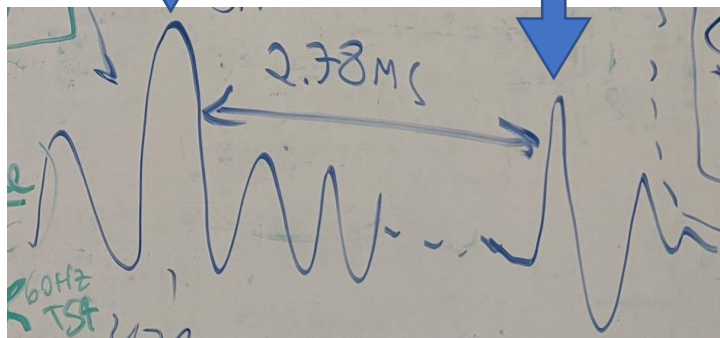
LCLS use timeslots 1&4

In sector 10 is where is timing trigger signal is generated and be used at all other sectors and buildings.

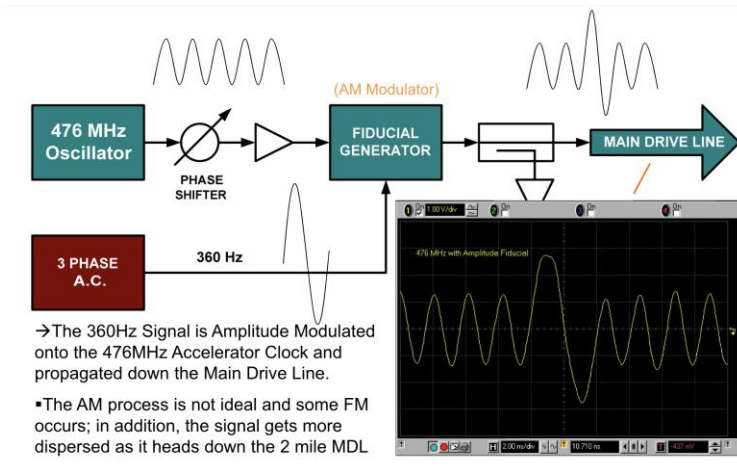
S10  
(sector 10)

Marked  
trigger  
signal

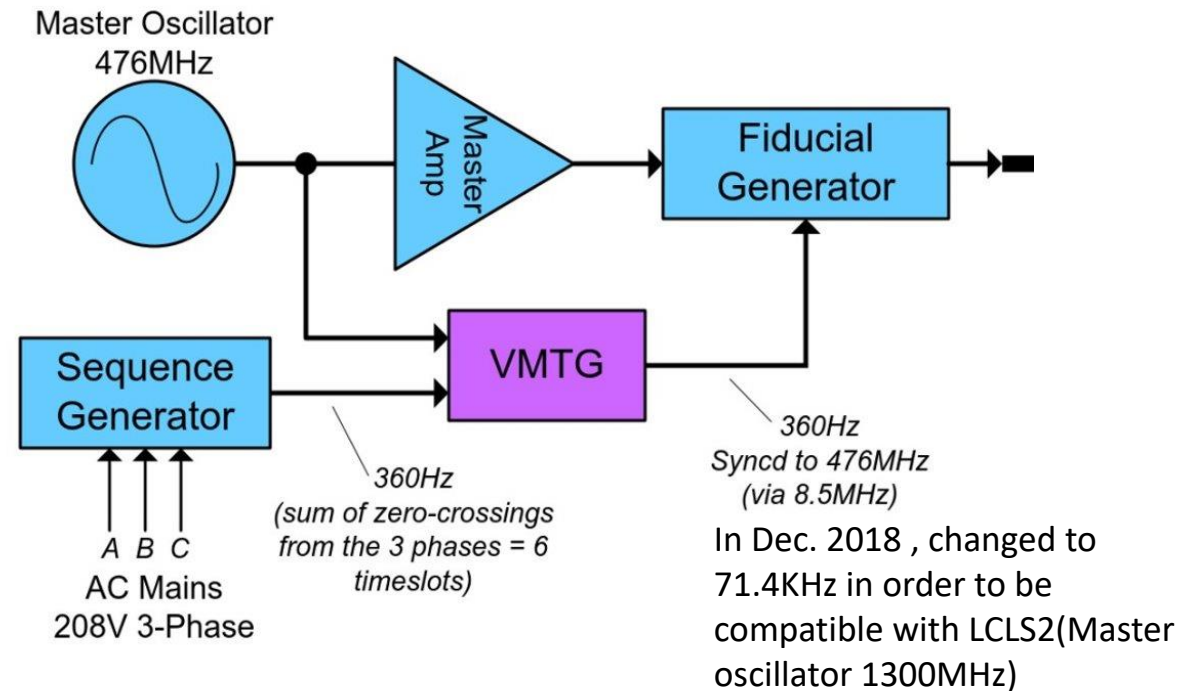
Marked  
trigger  
signal



The 360Hz signal is Amplitude Modulated onto the 476MHz Accelerator Clock and propagated down the Main Drive Line (2.78ms is the timing between two triggers)



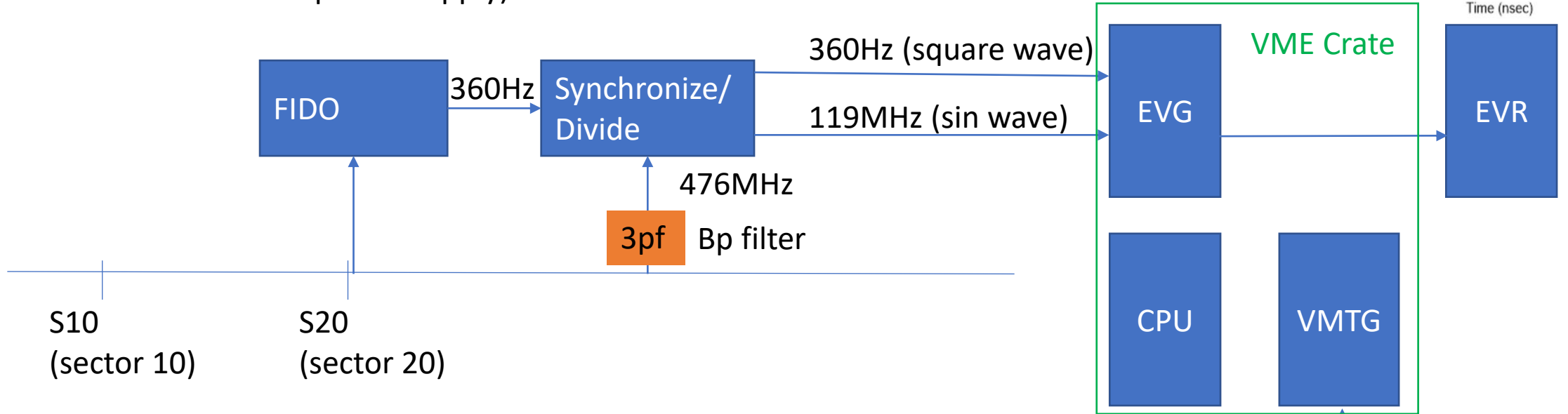
A Sequencer chassis derives a 360 Hz signal coincident with the zero crossing of the 3 phase AC power. This is combined with 476 MHz from a precision COTS Master Oscillator. These signals are combined in a VME-based Master Trigger Generator which fires the Fiducial Generator which combines with the 476 MHz for distribution on the Main Drive Line.



*LI00 Master RF Phase Ref & Timing Fid Source*

Moved from LI00 to IN10 (2017)

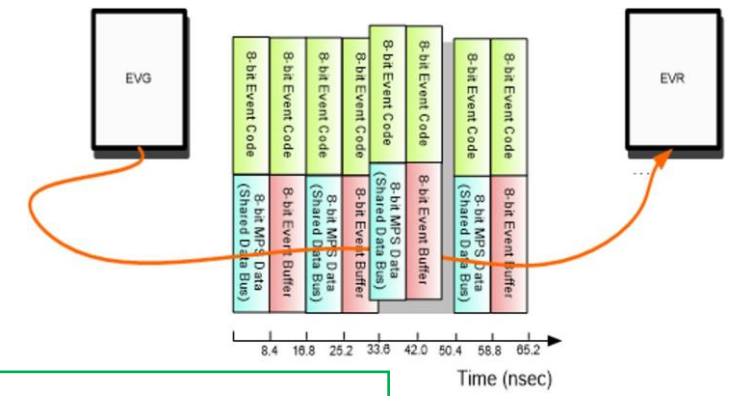
LCLS runs at a maximum rate of 120 Hz  
 (Each timeslot represent 60 Hz signal,  
 ex. LCLS timeslot 1 and 4 which is 120  
 Hz which is the maximum rate of RF  
 hardware power supply)

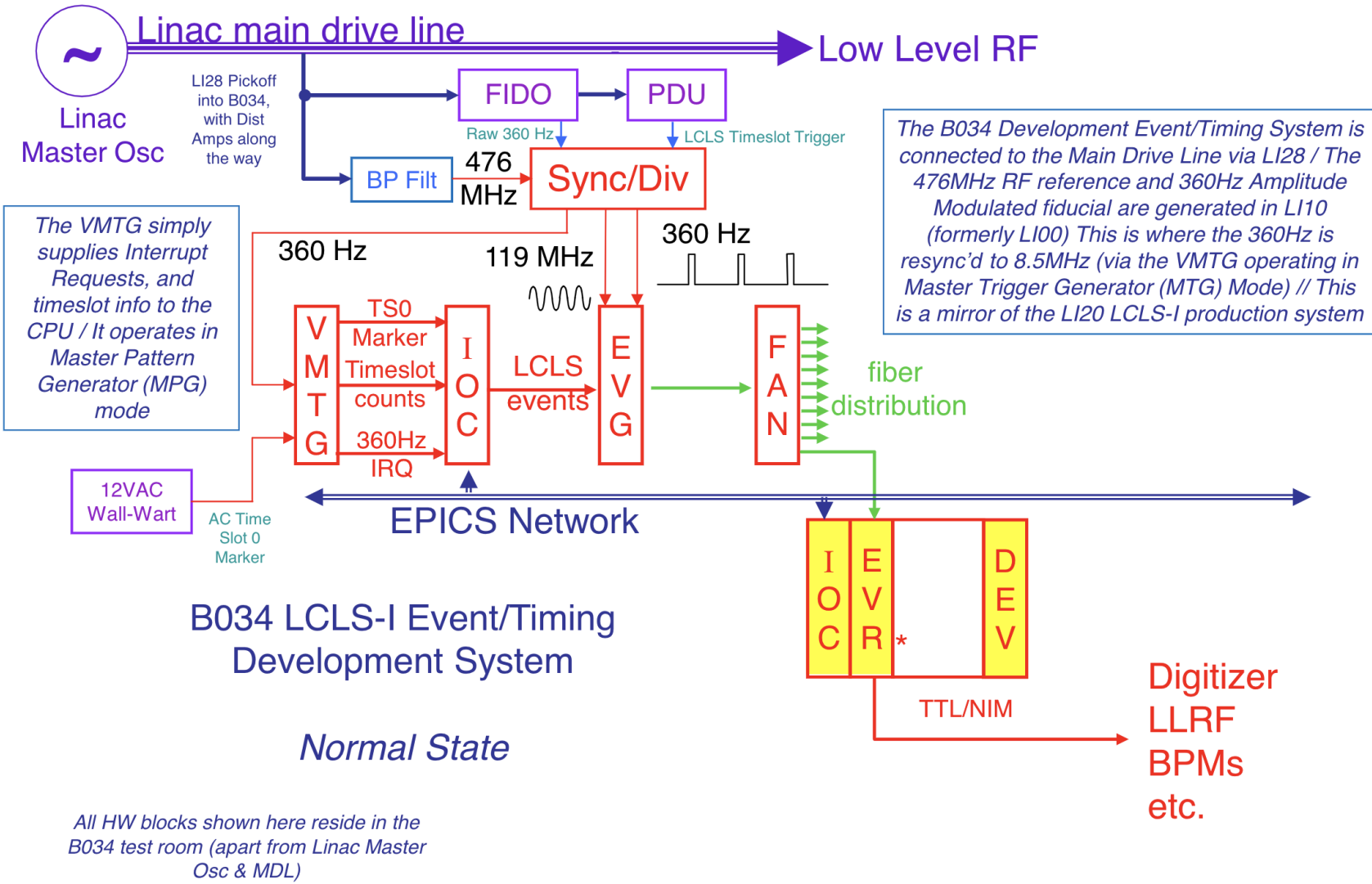


476MHz is divided/4 to get 119Mhz+fiducial by another system / This is because the older technology HW could not run at 476MHz

Sector 30 with amplifier to amplify the signal from Main Drive

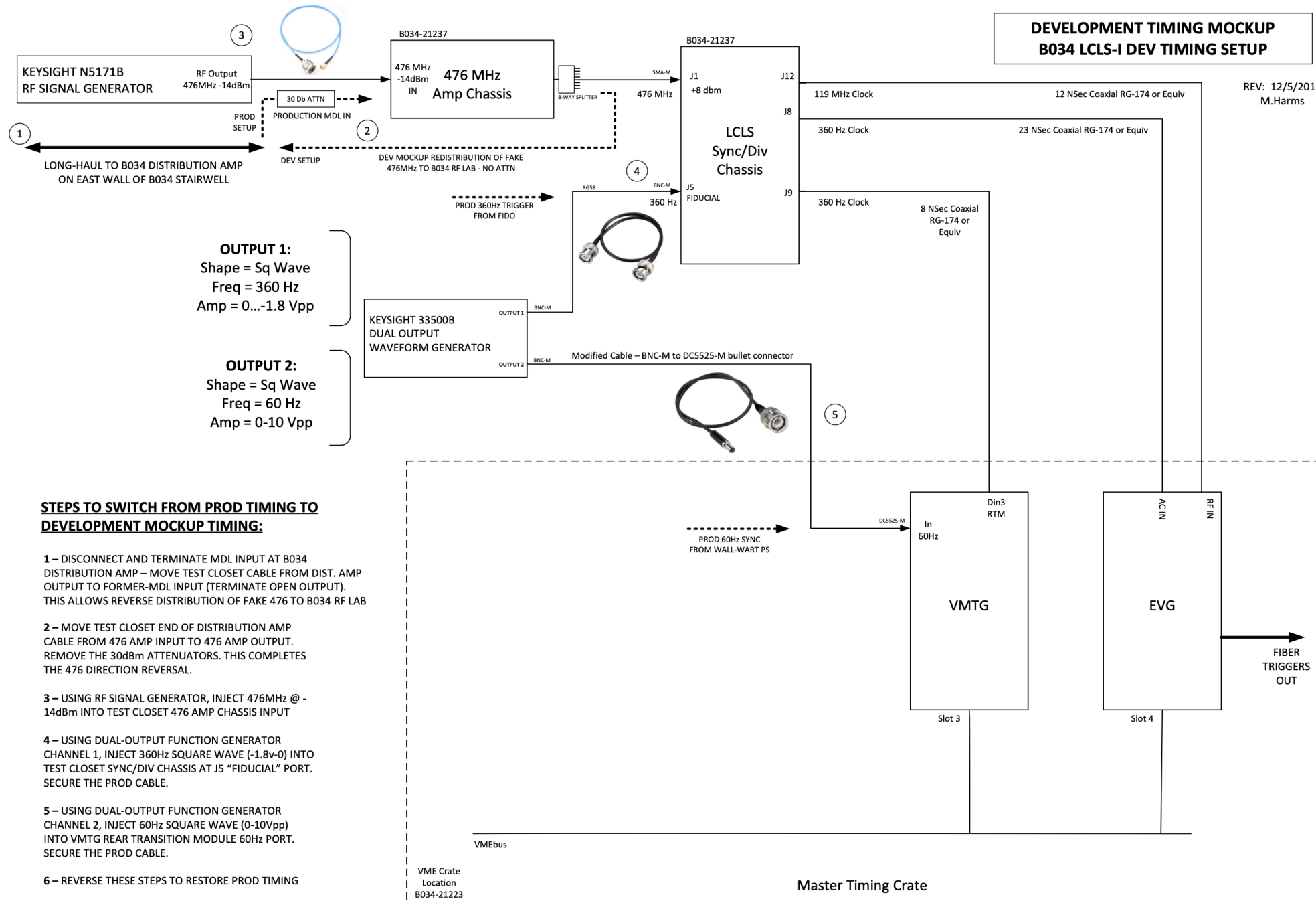
60Hz  
 60Hz Fiducial act as the mark on the trigger form to indicate 0 crossing of ts1





**DEVELOPMENT TIMING MOCKUP  
B034 LCLS-I DEV TIMING SETUP**

REV: 12/5/2019  
M.Harms



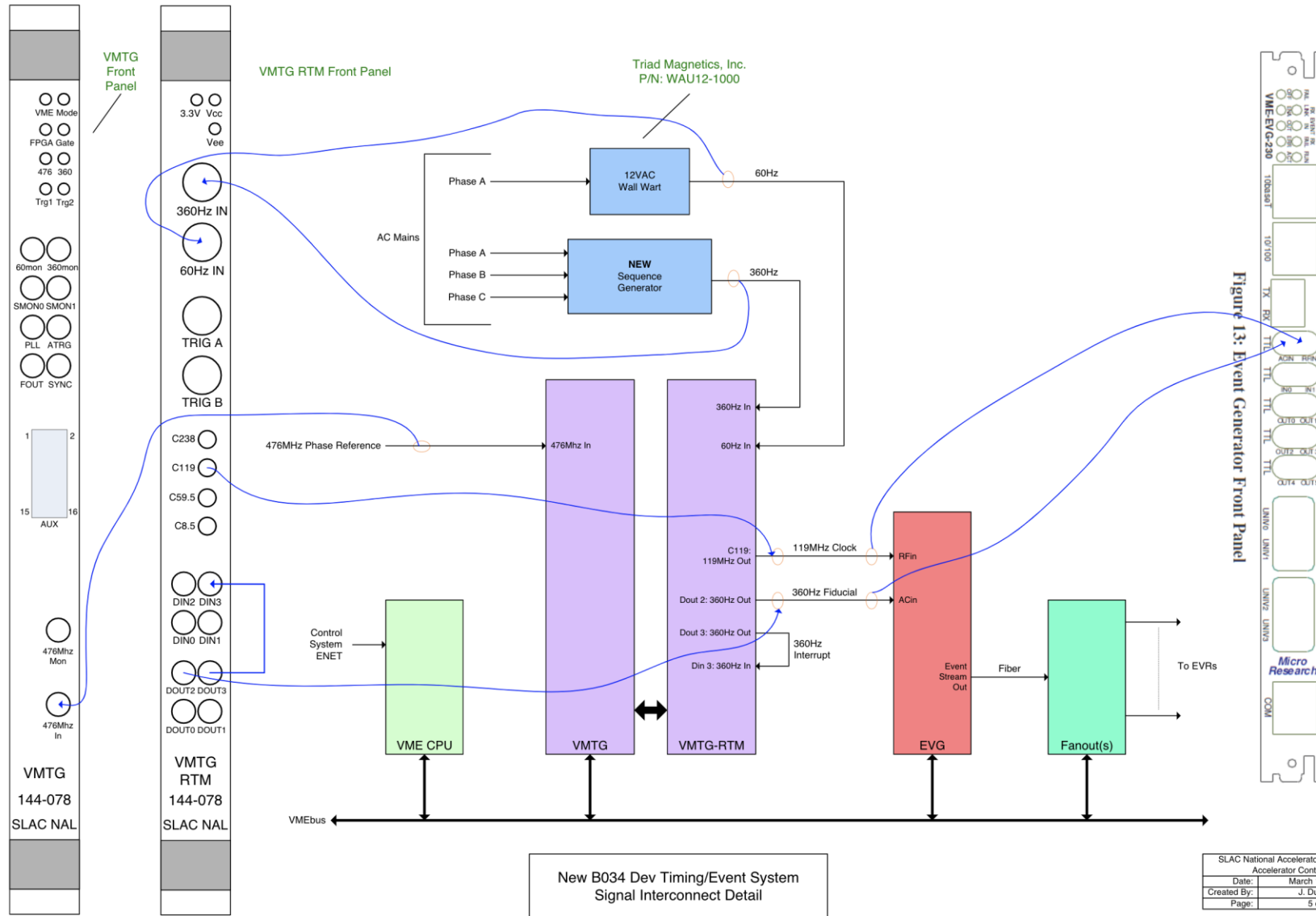


Figure 13: Event Generator Front Panel

# NC Timing

- Cu BSA provides scalar data that is time stamped by the Timing (Event) System.
- Cu BSA provides data filtering according to user needs.
- Cu BSA provides pulse-by-pulse data buffers up to the beam rate.
  - Maximum of 2800 data points.
  - Each data point can be an average of up to 1000 beam pulses
  - Maximum rate of 120 Hz.
  - ~1700 Cu BSA signals.



# EVG ioc name

- EVG-Event Generator
  - EVG is an IOC
  - loc-in20-ev01 for LCLS -(PV SYS0)
  - loc-sys1-ev01 for FACET
  - loc-xt01-ev01 for XTA -(PV SYS6)
  - loc-b34-ev01 for Development -(PV SYS0)
  - loc-as01-ev01 for ASTA (Test Facility) -(PV SYS7)
  - Runs epics/ioc/MpgApp (CVS module is Mpg)

# NC Timing Frame

- The **timing frame** contains the information regarding the current operating mode:
  - Time
  - PulseID
  - Beam Code (BC) (0=Any, 1=Cu to HXR, 2= Cu to SXR –see next slide)
  - Modifier bits: time slot; kicker trigger mask presence; beam presence; subset of lower rate trigger mask per destination; etc..
  - Event Codes
  - BSA fields
- N timing frame : 1 Timing Pattern
- The **timing pattern** is used by the receiver to:
  - Trigger devices
  - Trigger Data acquisition using Beam Synchronous Acquisition (BSA)

- An IOC is equipped with an EVR.
- Timing Fiber is run from EVG, most likely through a Fanout module.
- Special software is installed in the IOC that knows how to talk to the EVR.
- Assuming the requested signals can be read out within 1/120th sec from the hardware, EPICS Databases are created for the Cu BSA PV.

# Timing Pattern

LCLS Subsystems and Areas: Global Event / Timing System

Global IN20 LI21 LI22 LI23 LI24

Event Generator (EVG) IOC: IN20:EVG01

Diagnosics Events... Magic Decoder...

LCLS Rates (Hz)

Beam Full Rate	120.0
Pockels Cell	120.0
Klystron Accelerate	120.0
Klystron Accel & 10 Hz	10.0
BYKIKS	0.0
BYKIK	0.0
TCAV0	0.0
TCAV3	0.0
Burst	0.0

NC\_HARD\_INJ 120.0  
NC\_HARD 120.0  
NC\_SOFT\_INJ 0.0  
NC\_SOFT 0.0

Desired Beam Rate Mode: HZR 120 / SXR 00  
Actual Beam Rate Mode: HZR 120 / SXR 00

Abort Triggers: BYKIK Abort, Disable, Enable

Abort beam at BYKIK: 2

beam shots: 1

beam shots until next: 1

IN20 EVG Events Development

Event Code Sequence Events Time Slot 1 to 6 Event Codes Pattern EVG EXIT

Name	Event Code (Clock Ticks)	Delay* (nsec)	On/Off	Rate (Hz)	Pattern Pipeline
Fiducial	1	0	0	360.0	OK
Heartbeat	122	1	1	360.0	
360Hz	9	12950	108706 1	360.0	

\* Delay (nsec) = (Delay + Delay Offset for All Events) / 11899921 (Hz) \* 1E9

Delay Offset for All Events (Clock Ticks): -14

Acquisition Count: Mask Setup Count BPM Masks 71905549

LCLS Beam Events

Name	Event Code (Clock Ticks)	Delay* (nsec)	On/Off	Beam Mask Code Setup	Rate (Hz)	Name	Event Code (Clock Ticks)	Delay* (nsec)	On/Off	Beam Mask Code Setup	Rate (Hz)	Desired Rate (Hz)
Beam Full	140	11900	99882 1 0	Masks	120.0	Klystron Standby	152	11912	99983 1 0	Masks	60.0	60Hz
Beam&60Hz	141	11901	99891 1 1	Masks	60.0	Klystron Standby & No TCAV0	153	11913	99992 1 0	Masks	60.0	60Hz
Beam&30Hz	142	11902	99899 1 1	Masks	30.0	Klystron Standby & No TCAV3	157	11917	100025 1 0	Masks	60.0	60Hz
Beam&10Hz	143	11903	99908 1 1	Masks	10.0	Klystron Accel and 10Hz	154	11914	100000 1 1	Masks	10.0	
Beam & 5Hz	144	11904	99916 1 1	Masks	5.0	OTRDMP	155	11915	100008 1 3	Masks	0.0	
Beam & 1Hz	145	11905	99924 1 1	Masks	1.0	Pockels Cell	158	11918	100034 1 1	Masks	120.0	
Beam&0.5Hz	146	11906	99933 1 1	Masks	0.5	Profile Mon	159	11919	100042 1 1	Masks	10.0	
Full N-1	147	11907	99941 1 1	Masks	120.0	TCAV3 OTR	160	11920	100050 1 1	Masks	0.0	
Full N-2	148	11908	99950 1 1	Masks	120.0	BYKIKS	161	11921	100059 1 1	Masks	0.0	
TCAV0	149	11909	99958 1 1	Masks	0.0	BYKIK	162	11883	99740 1 1	Masks	0.0	
TCAV3	156	11916	100017 1 1	Masks	0.0	A-Line KICK	163	11922	100067 1 1	Masks	0.0	
Burst	150	11910	99966 1 1	Masks	0.0	Pulse Picker	164	11923	100076 1 1	Masks	0.0	
Klystron Accel	151	11911	99975 1 1	Masks	120.0	OTRDMPB	165	11924	100084 1 1	Masks	360.0	

MPS Checkout EC... Machine Checkout EC...

User-Defined Event Codes

Name	Event Code (Clock Ticks)	Delay* (nsec)	On/Off	Beam Mask Code Setup	Rate (Hz)
Dual Laser Diagnostics	131	11925	100093 1 1	Masks	120.0
Tse.140.exclude.bykik	132	11926	100101 1 1	Masks	120.0
User Defined 3	133	11927	100109 1 1	Masks	120.0
LINAC_ONE_HERTZ - 10/120th sec	134	11928	100118 1 1	Masks	120.0
User Defined 5	135	11929	100126 1 1	Masks	120.0

IN20 EVG Diagnostics (on lcls-dev3)

IOC:IN20:EVG01 EVG Diags Development EVG EXIT

Pattern Pipeline OK

PULSEID	TS1	TS6	TS5	TS4
BEAMCD	0x167D	0x167C	0x167B	0x167A
TIMESLOT	1	6	5	1
MODIFIER1	0x8100	0x0	0x0	0x100
MODIFIER2	0x1	0x20	0x10	0x8
MODIFIER3	0x7EE000	0x0	0x0	0x8E10F
MODIFIER4	0x20000000	0xC0000000	0xA0000000	0x80000000
MODIFIER5	0x13FE7800	0x20000000	0x20000000	0x120E7800
MODIFIER6	0x0	0x0	0x0	0x0
AVGDONE	0xE7800	0x0	0x0	0xE7800
ALLDONE	0x0	0x0	0x0	0x0

Time Pipeline

Seconds	0x3BA45E41	0x3BA45E41	0x3BA45E41	0x3BA45E41
Nsec				

Status: 0x0 0x0 0x0 0x0

Counters All Counter Reset

Total	215771221	TS Sync Error	1
Rollover of Total	0	TS Pattern Sync Error	0
Total (ISR) Writes	215739519	TS/Pattern Mismatch	0
Rollover of Writes	0	Sequence RAM Busy	0
Invalid Waveform	0	Seq RAM Mode Error	0
Timeouts	0	Sequence RAM Active	31700
Write Error	0	Seq Ram Lock Error	0
ISR Overwrite	0	Seq Ram Invalid Data	47982
Backward Time Err**	0	MPS State	TIMEOUT
NTP Error	0	Total MPS Messages	0
Invalid MPS Data	215723845	Rollover of Above	0
Mod 720 Sync Error	0	MPS Timeout	0
Pulse ID Sync Error	0	MPS Invalid Message	0
Pulse ID Rollover	1646	MPS Unknown Msg	0
NTP State	OK	MPS Parse Error	0
		MPS Invalid Time	0
		MPS Time Off-By-One	0

Processing Time (us) Send MPS Test Msg

Record Average	101	Fiducial Average	56
Record Maximum*	128848919	Fiducial Maximum*	865
Start Time Diff Min*	2689	MPS Time Diff Min*	30000
Start Time Diff Max*	58316	MPS Time Diff Max*	0
Rate (Hz)	360.0	MPS from Patt Min*	30000
* Since Reset ** Since Boot		MPS from Patt Max*	0

IN20 EVG Diagnostics (on lcls-dev3)

IOC:IN20:EV01 EVG Diags Development

EVG EXIT

**Pattern Bits**

	TS1	TS6	TS5	TS4
PULSEID	0x167B	0x167C	0x167B	0x167A
BEAMCD	1	0	0	1
TIMESLOT	1	6	5	4
MODIFIER1	0x8100	0x0	0x0	0x100
MODIFIER2	0x1	0x20	0x10	0
MODIFIER3	0x7EE000	0x0	0x0	0x8E0
MODIFIER4	0x20000000	0xC0000000	0xA0000000	0x80000000
MODIFIER5	0x13FE7800	0x20000000	0x20000000	0x120E7800
MODIFIER6	0x0	0x0	0x0	0x0
AVGDONE	0xE7800	0x0	0x0	0xE7800
ALLDONE	0x0	0x0	0x0	0x0

**Time Pipeline**

Seconds	0x3BAA5E41	0x3BAA5E41	0x3BAA5E41	0x3BAA5E41
Nsec				

Status: 0x0 0x0 0x0 0x0

**Counters** All Counter Reset

Total	215771221	TS Sync Error	1
Rollover of Total	0	TS/Pattern Sync Error	0
Total (ISR) Writes	215739519	Sequence RAM Busy	0
Rollover of Writes	0	Seq RAM Mode Error	0
Invalid Waveform	0	Sequence RAM Active	31700
Timeouts	0	Seq Ram Lock Error	0
Write Error	0	Seq Ram Invalid Data	47382
ISR Overwrite	0	MPS State	TIMEOUT
Backward Time Err**	0	Total MPS Messages	0
NTP Error	0	Rollover of Above	0
Invalid MPS Data	215723845	MPS Timeout	0
Mod 720 Sync Error	0	MPS Invalid Message	0
Pulse ID Sync Error	0	MPS Unknown Msg	0
Pulse ID Rollover	1646	MPS Parse Error	0
NTP State	OK	MPS Invalid Time	0
		MPS Time Off-By-One	0

**Processing Time (us)** Send MPS Test Msg

Record Average	101	Fiducial Average	56
Record Maximum*	128848919	Fiducial Maximum*	865
Start Time Diff Min*	2689	MPS Time Diff Min*	30000
Start Time Diff Max*	58316	MPS Time Diff Max*	0
Rate (Hz)	360.0	MPS from Patt Min*	30000
* Since Reset		MPS from Patt Max*	0
** Since Boot			

Timing Pattern Bits (PNBN)

EXIT

Units 1 to 20 Units 61 to 80

Units 21 to 40 Units 81 to 100

Units 41 to 60 Units 101 to 120

Units 121 to 140

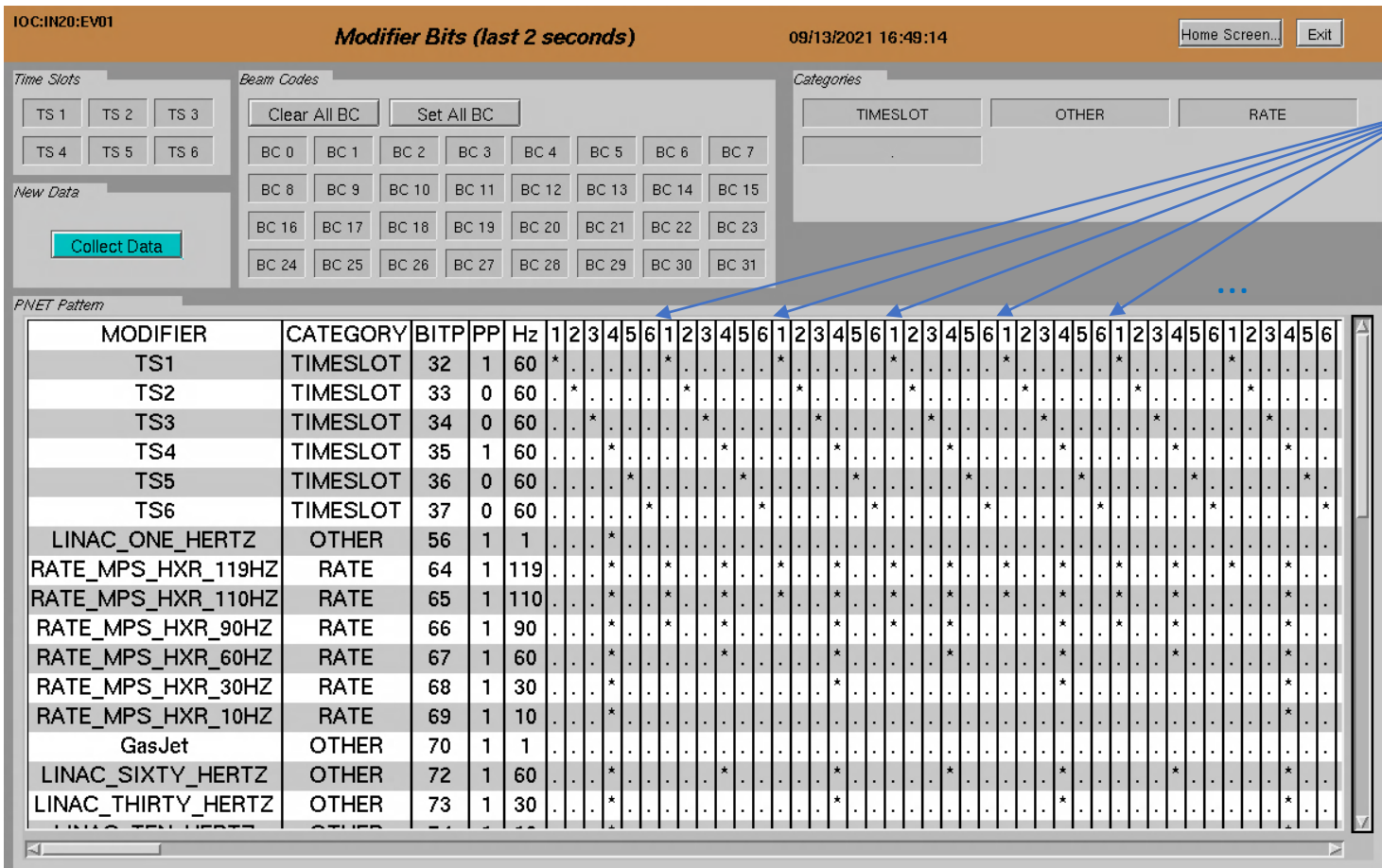
Timing Pattern Bits

Timing Pattern Units 1 to 20

EXIT

Bit Posn	# of Bits	Name
0	8	YY
8	5	PP
14	1	MPG_IPLING
15	1	MOD720RESYNC
16	4	PULSIDRESYNC
21	1	
22	1	
23	1	
24	1	
25	1	
26	1	
27	1	
28	1	
29	1	
30	1	
20	12	PSK_CONTROL
32	6	TSL0T_U6
32	1	TS1
33	1	TS2
34	1	TS3





The pattern repeat every 360 cycles (360Hz) --> 60(each time slot is 60Hz)\*6(6 time slots)=360Hz  
 For LCLS the maximum rate is 120Hz since it uses S1 & S4 (60+60=120Hz)  
 LCLS can have timing send out timing pattern frame in 120Hz

Each pattern contain 60 times 6 time slots, ex, TS1 send out 60 times of data in one pattern.

Each timeslot can hold timing frame shown in p.11

The slowest rate it can send is 1bit per 360 cycles -->1Hz

# Modifier section

IN20 EVG Diagnostics (on lcls-dev3)

IOC:IN20:EV01 EVG Diags Development

Buttons: EVG, EXIT

Section: Pattern Pipeline

	TS1	TS6	TS5	TS4
PULSEID	0x167D	0x167C	0x167B	0x167A
BEAMCD	1	0	0	1
TIMESLOT	1	6	5	4
MODIFIER1	0x8100	0x0	0x0	0x100
MODIFIER2	0x1	0x20	0x10	0x8
MODIFIER3	0x7EE000	0x0	0x0	0x8E10F
MODIFIER4	0x20000000	0xC0000000	0xA0000000	0x80000000
MODIFIER5	0x13FE7800	0x20000000	0x20000000	0x120E7800
MODIFIER6	0x0	0x0	0x0	0x0
AVGDONE	0xE7800	0x0	0x0	0xE7800
ALLDONE	0x0	0x0	0x0	0x0

Section: Time Pipeline

Seconds	0x3BAA5E41	0x3BAA5E41	0x3BAA5E41	0x3BAA5E41
Nsec				
Status	0x0	0x0	0x0	0x0

Section: Counters

Counters	All Counter Reset	TS Sync Error	1
Total	215771221	TS Pattern Sync Error	0
Rollover of Total	0	TS/Pattern Mismatch	0
Total (ISR) Writes	215739519	Sequence RAM Busy	0
Rollover of Writes	0	Seq RAM Mode Error	0
Invalid Waveform	0	Sequence RAM Active	31700
Timeouts	0	Seq Ram Lock Error	0
Write Error	0	Seq Ram Invalid Data	47382
ISR Overwrite	0	MPS State	TIMEOUT
Backward Time Err**	0	Total MPS Messages	0
NTP Error	0	Rollover of Above	0
Invalid MPS Data	215723845	MPS Timeout	0
Mod 720 Sync Error	0	MPS Invalid Message	0
Pulse ID Sync Error	0	MPS Unknown Msg	0
Pulse ID Rollover	1646	MPS Parse Error	0
NTP State	OK	MPS Invalid Time	0
		MPS Time Off-By-One	0

Section: Processing Time (us)

Processing Time (us)	Record Average	101	Fiducial Average	56
Record Maximum*	128848919		Fiducial Maximum*	865
Start Time Diff Min*	2689		MPS Time Diff Min*	30000
Start Time Diff Max*	58316		MPS Time Diff Max*	0
Rate (Hz)	360.0		MPS from Patt Min*	30000
* Since Reset	** Since Boot		MPS from Patt Max*	0

Modifier section is separated into 6 sections as MOD1, MOD2, ..., MOD6

MOD1 is the lowest 32 (0-31 bit) bit of the timing pattern which is for EVG internal usage.

MOD6 is the highest 32 (160-191 bit) bit of the timing pattern which is for MPS data (excluded by the pipeline)

MOD2-5 are for EVG event code



```

/* Bits in modifier 3 */
#define MOD3_IDX          2
#define POCKCEL_PERM     (0x00080000) /* Pockels cell permit */
#define TCAV0_PERM      (0x80000000) /* TCAV0 */
//CLTS Project MPS Modifier Bits to set rates to two destinations:
/* Masks defined for CLTS timing MPS communication */
#define RATE_MPS_HXR_119HZ (0x00000001) /* RATE_MPS_HXR_119HZ BITP 64 */
#define RATE_MPS_HXR_110HZ (0x00000002) /* RATE_MPS_HXR_110HZ BITP 65 */
#define RATE_MPS_HXR_90HZ  (0x00000004) /* RATE_MPS_HXR_90HZ  BITP 66 */
#define RATE_MPS_HXR_60HZ  (0x00000008) /* RATE_MPS_HXR_60HZ  BITP 67 */
#define RATE_MPS_HXR_30HZ  (0x00000010) /* RATE_MPS_HXR_30HZ  BITP 68 */
#define RATE_MPS_HXR_10HZ  (0x00000020) /* RATE_MPS_HXR_10HZ  BITP 69 */
#define RATE_MPS_HXR_05HZ  (0x00000080) /* RATE_MPS_HXR_05HZ  BITP 75 */
#define RATE_MPS_HXR_01HZ  (0x00001000) /* RATE_MPS_HXR_01HZ  BITP 76 */
#define RATE_MPS_SXR_119HZ (0x00002000) /* RATE_MPS_SXR_119HZ BITP 77 */
#define RATE_MPS_SXR_110HZ (0x00004000) /* RATE_MPS_SXR_110HZ BITP 78 */
#define RATE_MPS_SXR_90HZ  (0x00008000) /* RATE_MPS_SXR_90HZ  BITP 79 */
#define RATE_MPS_SXR_60HZ  (0x00020000) /* RATE_MPS_SXR_60HZ  BITP 81 */
#define RATE_MPS_SXR_30HZ  (0x00040000) /* RATE_MPS_SXR_30HZ  BITP 82 */
#define RATE_MPS_SXR_10HZ  (0x00100000) /* RATE_MPS_SXR_10HZ  BITP 84 */
#define RATE_MPS_SXR_05HZ  (0x00200000) /* RATE_MPS_SXR_05HZ  BITP 85 */
#define RATE_MPS_SXR_01HZ  (0x00400000) /* RATE_MPS_SXR_01HZ  BITP 86 */
#define BKRCUS             (0x00800000) /* BKRCUS scheduled by EVGUI BITP 87*/

```

Take "RATE\_MPS\_HXR\_05HZ" as example, (0x00000800), in hex, there are 32 bit for MOD3 section. Therefore,  $0x00000800 = 0000100000000000$ . Which is  $32 * 2 - 1 + 12 = 75$ ;  $32\text{bit} * (\text{MOD}\# - 1 (=2)) + \text{Section BITP}(0x00000800, \text{position } 12 \text{ in binary}) - 1(0-31, 32-63, 64-95, \dots) = \text{Modifier BITP}$

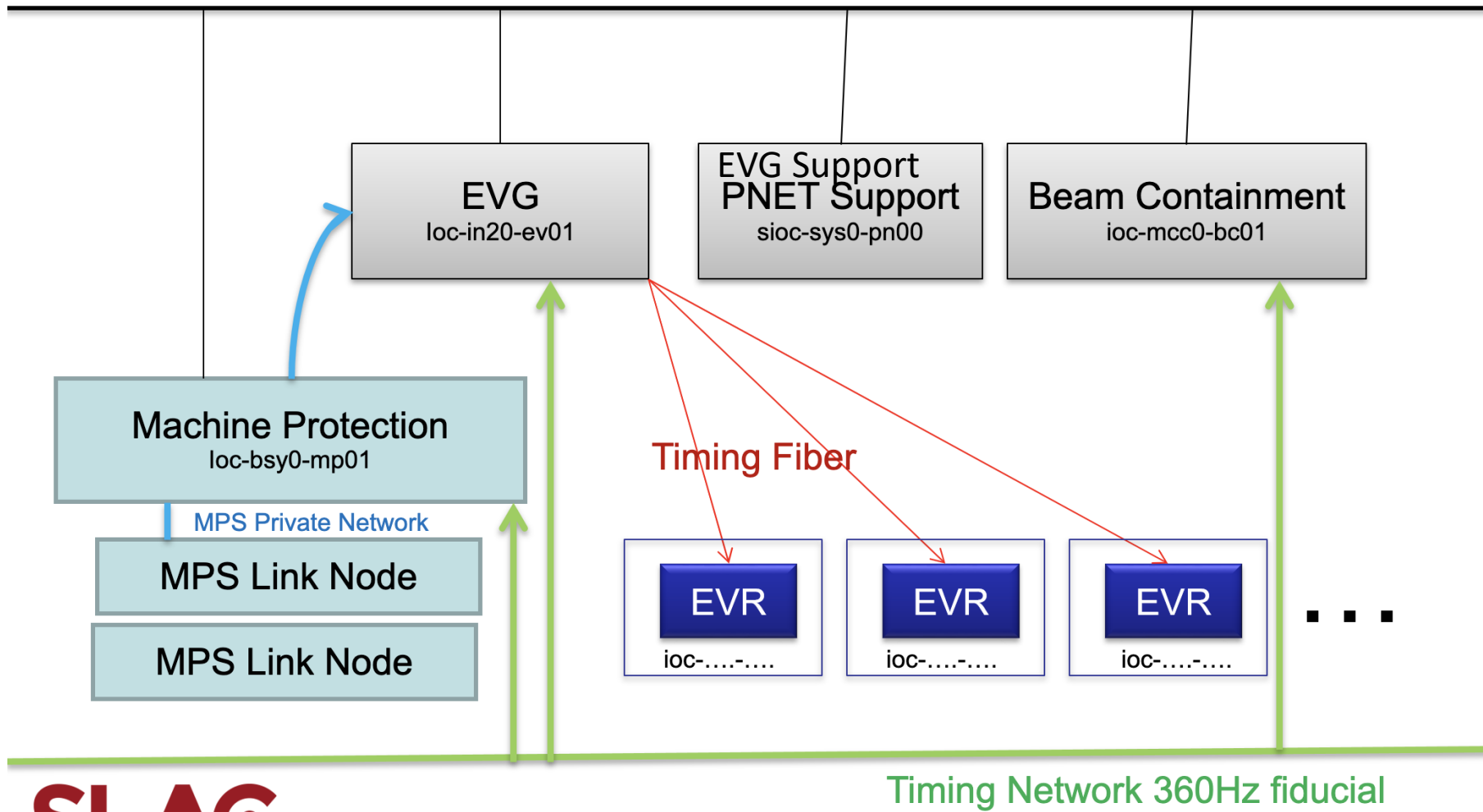
# EVG Note

- Modifier bit is 192 bit long that separated into 6 sections as MOD1-6
- Modifier bit repeat every 2 seconds as 720Hz
- Modifier bit is configurable
- Modifier bit and EVG event code both live in EVG
- Event code search from modifier bit for matching bit that fit the configuration of the event code
- Hence the event code could have its own frequency based on how often the matching condition shows up
- EVR receive the event code from EVG

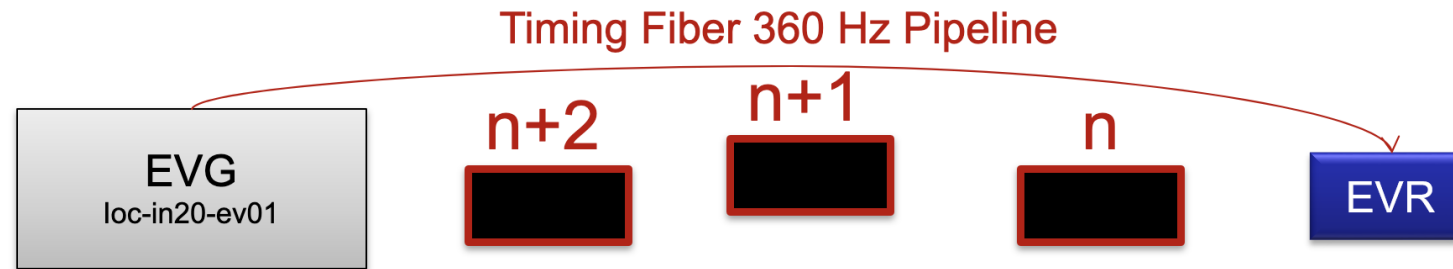
# Timing pattern change

- There are only three scenarios that change the timing pattern
  - MPS --> rate reduction
  - Manually shut off the beam
  - Hatch operator modify the pattern to lower the beam rate (kicker for rate reduction)
    - When changing pattern, the even code will change at the same time since the pattern got changed

# Channel Access



# What does EVG send to EVR?

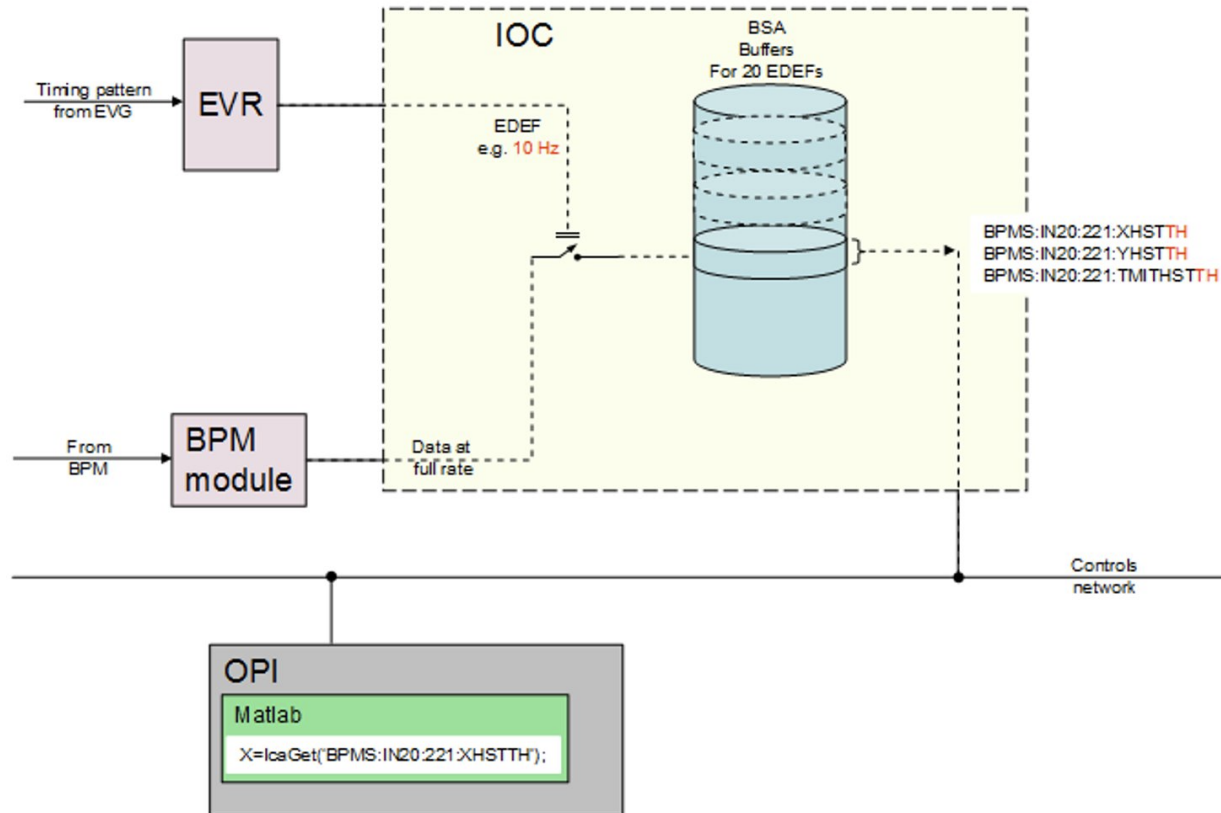


EVR receive three timing frame from EVG as called "**pipeline**". As EVR can see the next three timing frame from the pipeline, EVR can start preparation of the device so it can match up the time when there is a beam

Event Codes [0..255]  
Time Stamp w/Pulse Id  
192 Modifier Bits

For example, EVR can see  $n$ ,  $n+1$  and  $n+2$ . EVR knows the device ready time is two timing frame, once EVR sees  $n+2$  is with beam and need the device to activate, at  $n$  it will start the preparation so when  $n+2$  arrive it can perform in time.

# BSA (Beam Synchronous Acquisition)



# How to access NC EVG

From *physics* account on Prod (lcls-srv01):

Reserve an *EDEF* with *lclshome* -> NC Gun -> Event / NC Global

For further detail of EVG EDEF, see slide Cu-BSA.pptx

Source:  NC Gun  SC Gun Destination: HXR SXR

Applications: Operator Tools, Physics Apps, Global Displays

LCLS Subsystems and Areas: Global Event / Timing System

Global IN20 LI21 LI22 LI23 LI24 LI25 LI26 LI27 LI28 LI29 LI30 BSY LTUH LTUS UNDH UNDS DMPH DMPS FEEH FEES NEH XRT FEH

Event Generator (EVG) IOC: Diagnostics..., Events..., Magic Decoder...

EVG IOC Status: Pattern/PNET, NTP, MPS Interface, Master Beam Control...

Beam Synchronous Acquisition: Event Definitions...

VMTG/Main Drive Line: VMTG..., Beam Rate Control...

EVG in IN20: Beam Rate Control...

Profile Monitor: Dark Current Diags (On)

MPS Rates: Pockels Cell (0.0), Mech Shutter (0.0), BYKIK (0.0), BYKIKS (0.0), Laser Htr Shutter (0.0)

MPS Control: Mitigation Control..., Burst Control...

CAMAC Timing: PDU Global Rules...

LCLS Rates (Hz): Beam Full Rate (120.0), Pockels Cell (120.0), Klys Accelerate (120.0), Klys Accel & 10 Hz (10.0), BYKIKS (0.0), TCAV0 (10.0), TCAV3 (0.0), Burst (0.0), BPM Calibration 1 (120.0), BPM Calibration 2 (120.0), Toroid Calibration (120.0), Profile Monitors (10.0), TCAV3 OTR (0.0), Klystron Standby (120.0), Klys Stdbly & No TCAV0 (110.0), Klys Stdbly & No TCAV3 (120.0), Pulse Picker (0.0)

Base Rate Triggers: TS4 and TS1 120 Hz (120.0), TS4 60 Hz (60.0), TS4 30 Hz (30.0), TS4 10 Hz (10.0), TS4 5 Hz (5.0), TS4 1 Hz (1.0), TS4 0.5 Hz (0.5), Fiducial (360.0)

Abort Triggers: BYKIK Abort (Enable), BYKIKS Abort (Enable), Abort beam at BYKIK every (37) beam shots, Abort beam at BYKIKS every (11) beam shots

Trigger Control: BYKIKS Burst (Off), BYKIK Burst (Off), Kick on TCAV3 (On), Control (Burst), Rate (Full), Number of Pulses (10), Num Pulses So Far (0)

NC\_HARD\_INJ (120.0), NC\_HARD (120.0), NC\_SOFT\_INJ (0.0), NC\_SOFT (0.0), Desired Beam Rate Mode (HXR 120 / SXR 0), Actual Beam Rate Mode (HXR 120 / SXR 0)

PRODUCTION evnt\_all\_main.edi 09/08/2021 16:25:29

# EVG note when reboot

LCLS Subsystems and Areas: Global Event / Timing System

Global IN20 LI21 LI22 LI23 LI24 LI25 LI26 LI27 LI28 LI29 LI30 BSY LTUH **LTUS** UNDH UNDS DMPH DMPS FEEH FEES NEH XRT FEH

Event Generator (EVG) IOC: Diagnostics... Events... Magic Decoder...

EVG IOC Status: Pattern/PNET OK, NTP OK, MPS Interface OK, Master Beam Control...

Beam Synchronous Acquisition: Event Definitions... **VMTG/Main Drive Line VMTG...**

Profile Monitor: Dark Current Diags On

PS Rates: Pockels Cell 0.00, High Shutter 0.00, BYKIK 0.00

LCLS Rates (Hz): Beam Full Rate 120.0, Pockels Cell 120.0, Klys Accelerate 120.0, Klys Accel & 10 Hz 10.0, BYKIKS 0.0, BYKIK 0.0, TCAV0 10.0, TCAV3 0.0, Burst 0.0

BPM Calibration 1 120.0, BPM Calibration 2 120.0, Toroid Calibration 120.0, Profile Monitors 10.0, TCAV3 OTR 0.0, Klystron Standby 120.0, Klys Stdby & No TCAV0 110.0, Klys Stdby & No TCAV3 120.0, Pulse Picker 0.0

Base Rate Triggers: TS4 and TS1 120 Hz 120.0, TS4 60 Hz 60.0, TS4 30 Hz 30.0, TS4 10 Hz 10.0, TS4 5 Hz 5.0, TS4 1 Hz 1.0, TS4 0.5 Hz 0.5, Fiducial 360.0

Abort Triggers: BYKIK Abort, BYKIKS Abort, Disable/Enable buttons

Trigger Control: BYKIKS Burst, BYKIK Control, Rate, Number of Pulses, Num Pulses So Far

Desired Beam Rate Mode: HXR 120 / SXR 00

Actual Beam Rate Mode: HXR 120 / SXR 00

PRODUCTION evnt\_all\_main.edl

Master Trigger Generator - Main (/usr/local/lcls/tools/edm/display/event/VMTG\_top.edl on lcls-srv01)

Help... Home Screen... Exit

Parameter	Value
<b>VMTG S10 Master Trig Freq</b>	360.752 Hz
<b>VMTG S10 IRQ Input Freq</b>	N/A
<b>VMTG S10 TS0 Freq</b>	N/A
<b>VMTG S10 Sync Frequency</b>	0.07 MHz
<b>VMTG S10 RF Power</b>	-22.158 dBm
<b>VMTG S10 Temperature</b>	62.290 F
<b>Global</b>	(Visual indicator: 3 green bars)
<b>VMTG S20 Master Trig Freq</b>	N/A
<b>VMTG S20 IRQ Input Freq</b>	358.939 Hz
<b>VMTG S20 TS0 Freq</b>	60.006 Hz
<b>VMTG S20 RF Power</b>	-59.637 dBm
<b>VMTG S20 Temperature</b>	62.345 F



**Master Trigger Generator - Main**

Help... Home Screen...

<b>VMTG S10</b>	<b>Global</b>	<b>VMTG S20</b>
Master Trig Freq: 362.582 Hz	[Green Bar]	Master Trig Freq: [Grey Bar]
IRQ Input Freq: N/A	[Green Bar]	IRQ Input Freq: [Grey Bar]
TS0 Freq: N/A	[Green Bar]	TS0 Freq: [Grey Bar]
Sync Frequency: 0.07 MHz		
<b>ADC Data</b>		<b>ADC Data</b>
RF Power: -22.161 dBm		RF Power: [Grey Bar]
Temperature: 62.538 F		Temperature: [Grey Bar]

Expert... Info... Expert...

Diagnostics  
Registers

**Master Trigger Generator - Registers (on lcls-srv01)**

/usr/local/lcls/tools/edm/display/event/VMTG\_SyncSel.edl (on lcls-srv01)

Help... Home Screen... Exit

**Master Trigger Generator - Synchronization Clock Select Control**

Home Screen... Exit

Sync Frequency: 0.07 MHz | 8.5MHz | **71.43KHz**

**Make sure 71.43KHz is selected**

SC Filt CLK1: 0xa6	0xA6	Master Trig Delay: 0	0x0
SC Filt CLK0: 0xa6	0xA6	External Trig Dly Prescale: 0	0x0
SC Filt Ctrl: 0xe8bd	0xEF8D	External Trig Delay: 0	0x0
Bd/GW Vers: [Grey Bar]	0x150	MTG Out Fine Delay: 0	0x0
Int Ctrl: [Grey Bar]	0x0	Interrupt Src Dly Prescale: 0x50	0x50
Int Status: [Grey Bar]	0x0	Interrupt Source Delay: 0x23a	0x23A
Int Vector: [Grey Bar]	0x0	TS0 Delay Prescale: 0x50	0x50
CSR2: 0x8000	0x888F	TS0 Delay: 0	0x0
CSR1: 0x8001	0x8011	TS0 Width Prescale: 0x4	0x4
CSR0: 0x140c	0x140C	TS0 Width: 0x8980	0x8980

Sync Clock Select

Signal Monitor Controls

Read-back: 0xECFC, 0x0, 0x0

# SC Timing

# SC Timing

- SC BSA provides data buffers time stamped by the SC Timing System (Timing Pattern Generator – TPG ).
- SC BSA provides data filtering according to user needs.
- SC BSA provides pulse-by-pulse data buffers up to 1KHz.
  - Maximum of 20000 data points.
  - Each data point can be an average of up to 1000 beam pulses
  - Maximum rate of 1KHz
- Difference NC BSA:
  - It is not a scaler acquisition
  - The acquisition cannot be run at beam rate but only up to 1KHz

- Timing Pattern Generator (TPG) sends Timing Frames to each Timing Pattern Receiver (TPR) over a dedicated fiber network at 1MHz.
- PVs that participate in SC BSA have Pulse Id encoded into the nanoseconds part of their time stamp.

- An IOC is equipped with an TPR.
- Timing Fiber is run from TPG, most likely through a Fanout module.
- Special software is installed in the IOC that knows how to talk to the TPR.
- Assuming the requested signals can be read out within 1/120th sec from the hardware, EPICS Databases are created for the SC BSA PV.

# How to access SC TPG?

For further detail of TPG BSA, see slide "SC-BSA.pptx"

From *physics* account on Prod (lcls-srv01):

Reserve an *BSA* with *lclshome* -> SC Gun -> Event / SC Global

The screenshot displays the SC TPG control interface. At the top, the 'Source' is set to 'SC Gun' (highlighted with a red box) and the 'Destination' is set to 'DIAG0'. Below this is a routing matrix with 'All' as the source and various destinations as columns. The 'Event' row is highlighted with a red box. An 'SC Timing Display' panel is overlaid on the right, showing a table of parameters for various destinations.

Destination:	SC1 Laser	SC1 Gun	SC1TDINJ	SC1 DIAG0	SC1 DumpBSY	SC1 TDUNDHXR	SC1 TDUNDSXR	SC1 DUMPHXR	SC1 DUMPSXR	SC1 S30XL	DST11	DST12	DST13	DST14	DST15
Destination Rate:	10	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Actual Rate:	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel	PyOMLabel
MPS Beam Class RBV:	0	0	0	10	0	0	0	0	0	0	0	0	0	0	0
Timing Beam Class set PV:	1	5	0	5	5	0	0	0	0	1	0	0	1	1	1
Timing Beam Class RBV:	1	5	0	5	5	0	0	0	0	1	0	0	0	0	0
Charge PV:	PyOMLabel														

The 'SC Timing Display' panel also includes a 'Pattern Select' section with 'Select Destination' set to 'SC1 DIAG0' and 'Pattern' set to '1000b\_1'. It features 'Load' and 'Apply' buttons. Below this is a table for fault monitoring:

	BCS Fault	MPS Fault
FLT Buf 0:	0	0
FLT Buf 1:	0	0
FLT Buf 2:	0	0
FLT Buf 3:	0	0

On the right side of the panel, there is a 'MPS Link Diagnostics' section with the following status:

- Physical Link Rx: Fault
- Physical Link Tx: Ready
- Local Link: Fault
- Remote Link: Fault
- Rx Clock Frequency: 250000200

A 'BSA Summary' button is located at the bottom right of the panel.

- MPS issues permits for each destination
- Cu MPS permits are Rate based, max 120 Hz
- Each "mitigation device" (destination) has a maximum rate permit PV published as an enum *and* as a double. Note these are PERMITs, not actual rates
- SC MPS permits are Beam Class based
- Beam classes are defined as (1) integrated charge in (2) time window with some (3) minimum bunch spacing
- Each destination will publish the current beam class PERMIT as an enum and three PVs to provide the three parameters that define a beam class
- In both cases, timing system will publish the actual rate to a destination

## Sc Timing pattern frame:

- Time
- PulseID
- Destination
- Fixed Rates
- AC Rates
- Beam Request
- Requested Charge
- MPS Valid
- BCS Fault
- MPS Limiting
- MPS Limits
- BSA fields ( Init; Active;  
AvgDone; Update)

## Cu Timing pattern frame:

- Time
- PulseID
- Beam Code (BC)  
(0=Any, 1=Cu to HXR, 2= Cu to SXR –see next slide)
- Event Codes
- Modifier bits: time slot;  
kicker trigger mask presence;  
beam presence; subset of  
lower rate trigger mask  
per destination; etc..
- BSA fields

Note: The information is packaged / called a little bit different, but it is similar concept.



# BSA and TPG

- TPG generate timing pattern where BSA acquire along with other device signals (MPS, BPM etc..) or signal (PID, TS, etc..)
- As the result BSA generate PV record with device signal and TPG signal

- Ex, TPG:SYS0:1:TSPIDHST21

Device name or  
Signal name

BSA data that  
acquire with the  
device signal



# Note

- LCLS1:0...120Hz
- LCLS2:0...1MHz
  - **PDU = Programmable Delay Unit**
- The PDU is where timing and pattern information meets the fiducial and the 8.4 ns clock from the FIDO and triggers with appropriate delays are output on the CAMAC upper backplane.
- PDU outputs 16 triggers of 67.2 ns width at ECL levels (~-0.8V to 1.8V)

# Troubleshoot for LCLS EVG

```
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
pnetSeqCheck2: Unexpected time slot, EVG = 2, EVG = 6
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x2
pnetSeqCheck1: Unexpected time slot pattern, EVG = 0x1, EVG = 0x20
```



The error shown the wall wart is still on with generator or regular power supply without the wall wart

# Q&A

- Why the signal needs to be amplified at sector 30 since only 30 sectors exist
- 3pf