LINAC Locking Review

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Outline

- Overview
- Requirements
- Scope
- Design
  - Hardware
  - Software
- Installation
  - Status
- Documentation
  - ESD Update
  - Checkout procedures
- Operations/Procedures
  - What to do when …

Overview

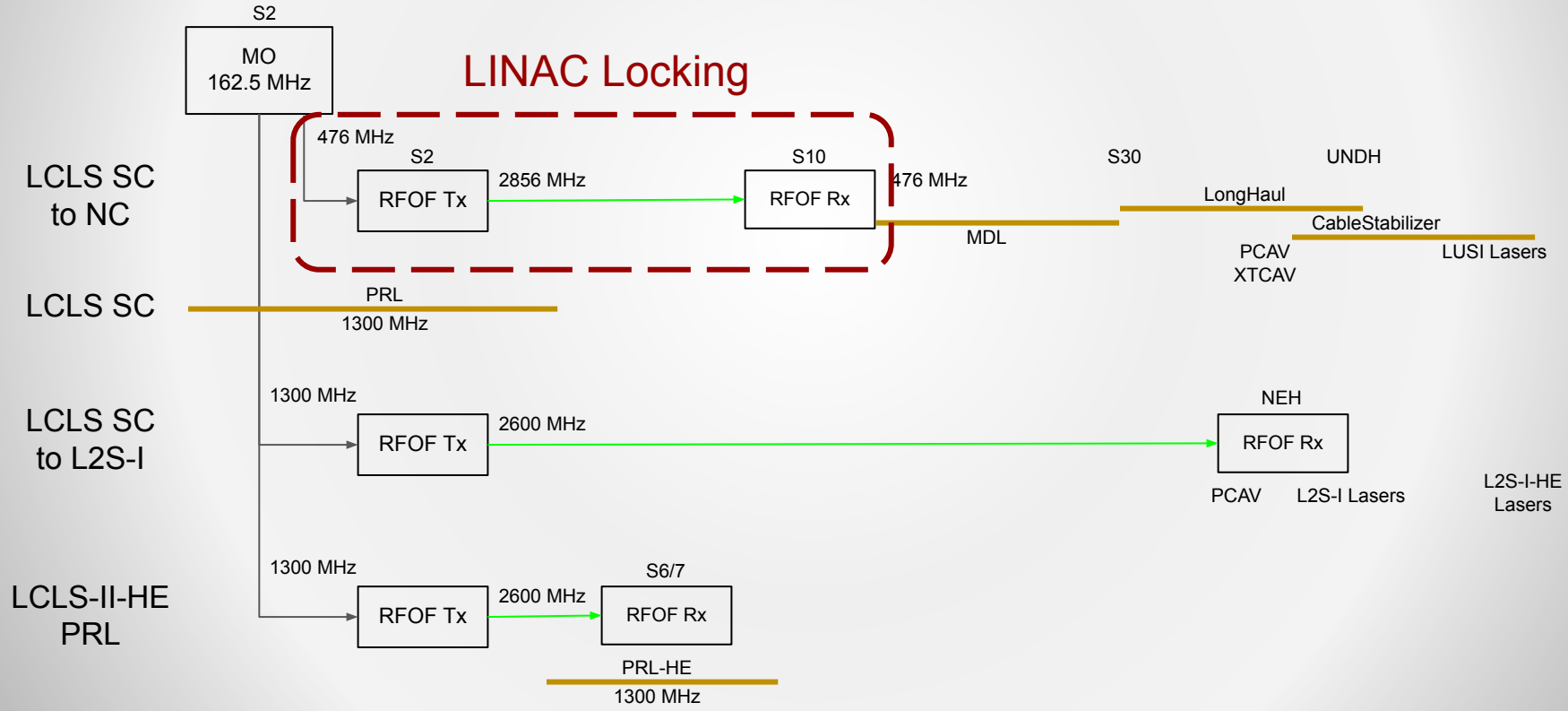
1) Several systems are built for LCLS-I reference frequencies, but we'd like to use them with the LCLS-II beam.

   XTCAV, STCAV, possibly experiment laser systems

2) Tender X-ray Instrument will want beam from both LINACs with some control over relative timing.

   Distributing 476 MHz locked to LCLS-II makes this possible.

RF Distribution Systems



Requirements

Generate 476 MHz RF reference in S2 for use with STCAV
- Similar jitter characteristics as MO
- RF transport to STCAV (S1) is in the STCAV project

Transmit 476 MHz reference to S10 to replace 476 MHz MO.
- Similar jitter characteristics as existing MO

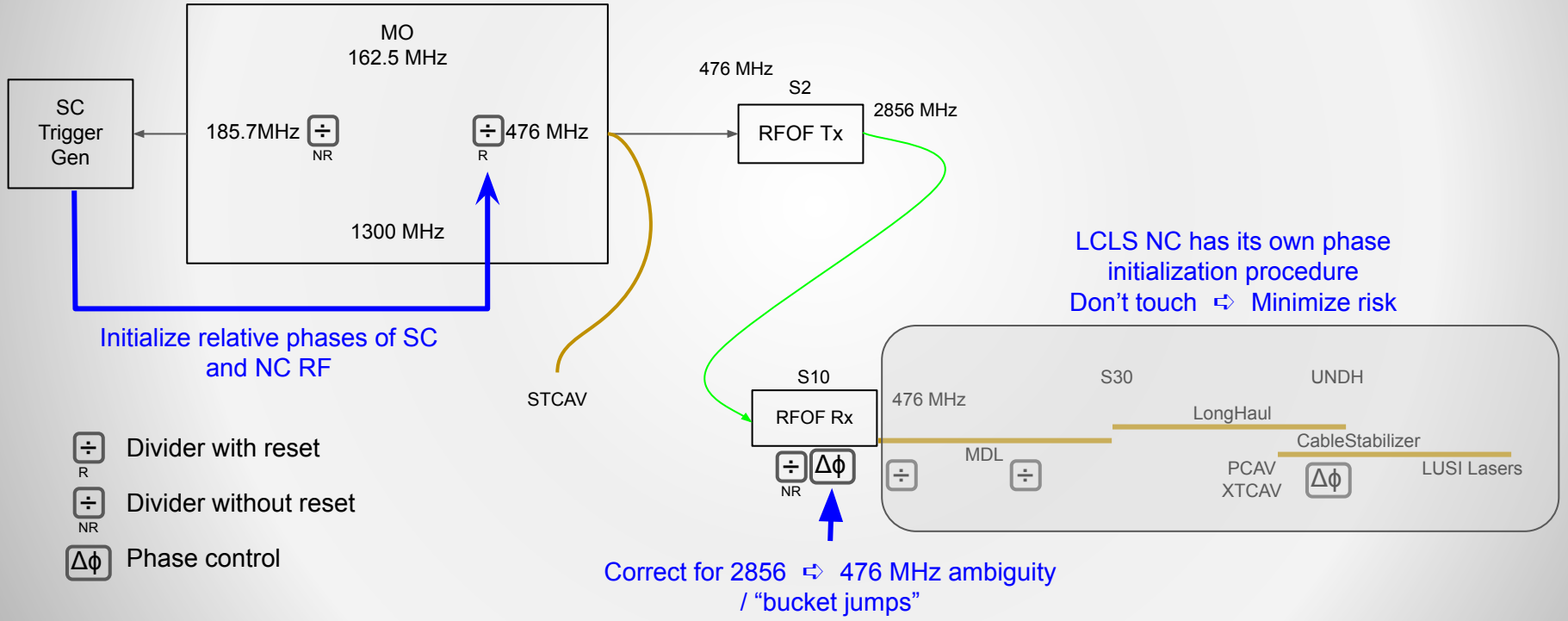
Align the triggering of SC/NC Timing Systems for XTCAV 120 Hz operation

Deferred: Merge the NC event timing onto SC event timing for TXI operation
- Triggering from SC timing will capture NC meta data

Scope

- Hardware
  - Sector 2
    - Chassis and Triggers for 476 MHz synthesis
    - RF conversion and RF over Fiber transmitter
  - Sector 10
    - RF over Fiber receiver
    - 476 MHz recovery and phase adjustment
  - Sector 20
    - Relative NC/SC timing measurement
- Software
  - IOCs for hardware control and monitoring
  - HLA
  - Displays
- Documentation
  - ESD Updates, Checkout Procedures

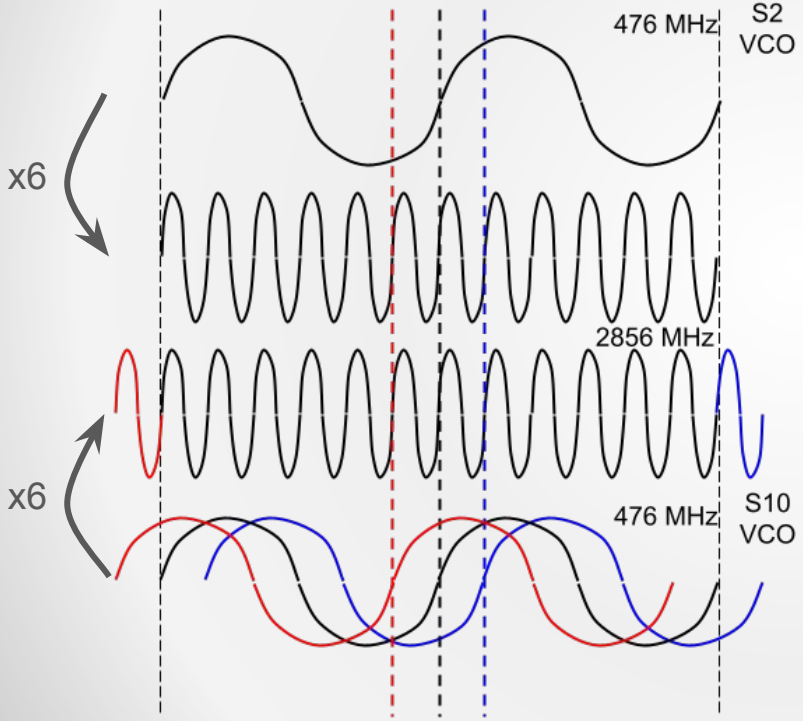
Design Overview



Design: Hardware

[Bo Hong]

Design: Phase Ambiguities and Bucket Jumps



2856 MHz from Sector 10 is locked to 2856 MHz from Sector 2, but that doesn't force the 476 MHz signals to have a known phase relationship.

There is a 6-fold ambiguity (3 shown).

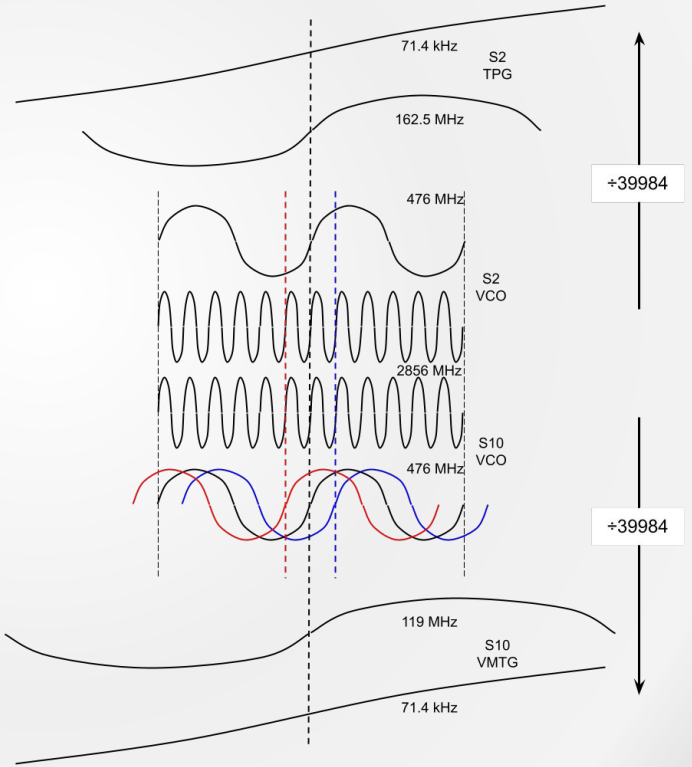
Laser lockers have a similar problem but more like a 40-fold ambiguity.

Design: Fiducial Alignment

VMTG injects fiducials at 360 Hz based on power line sampling it does at 119MHz / 1666 = 71 kHz

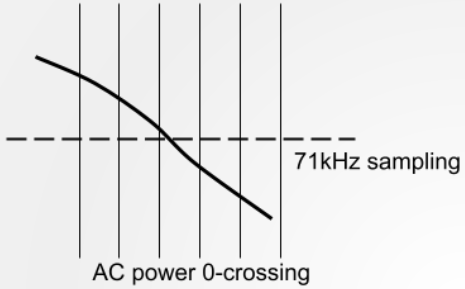
We want NC and SC timing to align 71kHz, so they can coordinate beam generation.

Either design a way to reset/trigger VMTG 71kHz prescale or slide the RF buckets until they align.



Design: Where do we find the 71 kHz references?

LCLS NC Timing



The LCLS VMTG samples the AC power line at the 71kHz subharmonic of its RF input.

Every 360 Hz fiducial is coincident with the 71kHz subharmonic.

LCLS SC Timing

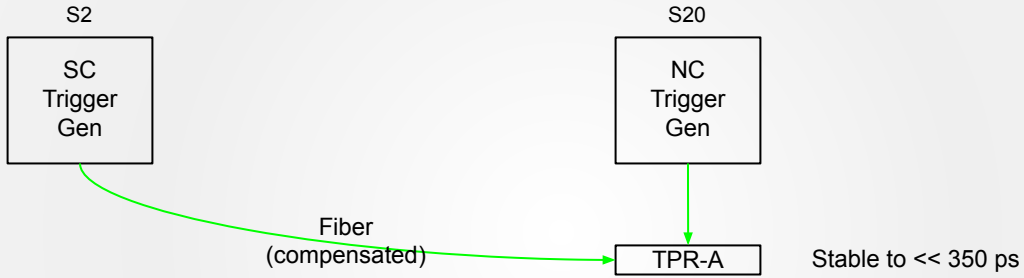
Table 4. Fixed rate markers

Fixed Rate	1300 MHz Prescale
1 Hz (actually 0.92857Hz)	1,400,000,000
10 Hz	140,000,000
100 Hz	14,000,000
1 kHz	1,400,000
10 kHz	140,000
71.43 kHz	18,200
half-rate	2,800 (nominal)
full-rate	1,400 (nominal)

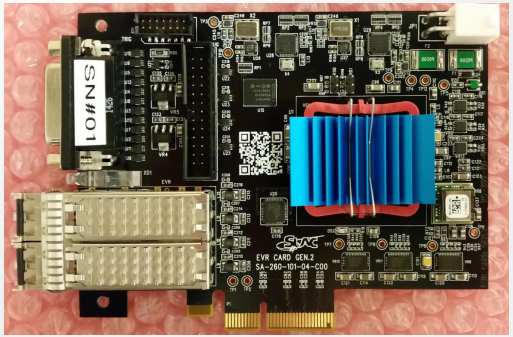
Both timing systems distribute their 71kHz subharmonic

Design: Trigger Alignment

71kHz alignment



We usually only use these boards to process one timing system or another, but the hardware is capable of processing both simultaneously. Added special firmware to receive both and measure relative delay of 71kHz NC vs SC.



Design: 1Hz, 60Hz, 360Hz Alignment

- NC timing designates 1 Hz fiducials internally (EVG)
- We can trigger the SC timing system to follow the NC timing.
  - TPG front panel has 3 TTL inputs for external triggers
  - Firmware is already running that can
    - Interpret those TTL signals for 1Hz, 60Hz, 360Hz, or
    - Sample the power line to generate independent fiducials
  - Connect NC timing to a TTL trigger board in cpu-sys0-sp01
- When NC timing is down, SC timing must generate its own 1Hz, 60Hz, 360 Hz fiducials (as it does now).

Design: Software

- 11.5 MHz PLL/VCO Control
- 476 MHz PLL/VCO Control
- Resynch Trigger Control
- Libera Sync RFoF Control
- 2856 MHz PLL/VCO Control
- Trigger Alignment Monitoring
- RF Phase Control HLA

11.5 MHz Phase Locked Loop Control

Sioc-sys0-ms07

- Part of the master source application
- Runs on cpu-sys0-sp01 (L2KG02-24)
- A copy of the existing PRL IOCs for 1300 MHz PLL control, except there is no remote slave unit here.
- Mostly monitoring, control loop is in firmware
- PVs described here https://confluence.slac.stanford.edu/display/~khkim/PV+name+for++LCLS2+Master+Source
- Reviewed by naming Czars
- Deployed

11.5 MHz Phase Locked Loop Control Display

Most important

476 MHz Phase Locked Loop Control

Sioc-sys0-ms08

- Part of the master source application
- Runs on cpu-sys0-sp01 (L2KG02-24)
- A copy of the existing PRL IOCs for 1300 MHz PLL control, except there is no remote slave unit here.
- Mostly monitoring, control loop is in firmware
- PVs described here https://confluence.slac.stanford.edu/display/~khkim/PV+name+for++LCLS2+Master+Source
- Reviewed by naming Czars
- Deployed

Resynch Trigger Control

Sioc-sys0-ms09

- Part of the master source application
- Runs on cpu-sys0-sp01 (L2KG02-24)
- The generic PCIe TPR trigger control IOC
- Uses the TprTrigger and TprPattern modules and PVs
- Generates 3 TTL triggers at 71 kHz
- No timestamping, no BSA
- Not deployed

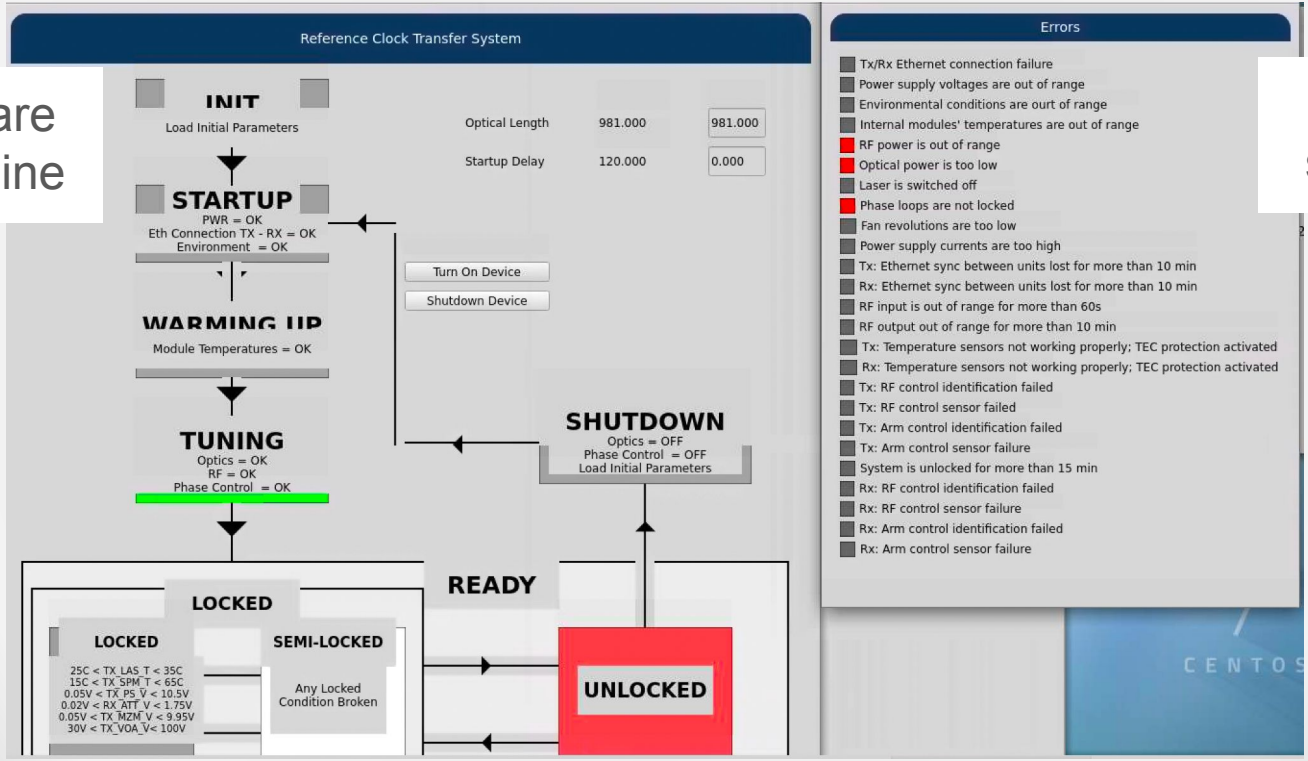
RFoF Telnet IOC

Sioc-sys0-ms11

- Part of the master source application
- Runs on cpu-sys0-sp02 (LKG10-27)
- Maps vendor telnet commands to PVs for monitoring
- PVs described here https://confluence.slac.stanford.edu/display/~skoufis/Linac+Locking+-+RFoF+Telnet+IOC+%28sioc-sys0-ms11%29+PVs
- Reviewed by naming Czars
- Deployed

RFoF Telnet IOC Display

The firmware state machine



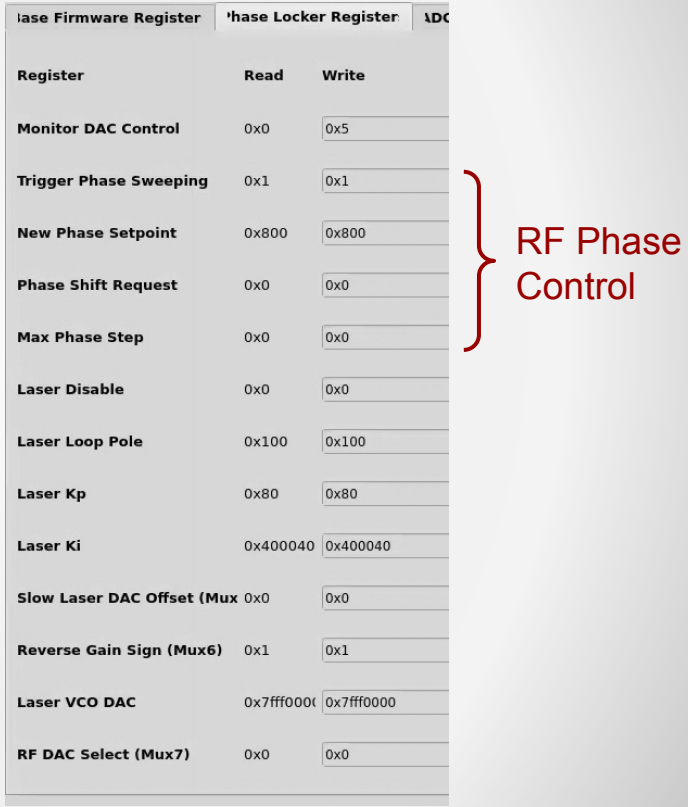
Error summary

Phase Locker IOC (2856 MHz)

Sioc-sys0-ms10

- Part of the master source application
- Runs on cpu-sys0-sp02 (LKG10-27)
- Derived from the Laser Locker IOCs
- PVs described here https://confluence.slac.stanford.edu/display/~skoufis/Linac+Locking+-+Phase+Locker+IOC+%28sioc-sys0-ms10%29+PVs
- Reviewed by naming Czars
- Deployed

Phase Locker IOC Display



Trigger Alignment IOC

Sioc-sys0-ms12

- Part of the master source application
- Runs on cpu-sys0-sp02 (LKG10-27)
- Reads PCIe to PVs for monitoring
- PVs described here https://confluence.slac.stanford.edu/display/~skoufis/Linac+Locking+-+Trigger+Alignment+IOC+%28sioc-sys0-ms12%29+PVs
- Reviewed by naming Czars
- Not deployed

Trigger Alignment IOC PVs

PV Name	Descr	Value
$(DEVICE):CU_LINK_UP	NC timing link up	1
$(DEVICE):CU_FID_CNT		
$(DEVICE):CU_ERR_CNT		
$(DEVICE):CU_INTV_ERR_CN		
$(DEVICE):CU_CLK_FREQ		
$(DEVICE):CU_REF_CNT		

PV Name	Descr	Value
$(DEVICE):SC_LINK_UP	SC timing link up	1
$(DEVICE):SC_FID_CNT	SC timing fiducial count	Incrementing at 929kHz
$(DEVICE):SC_ERR_CNT	SC timing error count	Not incrementing
$(DEVICE):SC_INTV_ERR_		
$(DEVICE):SC_CLK_FREQ		
$(DEVICE):SC_REF_CNT		

PV Name	Descr	Value
$(DEVICE):TMO_CNT	Measurement timeout count	Not incrementing
$(DEVICE):DIFF_CLOCKS	Timing reference difference, 119 MHz clocks	0 – 1665, Not changing
$(DEVICE):PHAS_DIFF	Timing reference difference, ps	0 – 14e6, updating at 1Hz, few ps jitter

Phase Controller HLA

- Monitor Trigger Alignment IOC output
  - Receive measured relative NC/SC RF timing
- Set Phase Locker IOC “PHAS_SETPT”
  - Initialize relative NC/SC RF timing to a known value in 2856 MHz buckets
  - Monitor for bucket jumps and correct
  - Fine tuning for NC/SC relative beam timing [simultaneous delivery]
    What can measure relative beam timing?
    - XTCAV - depends on cavity RF matching, limited time range
    - PCAV - depends on cavity timing match, greater range, more drift
    - Photon instruments?
- Defer initial deployment and study in MD

LCLS Home Displays

[Ryan McClanahan]

Installation Status

Units	Hardware Installed	IOC Deployed	Checkout Complete
Resync triggers	yes	no*	no*
11.5 MHz PLL	yes	yes	yes
476 MHz PLL	yes	yes	yes
Libera Sync RFoF	yes	yes	no**
S10 476 MHz VCO	yes	-	no
2856 MHz PLL	yes	yes	no
Trigger Alignment	no	no	no

Installation was paused to estimate and complete a plan for TTO.

TTO Planning

Hardware
Coordination
Drawings
Update rack profile (s2, s10, s20)
Update CAPTAR and labels on cables
Update drawing
Shadow the experts to learn failure/recovery of the system
RFoF Checkout
Terminate and connect fibers
RFoF Checkout
2856 MHz PLL Checkout
2856 MHz PLL Checkout
476 MHz VCO Checkout
476 MO Switchover
Trigger alignment card (TPR) install and checkout s20
Checkout procedure documentation
Checkout procedure review and signoff
LCLS-II Timing System ESD Revision
ESD review and signoff
Software Tasks
RFoF IOC
Deploy latest software release, ensure IOC boots up fine, verify that Asyn trace logging is under control and that Tx/Rx are reachable through the network.
Clean up: ALARMS, archive..etc

PHASE LOCKER IOC
Clean up: ALARMS, archive..etc
Deploy latest software release, ensure IOC boots up fine.
PLL IOCs
Fix the multiple CPSW errors that we get. Do we need to replace the firmware?
Clean up: ALARMS, archive..etc
Deploy the latest software release, ensure both IOCs boot up fine.
Test locking functionality for both the 11.5MHz and 476MHz modules.
PCIeTPR IOC
Debug, troubleshoot, test in Dev.
Clean up: ALARMS, archive..etc
Deploy into production.
Test in production.
TRIGGER ALIGNMENT IOC
Review Asyn driver implementation.
Review/Revise PVs, get approval from naming team.
Clean up: ALARMS, archive..etc
Test IOC and firmware in Dev.
Create CATER software job for the IOC deployment into production.
Deploy App and IOC into Production.
Test IOC in Production.

CATER JOBS
Revise the Test Plan section for the PLL software jobs.
Revise the Risk/Benefit sections for all software jobs.
Revise CATERs with EED
DISPLAYS
PYDM displays
DOCUMENTATION
README files for all 6 IOCs.
PEER Review
Preparation slides capturing ESD content
Review
EPICS IOC rework
Active Fanout
Active Fanout Intialization Settings

Documentation

- Rack Profiles
- CAPTAR
- Drawings
- ESD
- Checkout Procedures
- Online Guidance

Rack Profiles

- L2KG02-24
  - No change
- L2KG02-25
  - No Change
- L2KG02-27
  - Owned by PCDS. Have an updated profile to submit.
- LKG10-27
  - 2856 MHz PLL (TBD)
- LKG10-28
  - 476 MHz VCO and RFoF (TBD)
- LKG-21
  - Trigger Alignment Host CPU (TBD)

CAPTAR

- Sector 2 RF cabling to L2KG02-27 (TBD)
- Sector 2 - 10 Optical fiber cabling
- Sector 10 RF cabling
- Sector 21 cpu-li20-sp01 cabling. Ethernet. (TBD)

CAPTAR: Sector 10 RF and optical fiber cabling

system = 'LINAC LOCKING'

#	dwgnum	system	func	jobnum	cabletype	cablenum	origin	loc	rack	ele	side	slot	connnum	pinlist	station	conntype	length	routing
1		LINAC LOCKING	CONTROL VOLTAGE FOR VCO	LLRF01	RG58	LI13949	LKG10-2820--DAC OUT-	LKG10	28	20			DAC OUT			SMA	25	IC:
2							LKG10-2727--V TUNE-	LKG10	27	27			V TUNE			SMA		
3		LINAC LOCKING	476 REFERENCE	LLRF01	RF-CBL25F	LI13950	LKG10-2820--RF IN 2-	LKG10	28	20			RF IN 2			SMA	25	IC:
4							LKG10-2719--RF OUT 2-	LKG10	27	19			RF OUT 2			SMA		
5		LINAC LOCKING	2856 REFERNCE	LLRF01	1/4HEL	LI13951	LKG10-2820--RF IN 1-	LKG10	28	20			RF IN 1			SMA	25	IC:
6							LKG10-2727--RF OUT 1-	LKG10	27	27			RF OUT 1			SMA		

system = 'RFOF:SYS0:MS01'

#	dwgnum	system	func	jobnum	cabletype	cablenum	origin	loc	rack	ele	side	slot	connnum	pinlist	station	conntype	length	
1		RFOF:SYS0:MS01	LOW DRIFT OPTICAL LOW TCD	XTTIM1	FIOPLTC	XT00113	L2KG02-2724--Low Drift-	L2KG02	27	24	B		Low Drift			SC-APC	3218	IC: TC
2							LKG10-2732--Low Drift-	LKG10	27	32	B		Low Drift			SC-APC		
3		RFOF:SYS0:MS01	LOW NOISE OPTICAL LOW TCD	XTTIM1	FIOPLTC	XT00114	L2KG02-2724--Low Noise-	L2KG02	27	24	B		Low Noise			SC-APC	3218	IC: TC
4							LKG10-2732--Low Noise-	LKG10	27	32	B		Low Noise			SC-APC		
5		RFOF:SYS0:MS01	OPTICAL SPARE LOW TCD	XTTIM1	FIOPLTC	XT00115	L2KG02-2724--X-	L2KG02	27	24	B		X			SC-APC	3218	IC: TC
6							LKG10-2732--X-	LKG10	27	32	B		X			SC-APC		
7		RFOF:SYS0:MS01	LOW DRIFT OPTICAL	XTTIM1	FIBOPT06	XT00116	L2KG02-2724--X-	L2KG02	27	24	B		X			SC-APC	3218	IC: TC
8							LKG10-2732--X-	LKG10	27	32	B		X			SC-APC		

Drawings

- Amend LCLS2 master source drawing for Sector 2
- Add new LCLS2 master source drawing for Sector 10
- Amend LCLS2 timing system drawing for Sector 2 and Sector 20

Upload to Team Center

All TBD

LCLS2 Timing System ESD Update/Revision

- Updated to represent as-built.
- Describes LINAC Locking additions.
  - Hardware mostly
  - Software descriptions still TBD
- To be reviewed

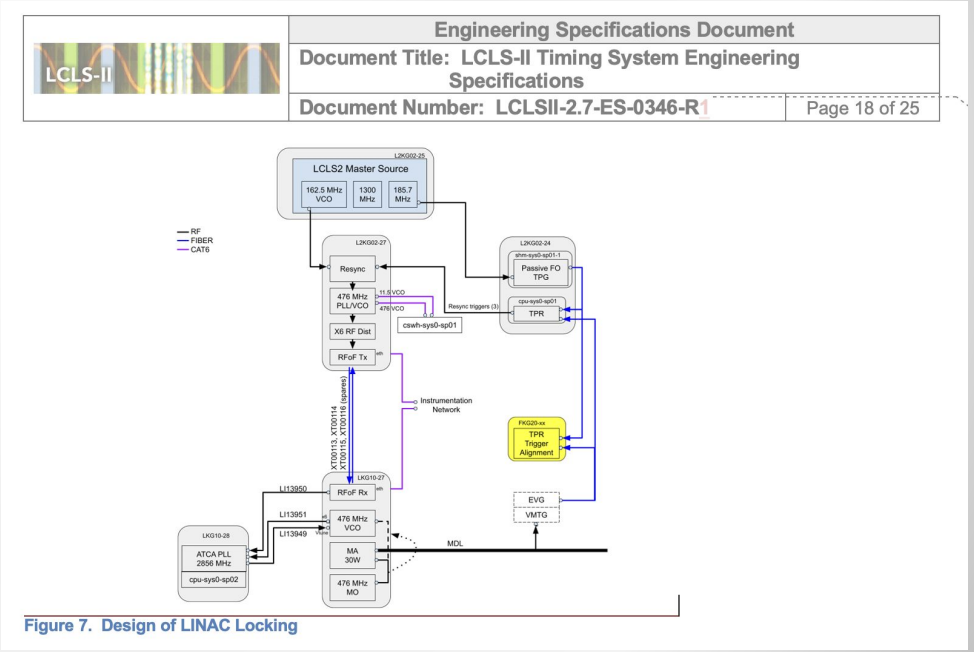


Figure 7. Design of LINAC Locking

LCLS2 Master Source Checkout Procedures

- Checkout procedures updated for the added systems.
  - Sector 2 11.5 MHz PLL (TBD)
  - Sector 2 476 MHz PLL
  - RFoF system
  - Sector 10 476 MHz Cleanup VCO
  - Sector 10 2856 MHz PLL
  - MA switchover to new MO
  - Trigger Alignment system
- Needs to go through review

Operations/Procedures

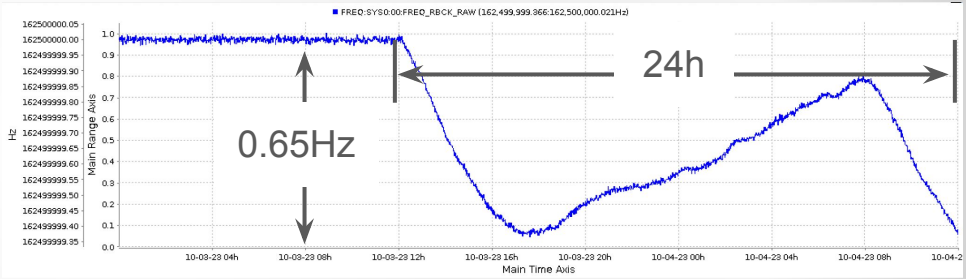
- What do failures look like
- How to recover
- How to plan outages

https://confluence.slac.stanford.edu/display/~rpm/Linac+Locking+Operations+questions

General Principles of Operation

All PLL feedbacks work in hardware. Runs without software

The 162.5 MHz Frequency Locker is a software feedback. Software can be down for 24 hours without much drift.



The trigger alignment/bucket jump feedback is software driven, but not critical to operation.

Networks can be down without causing interruption, with the exception of the RFoF system which communicates through the instrumentation network.

Outages

- Power outage or hardware failures in Sector 2 will disrupt the 476 MHz synthesis. In that case, the MA input cable needs to switch back to the original MO to allow LCLS/FACET to continue operation.
  - We could instrument an RF switch so recabling wouldn't be necessary. It is an infrequent occurrence, though.
- Power outage or hardware failures in Sector 10 will disrupt the 476 MHz delivery to LCLS/FACET, but have no effect on LCLS2 operation.

Summary

LINAC Locking will allow the XTCAV and STCAV diagnostics to be used with SC beam.

It is also a required step towards TXI operation

- Both LINACs/undulators deliver simultaneously to one hutch

The hardware has been installed and in the process of checkout/commissioning.

Documentation and knowledge transfer underway for TTO

Backup Slides