Behavioral Simulation using Vivado or VCS

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Introduction

Most projects follow the architecture depicted on the example on the links below.

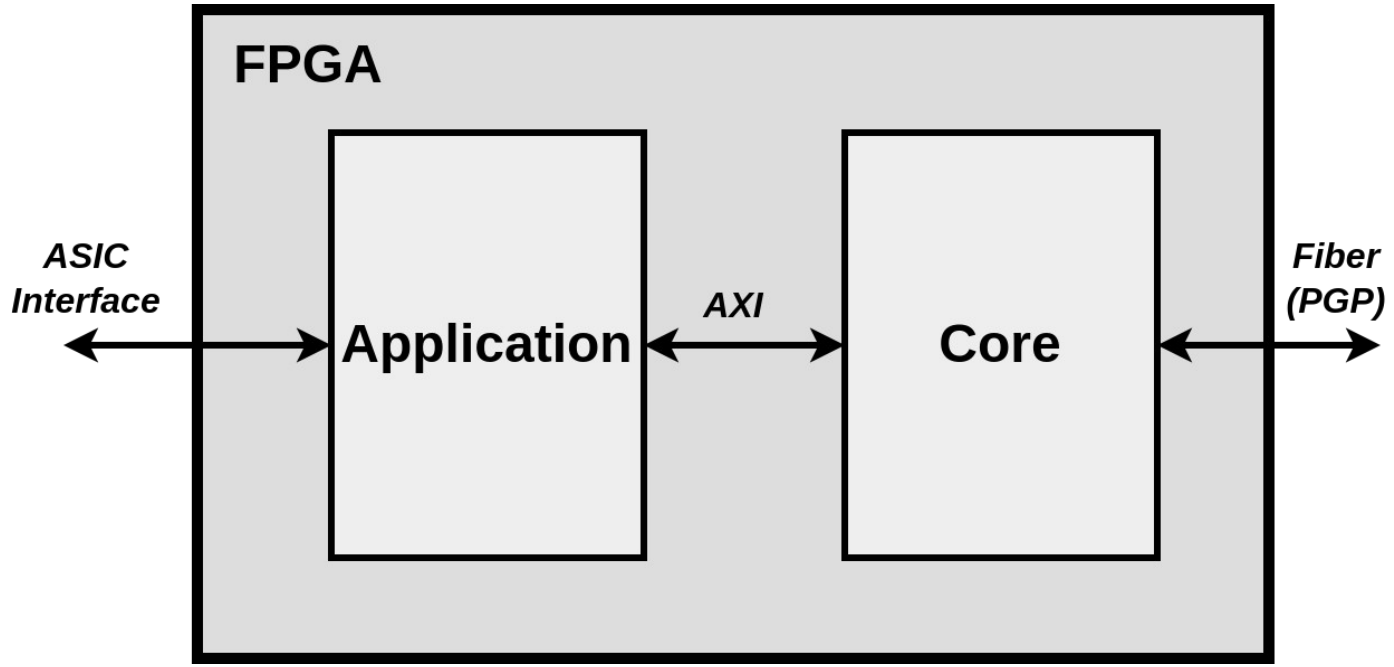
The aim is to create an RTL-based testbench that emulates the implemented design as closely as possible.

If the accompanying software (i.e. rogue) is also included in the simulation process, that is a big plus.

https://slaclab.github.io/Simple-PGPv4-KCU105-Example/index.html

https://github.com/slaclab/Simple-PGPv4-KCU105-Example

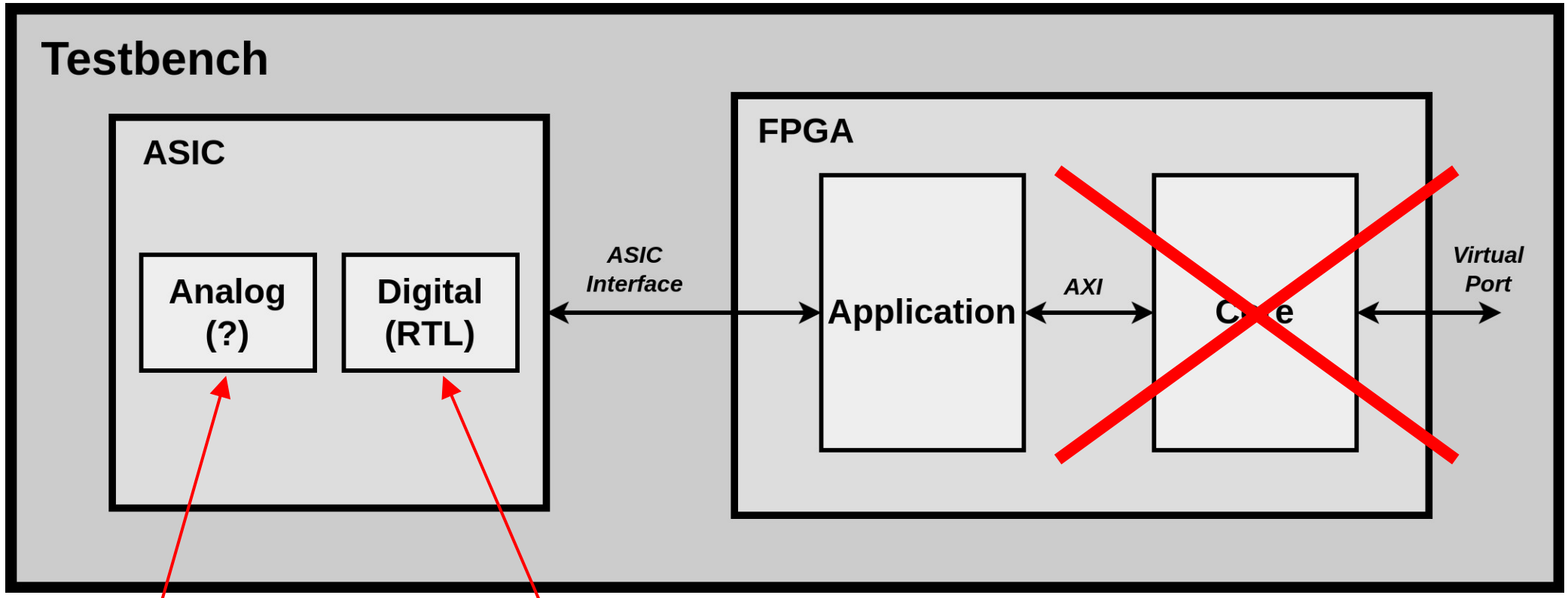
General Architecture for Detector Projects



Recurring theme in all repositories: one Application module (usually what we work with), and one Core module (static – part of the RTL infrastructure of the project)

If not working on a detector-related project, what changes is the fact that the Application module does not implement an ASIC Interface

General Architecture for Detector Projects – Vivado Tb



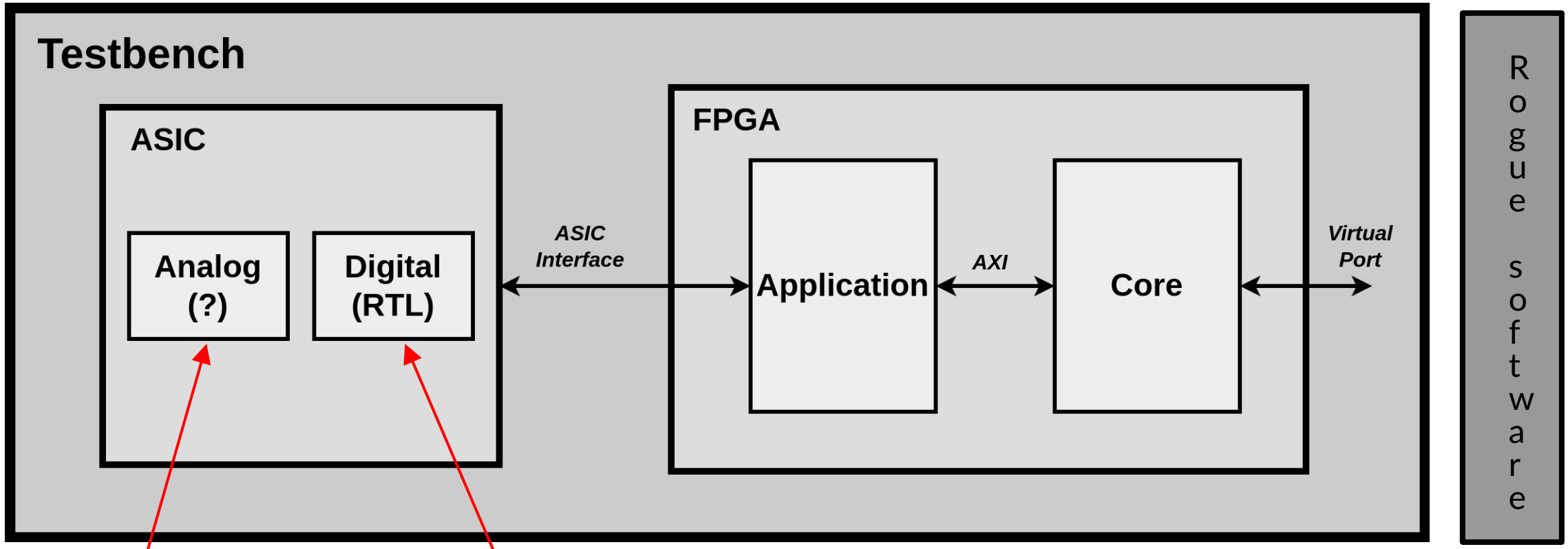
Sometimes some basic RTL-based model exists, sometimes not

Almost always taken from an ASIC-team managed repo

✓ Fast and easy to put together

✗ Does not include the software

General Architecture for Detector Projects – VCS Tb



Sometimes some basic RTL-based model exists, sometimes not

Almost always taken from an ASIC-team managed repo

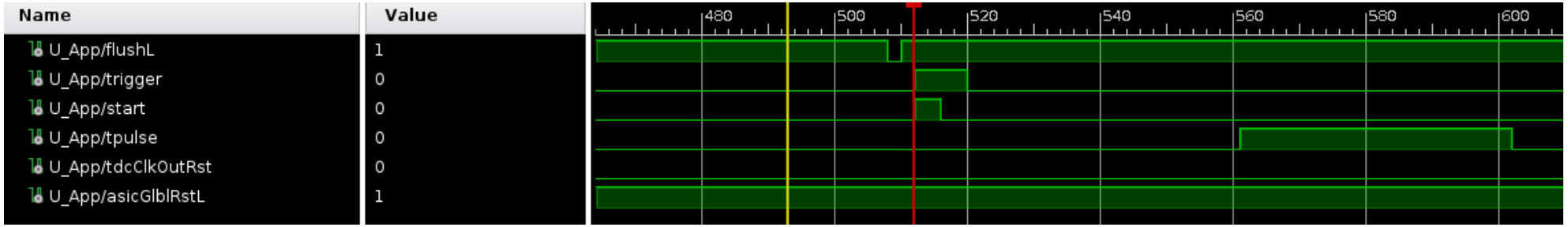
✓ Full testbench – emulates the rogue interface via a virtual port

✗ Takes more time to put together – software must be fully working

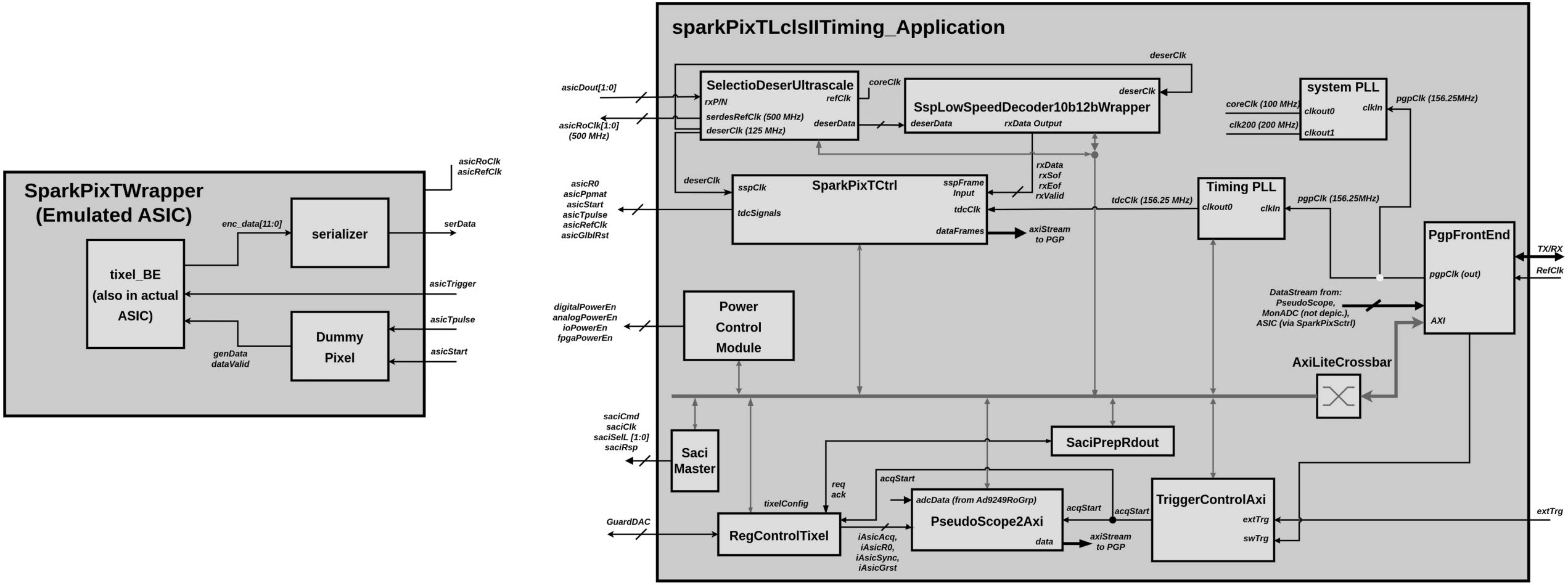
A fully-simulated project: SparkPix-T | Short Intro

the Data we are Looking for...

...and how we are injecting signals to the ASIC to get that Data



A fully-simulated project: SparkPix-T | Full Block Diagram



Links

https://github.com/slaclab/epix-hr-single-sparkPix-T
(mature project – full VCS simulation with rogue available)

https://github.com/slaclab/sparkpix-s-dev (*asic-fpga-integration-sim* branch)
(work-in-progress. Rogue works in VCS co-sim, but no full DAQ chain yet)

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