Pixel Sensor Testing

- Motivation
  - Upgrade in ~2017 (ATLAS LOI much earlier compared to this...)
  - Insertable B-Layer (IBL) a few years earlier ~2013 -> design to be determined ~1 year
- Lab testing
  - Systematic tests (characterization) of the new sensors
  - Ongoing since some years (one type of 3D sensor was tested at last test-beam)
  - (Identical) systematic tests will be performed on several places
- Today
  - My first interaction with sensor tests
  - Lots of things to learn...
    but, test setup seem to work fine :)
- Outline
  - Brief description about the sensors
  - Test lab setup
  - Results and discussion

Much of the information and pictures taken from talks by Alessandro et. al

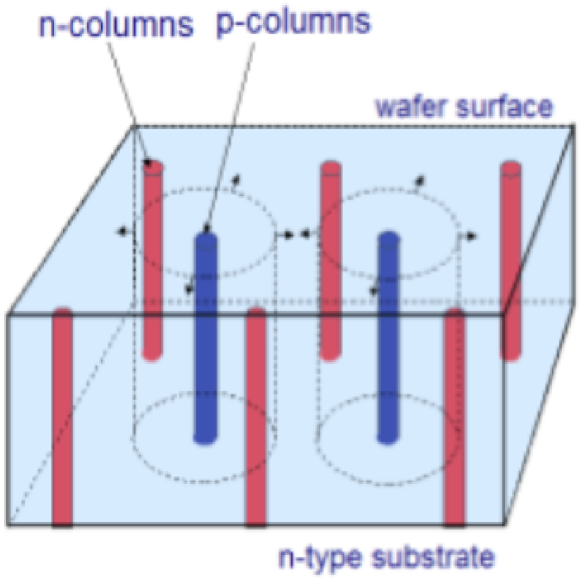
Overview of new pixel sensors

3D	**Planar Si**	**Diamond**
- Low depletion voltage - Fast signal collection - Radiation hard - Simple stave construction(active edge)	- n-in-p instead of n-in-n (no type inversion+run under-depleted) - Low depletion voltage (thin sensor) - “Simple and available“ (low cost?)	- Radiation hard - Fast signal collection - Operation temperature - (active edge)

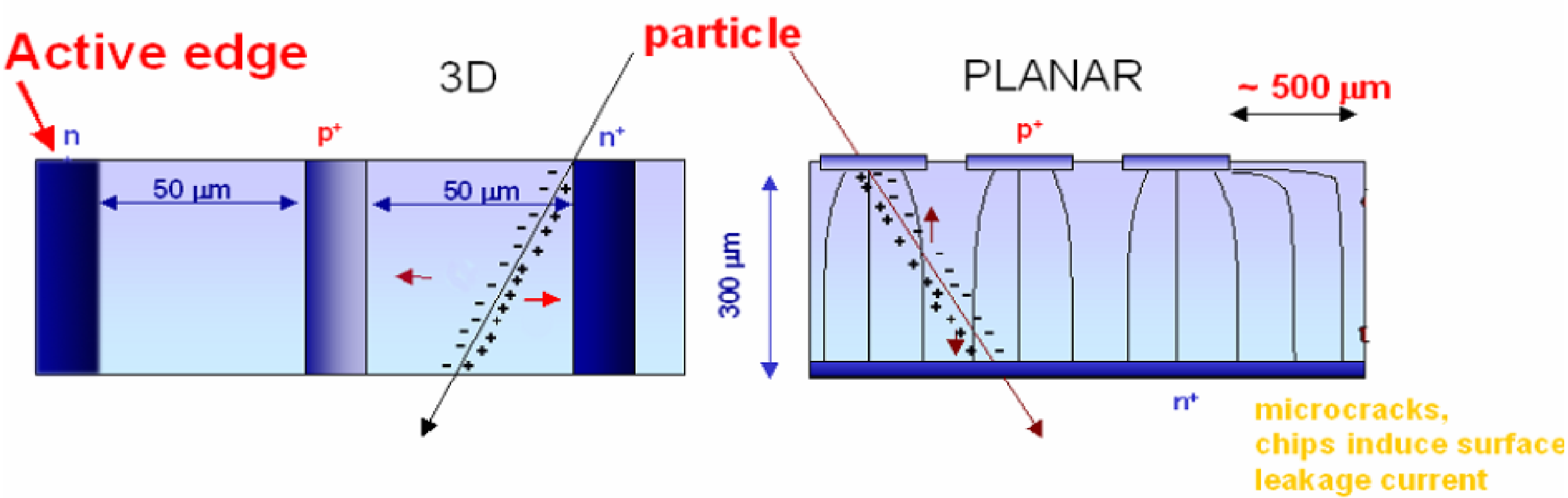
- Not up-to-date on the relative status w.r.t. upgrade and/or IBL projects
  - Believe that 3D is favored for IBL...
- Will show a (extremely) brief 3D sensor introduction
  - Only one? A. I only had time to “play” with one type of sensor so far
- Comparisons (also among similar sensors) will give more info
  - In particular to the current pixel sensors
  - Noise, bias voltage (power),etc. + (hopefully) source studies such as efficiencies,etc.

Full 3D Sensors

S. Parker et al. NIMA395 (1997)



- **Radiation hard**
- **Low depletion voltage**
- **Fast signal collection**
- **Active edge**
- **Fabricated and tested**
  - **"3DC" Stanford (tested w/ ATLAS front end, also irradiated sensors)**
  - **"3DC" Sintef (Oslo, tests?)**

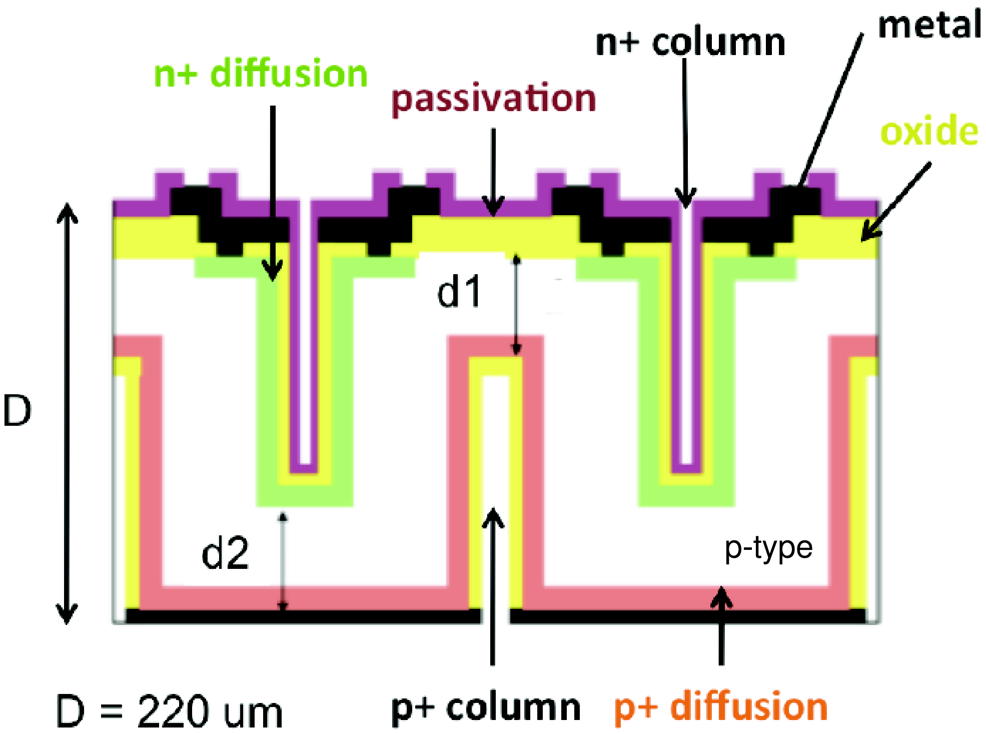


Mod-3D Sensors

G-F Dalla Betta/UniTN, M. Boscardin/FBK

Double column, double type columns (FBK-DDTC1)

2/3/4 electrodes per pixel



D = 220 um

d1 ~ 20 um

d2 ~ 100 um

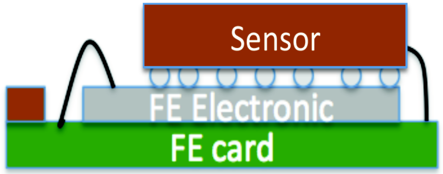
- **Radiation hard**
- **Low depletion voltage**
  - **Increase E-field after full depletion**
- **Fast signal collection**
- **No support wafer needed..?**
  - **Depending on active edge...**
- **No active edge?**
- **Low Q collection times in col. tips**
- **Fabricated and tested**
  - **FBK/IRST (Trento) + others**

- Bump bonded (Indium) to ATLAS front-end chip
  - For upgrade and(?) IBL there will be a new front-end chip

- All very preliminary results are shown using this sensor
  - No particular reason except practical ones

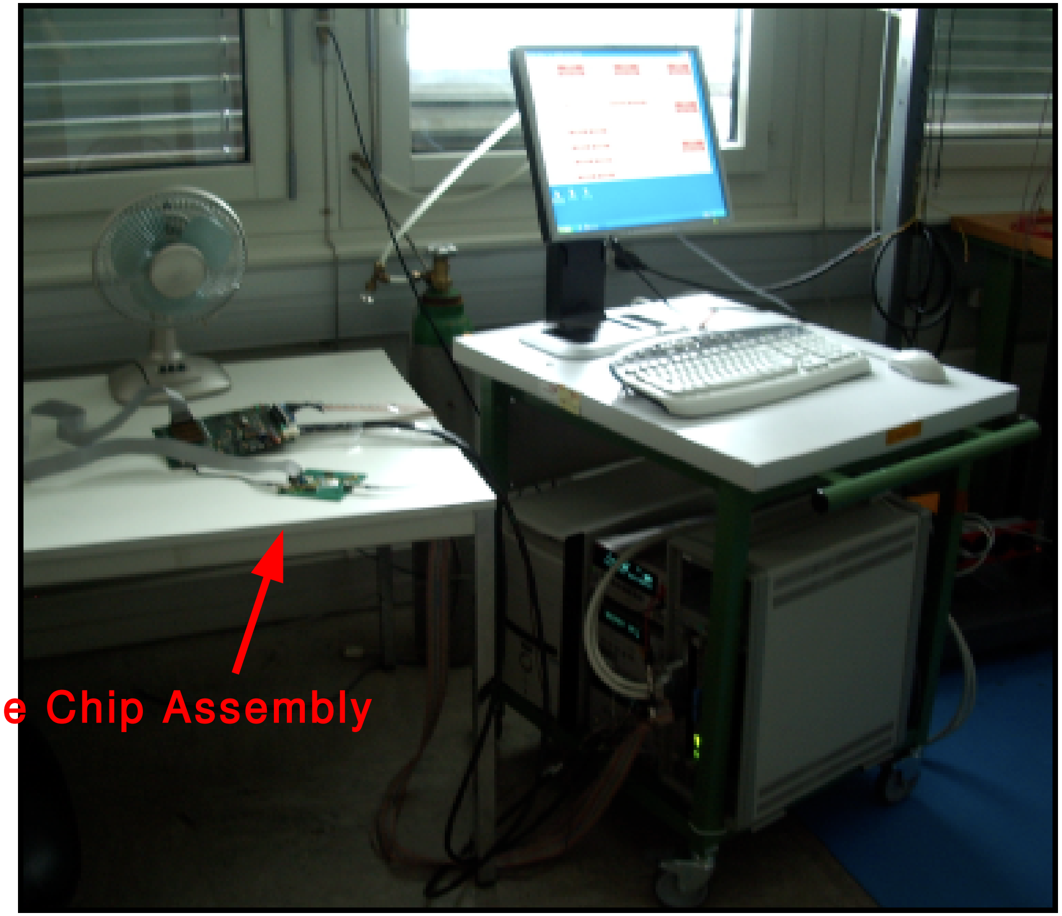
Pixel size:50x400μm^2

2880 pixels: 18x160



Test Lab Setup

- "Semi" clean room Building 161 2nd floor
- Communication handled by TurboDAQ
  - Two TurboDAQ setups; stationary + mobile

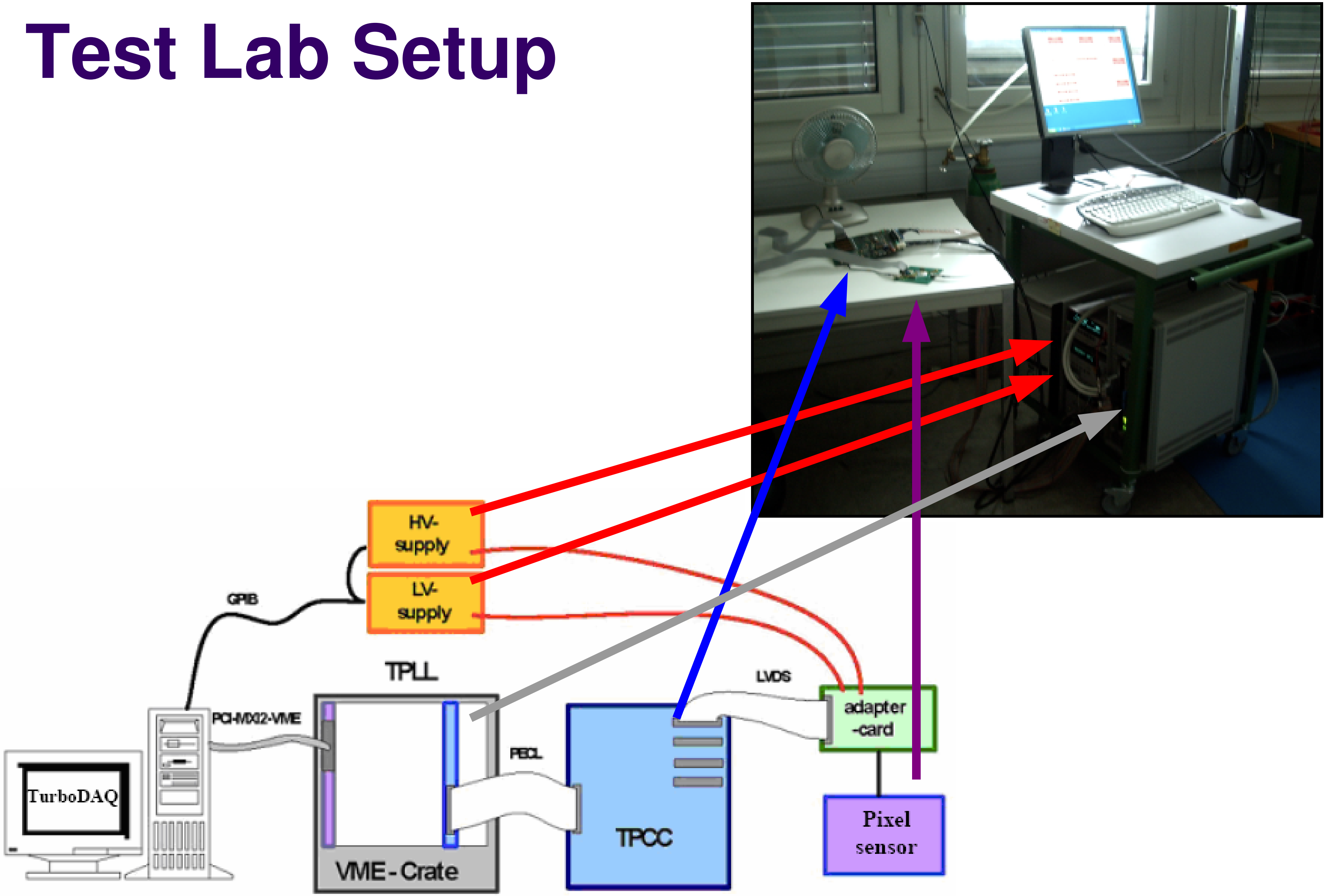


Single Chip Assembly

- No intro about TurboDAQ
- Developed (originally) at Berkeley
  - "Maintained" by Bonn?
- Some documentation
  - But not easy (at least to me)
- Goal of last week
  - Learn basic commands
  - Run simple scans
  - Handle results (~plot)

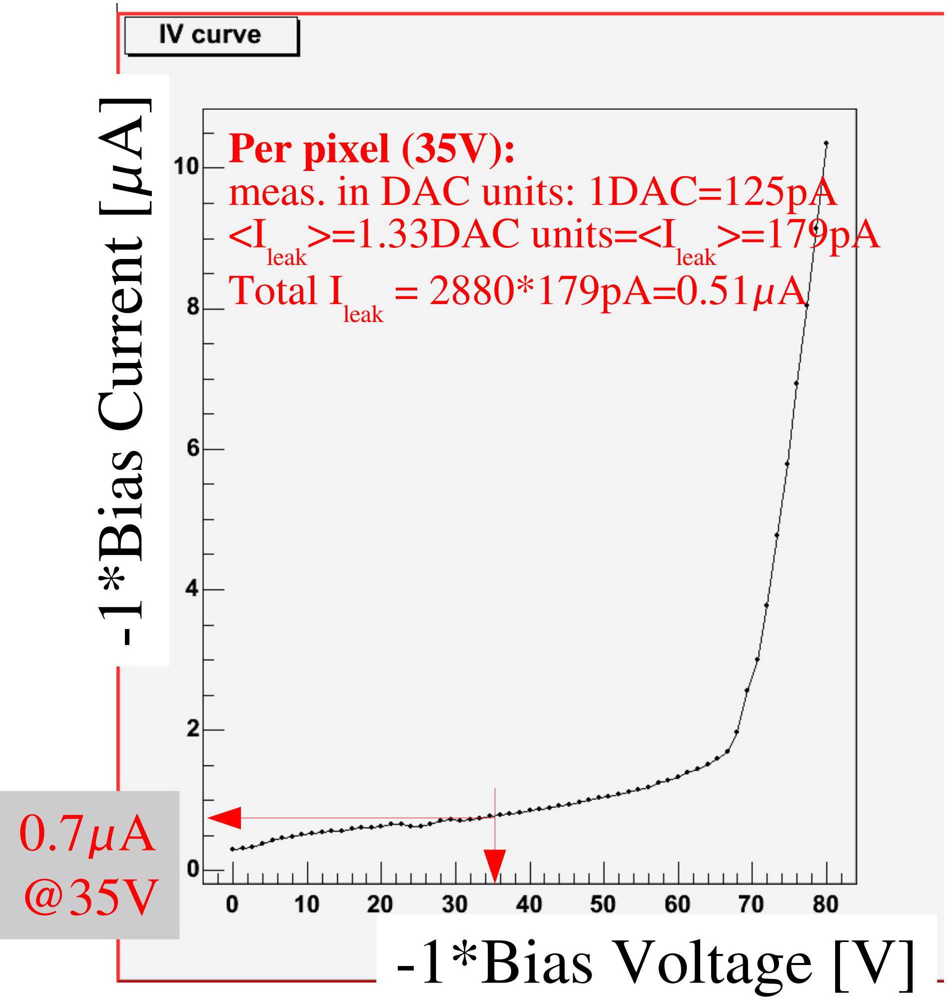
  -> Interpret results

Test Lab Setup



Sensor Testing: I-V curve

- Establish a working operation point for the detector
- Measure current for the detector (i.e. leakage current) as a function of bias voltage

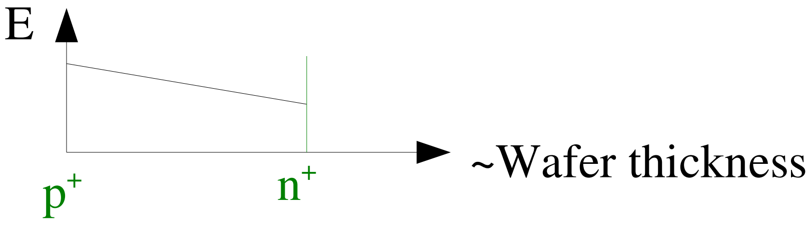


Per pixel (35V):
meas. in DAC units: 1DAC=125pA
$\langle I_{leak} \rangle$=1.33DAC units=$\langle I_{leak} \rangle$=179pA
Total I_{leak} = 2880*179pA=0.51μA

0.7μA @35V

- ~11V should give full depletion
- V_{bias}=0: leakage current ~0.3μA....
- Why not start at 11V?

Operation best in saturation region



- "Breakdown" at 75V

not sure why (not new); avalanche mode?

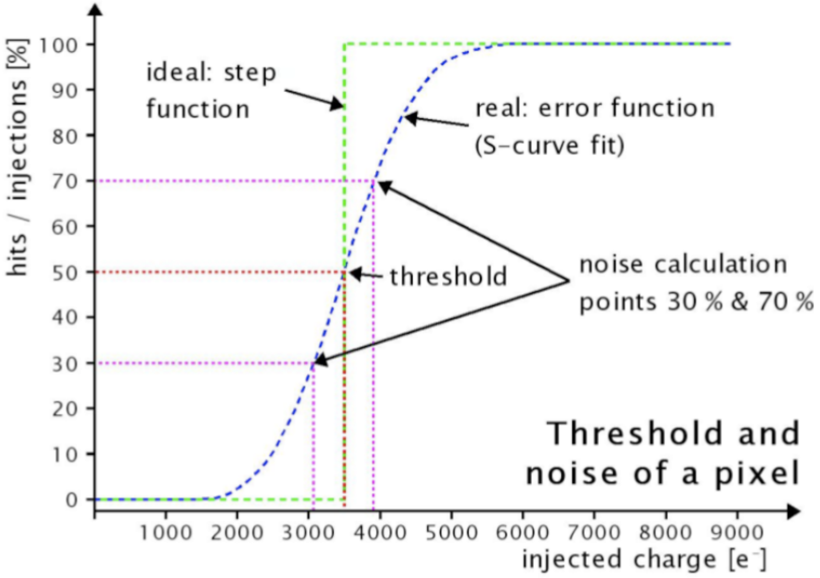
- Operate at 35V bias voltage

Pixel-by-pixel leakage measurement Not done yet!

Sensor Testing: FE tuning

A. La Rosa

Threshold & Noise



- Voltage pulse **VCal** injected into “injection capacitor” with capacitance e.g. **Clow**
- Input amplifier sees charge **Q≈VCAL×Clow**
- 100 injections/per pixel in range [0e$^-$,9000e$^-$]
- Hits per pixel measured for each injection:

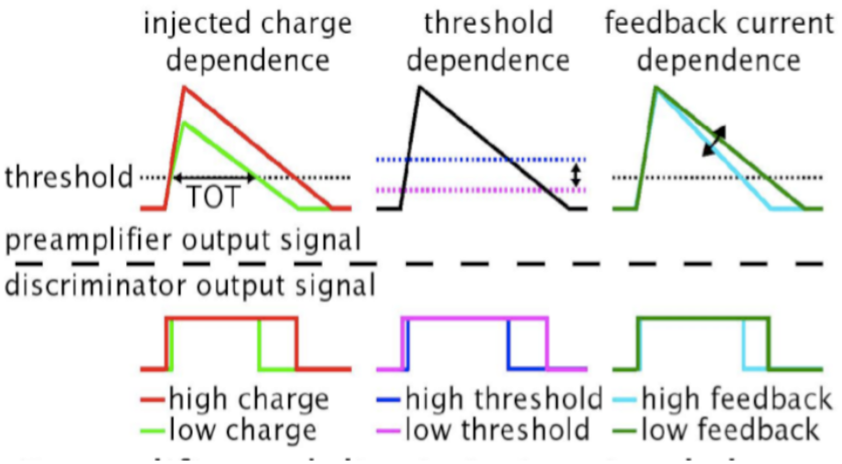
  response=hit/injection
- Ideal: Q>threshold⇒hit

  Q<threshold⇒no hit

  Step function

Real life: convolute with Gauss. noise **“S-curve”**

Preamplifier/discriminator shape



- Preamplifier outputs approx. triangular pulse
- Time-over-threshold depends
  - -Charge deposited
  - -Threshold
  - -Feedback current
- ToT measured in 25ns steps (start/stop clock)
- ToT calibration aims to harmonize response across all pixels for a given deposited charge

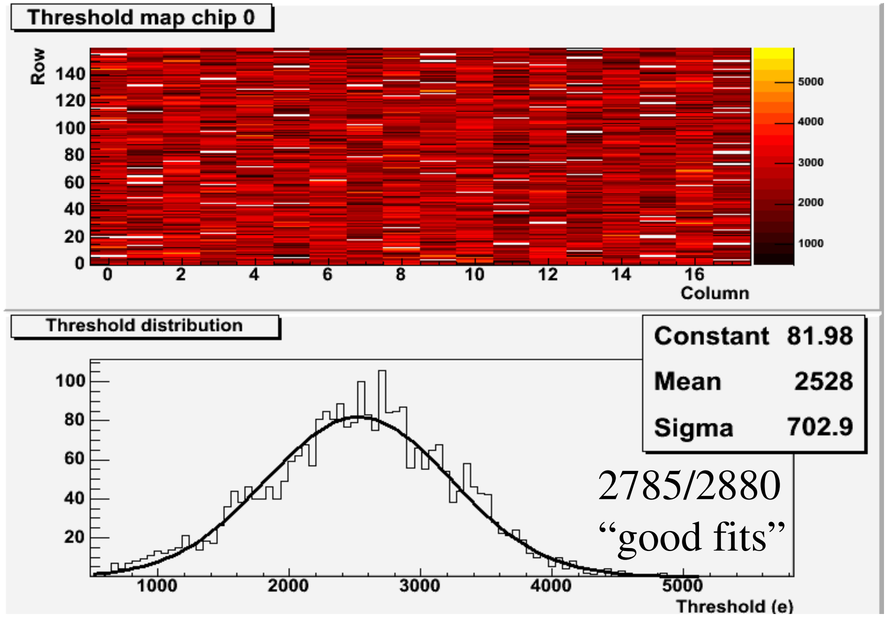
  60ToT@25000e$^-$ (30ToT@20000e$^-$)

(MPV for m.i.p. $\leqslant$20ke$^-$? for 220μm Si though)

Sensor Testing: Threshold

- Calibrate the threshold of the discriminator to a a priori given value
  - In this case threshold=$3200e^-$ ($4000e^-$ in the ATLAS pixel)
  - Goal is to operate (safe from noise) with as low threshold “as possible” -> more signal

Threshold scan using “default” settings



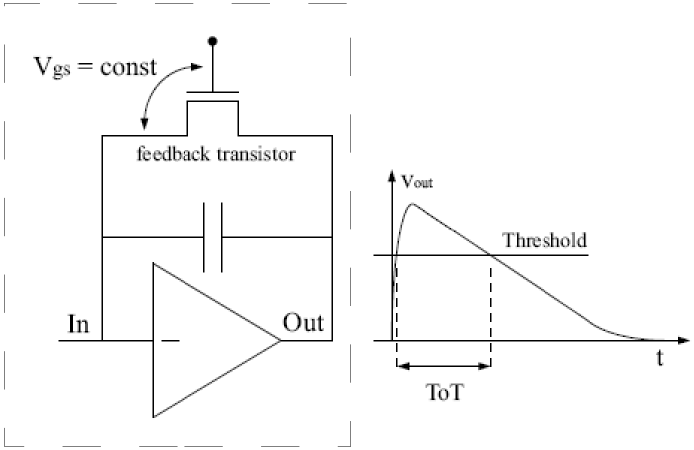
2785/2880 “good fits”

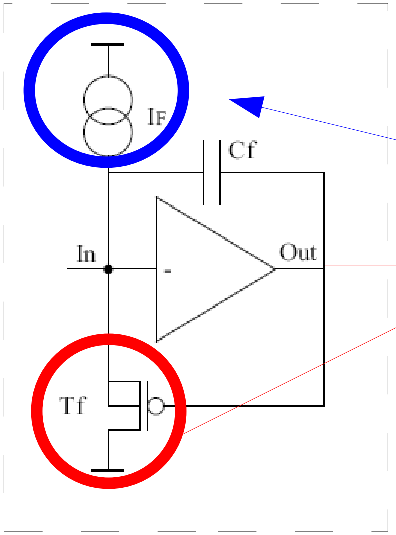
•The threshold is controlled by setting two values called **GDAC** and **TDAC**

GDAQ: 5-bit

TDAQ: 7-bit

Front End





Comparator circuit

- Feedback current circuit built from
  - resistor
  - capacitor(6fF)

  In parallel
- Resistor here exchanged with transistor

Tf (operating in linear region....?)

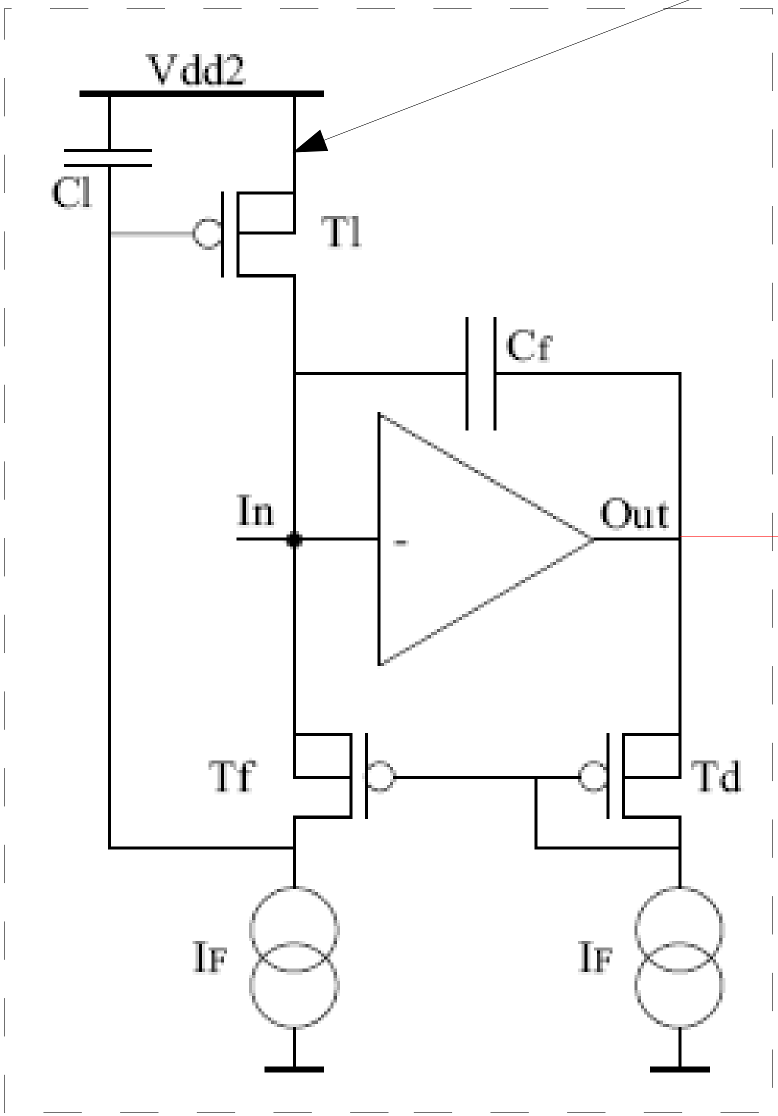
- Capacitor discharging at constant current

  approximately triangular shape
- Leakage current compensation

  auto adjusted “constant” input current **IF**

FE: Threshold

Note: sophisticated negative feedback **If** circuit to cancel leakage current



Threshold is defined as:

"The difference between the threshold potential (of the comparator) and the DC potential (Out) if the amplifier"

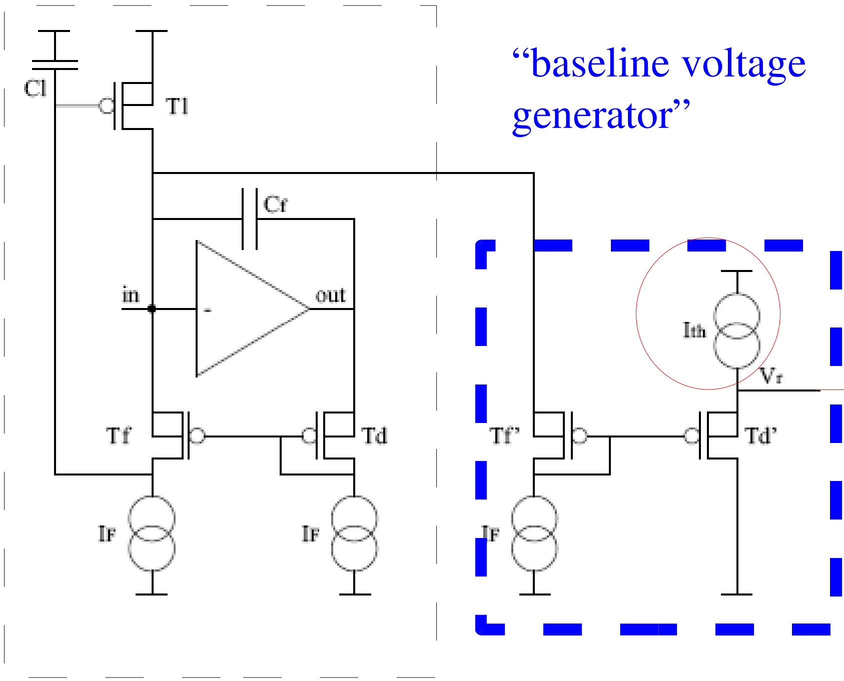
Comparator circuit

The power supply is non-uniform

- one global threshold voltage per matrix
- the potential drop leads to varying thresholds

Not understood yet!

FE: Global threshold



"baseline voltage generator"

Add circuit that "replicates+adds" to output

Controlled by current **Ith**

$Ith = N\times If$

Comparator circuit

n:slope

U_T:trans.spec.

"new"output voltage **Vr** :

$$Vr = V_{out}+n\times U_T\times\log(N)$$

The current **Ith** is generated by

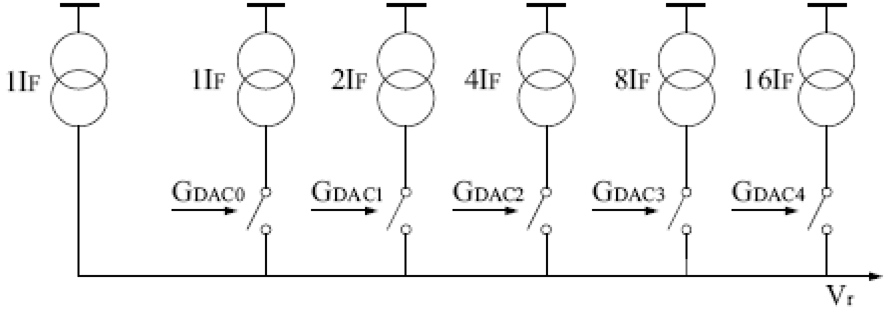
Turning on/off control logic 0-4: **$GDAC_i$**

$$V_{ThrUntuned}=n\times U_T\times\log(N)$$

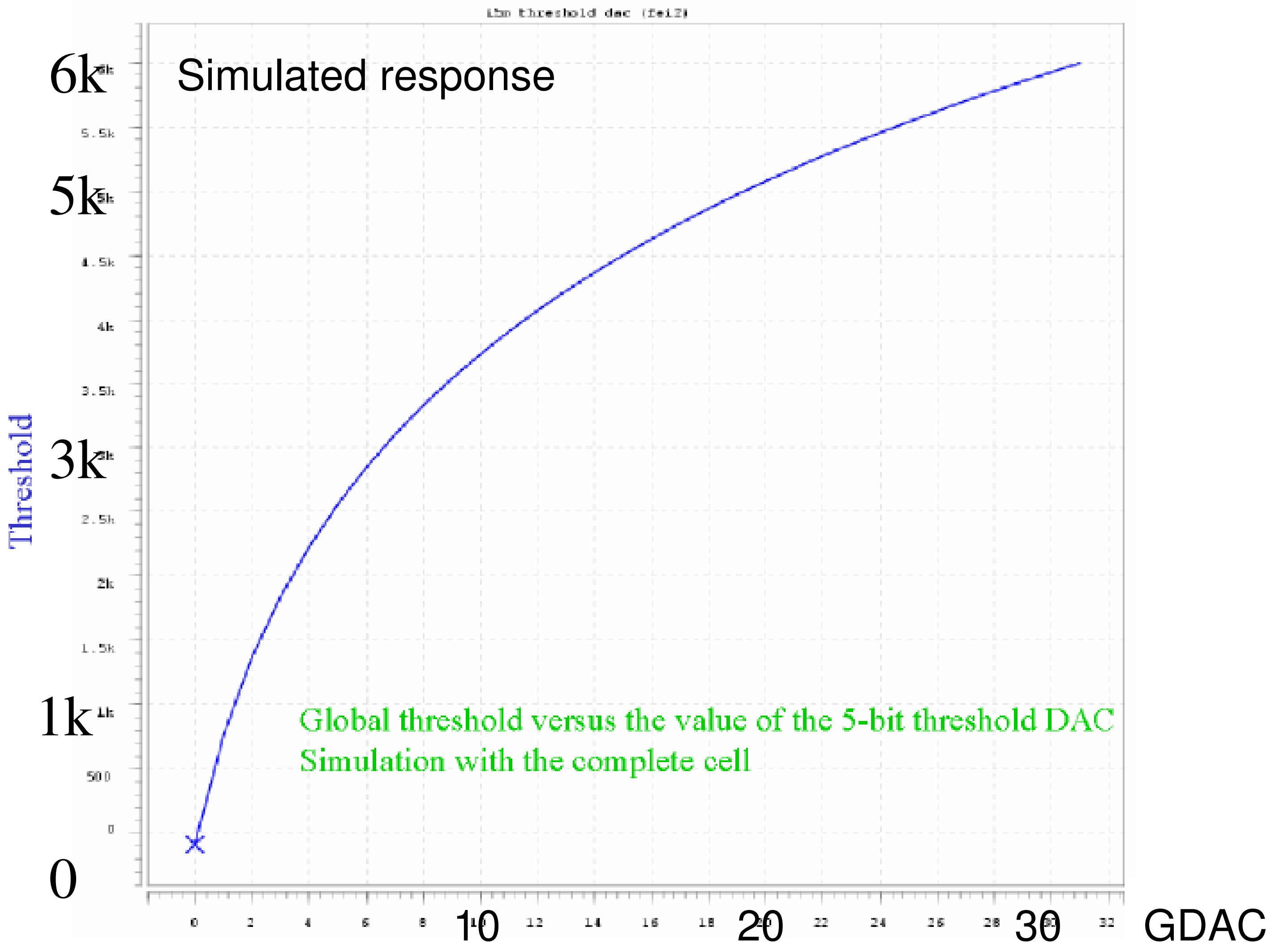
$$N=\Sigma 2^i GDAC_i$$

N is **per FE** hence "global"

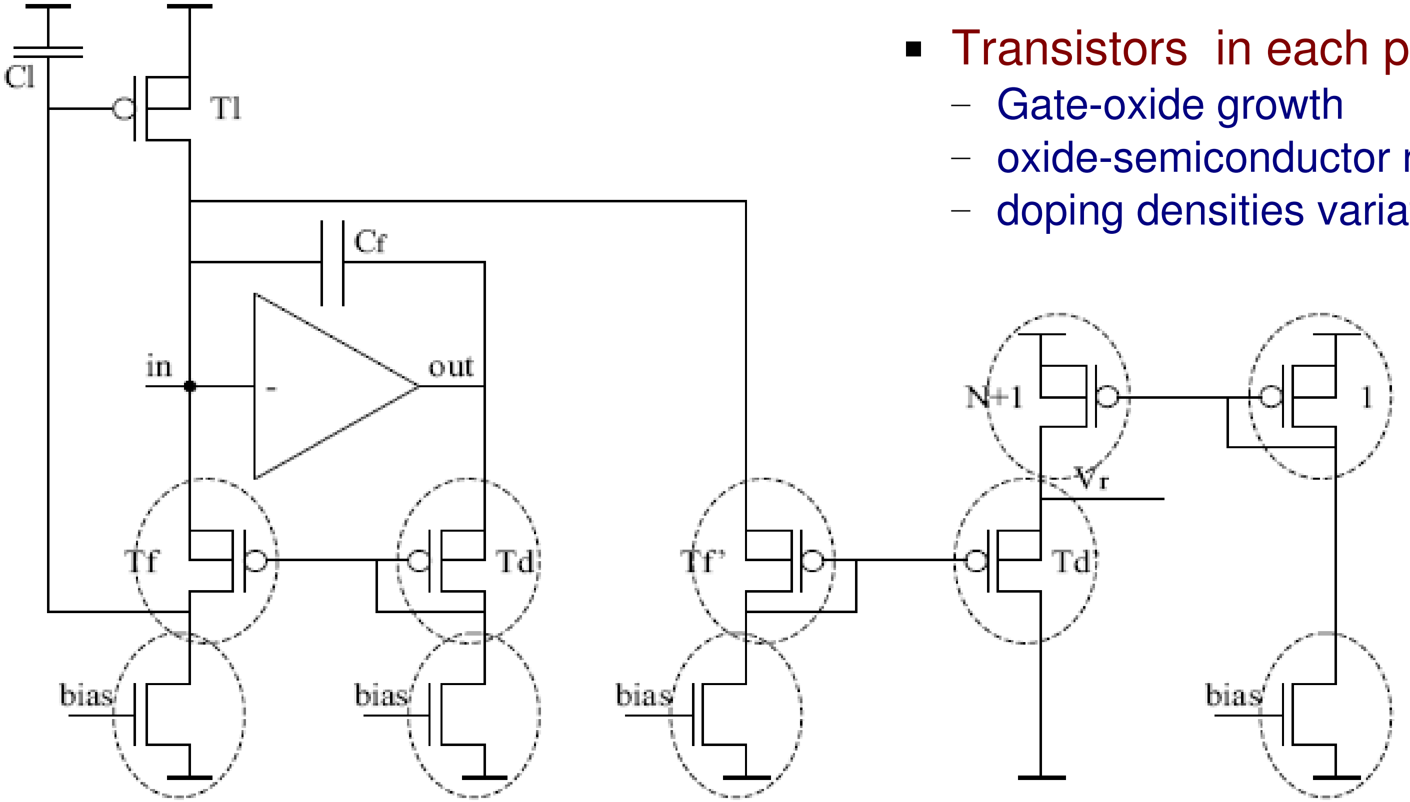
Each pixel is supplied from
32 identical current sources



FE: Global threshold



FE: Threshold “dispersion”



- Transistors in each pixel not identical
  - Gate-oxide growth
  - oxide-semiconductor non-uniformities
  - doping densities variations,...

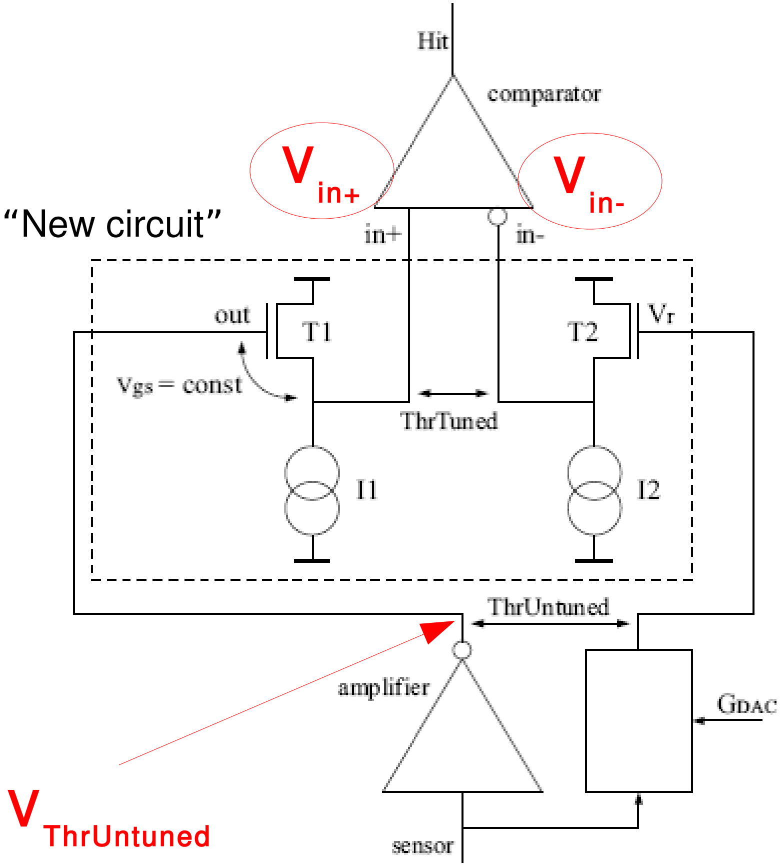
(Order of)10 transistors per pixel with each being slightly different

threshold dispersion:

$$\sigma_{Th}^2 = \sum_{i=1}^{10} \left(\sigma_{V_{Thi}}^2 + (nU_T)^2 \left(\frac{\sigma_{I_{subi}}}{I_{sub}} \right)^2 + (nU_T)^2 \left(\frac{\sigma_{Wi/Li}}{Wi/Li} \right)^2 \right)$$

FE: Threshold tuning

- Another circuit is added to manipulate/tune threshold **per pixel(or "locally")**



The tuned threshold seen at the comparator is

$$V_{thrTuned}=V_{in+}-V_{in-}$$

$$= V_{thrUntuned}+n\times U_T\times\log(I_1/I_2)$$

The currents $I_{1,2}$ are determined by

Digital-to-Analog Converters (DACs)

Steered by 6 control logic bits: **TDAQ**$_i$ ('N')

$$V_{thrTuned}= V_{thrUntuned}+n\times U_T\times\log(N/N-63)$$

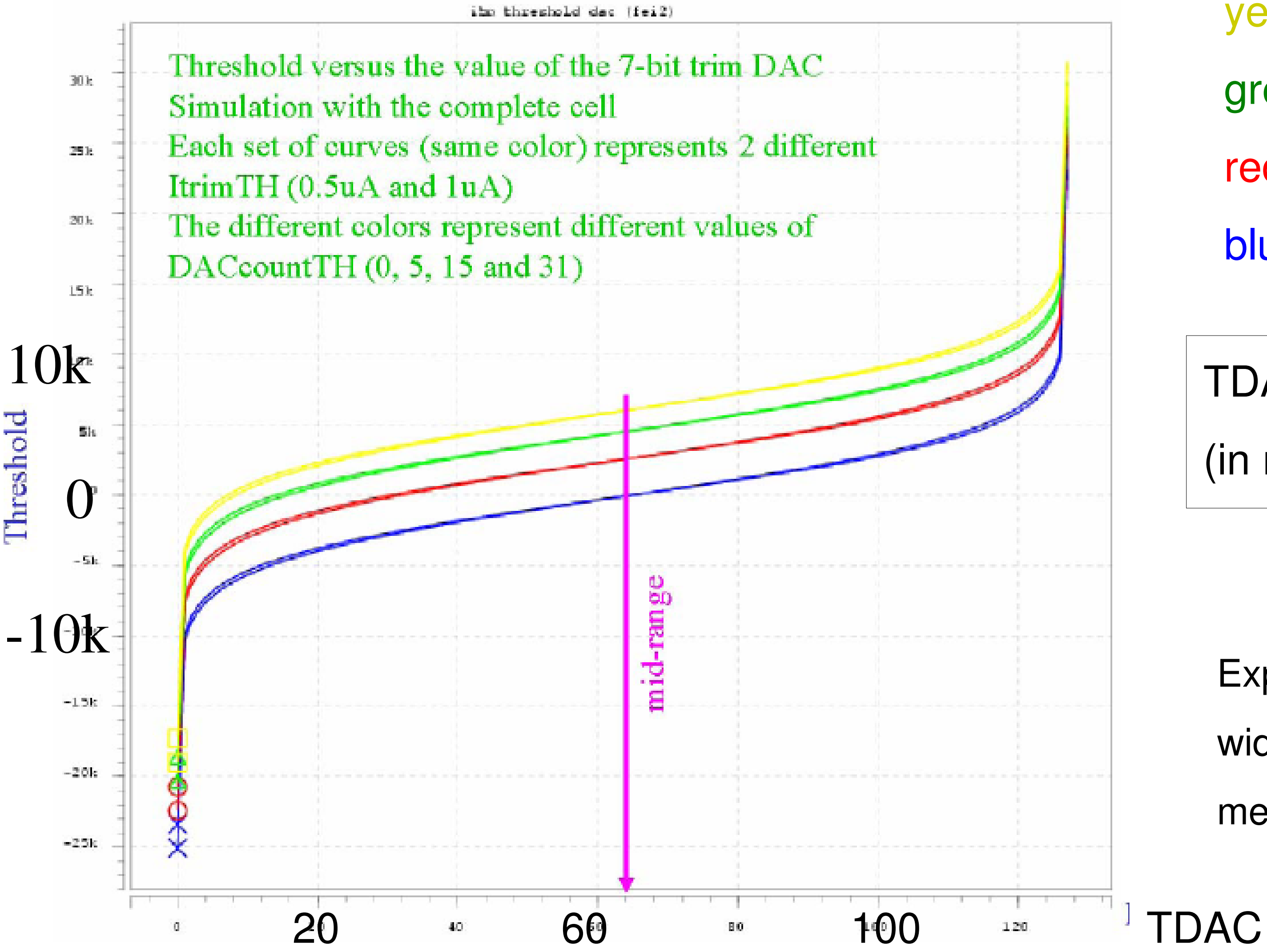
"Bit for free"leads to 7-bit ->128 instead of 64

Using "linearity" of the tuning...

Called "TDAC tuning"

Sensor Testing: GDAC &TDAC

Simulated response



Threshold versus the value of the 7-bit trim DAC
Simulation with the complete cell
Each set of curves (same color) represents 2 different ItrimTH (0.5uA and 1uA)
The different colors represent different values of DACcountTH (0, 5, 15 and 31)

yellow:GDAC=31

green:GDAC=15

red:GDAC=5

blue:GDAC=0

TDAQ=1 ⇔ Δthr 75e-

(in mid-region)

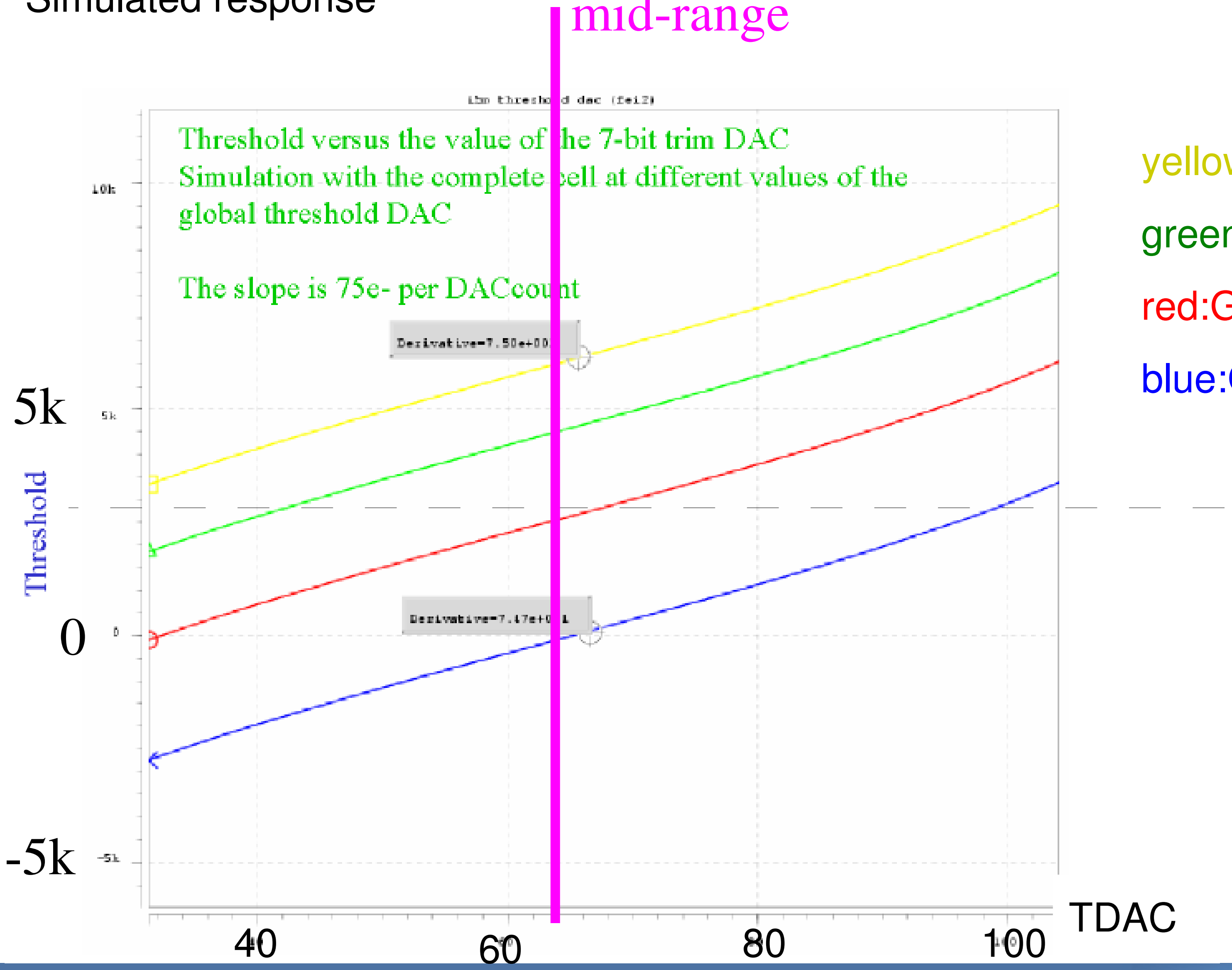
Expect threshold

width ~100e-

mean ~ within X?

Sensor Testing: GDAC &TDAC

Simulated response



Threshold versus the value of the 7-bit trim DAC
Simulation with the complete cell at different values of the global threshold DAC

The slope is 75e- per DACcount

yellow:GDAC=31

green:GDAC=15

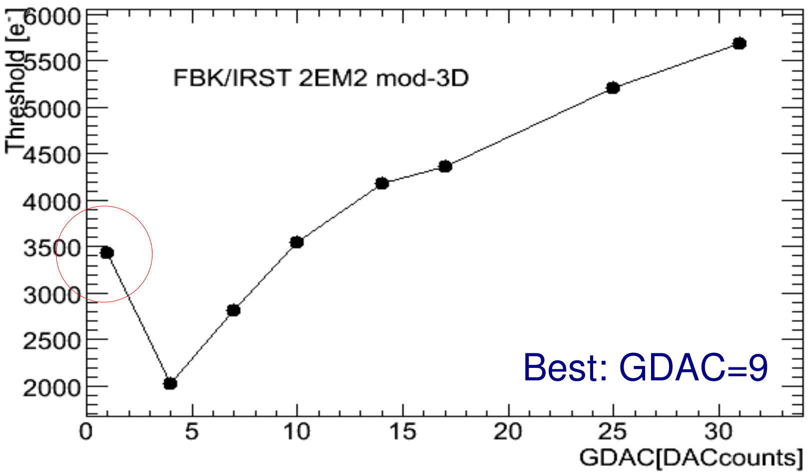
red:GDAC=5

blue:GDAC=0

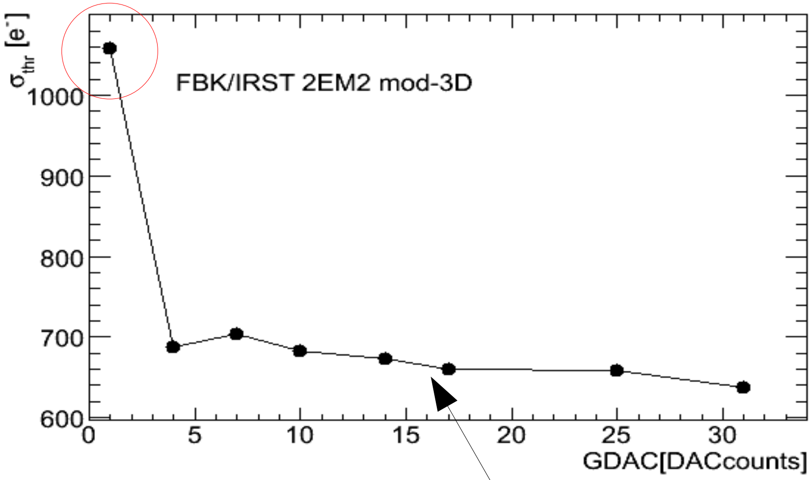
Sensor Testing: GDAC

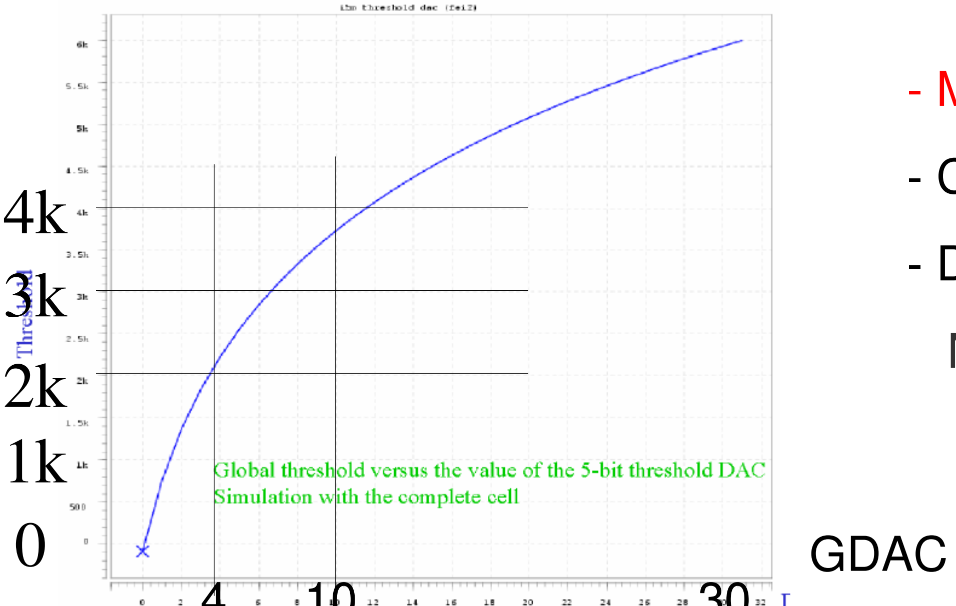
2785/2880
“good fits”

- Use the GDAC “bits” to manually change threshold (3200e-)



Best: GDAC=9





Global threshold versus the value of the 5-bit threshold DAC
Simulation with the complete cell

- Many failed fits at GDAC 1 and 31

- Consistent with “simulated response”

- Dispersion correlated with GDAC?

Not obvious from formula?

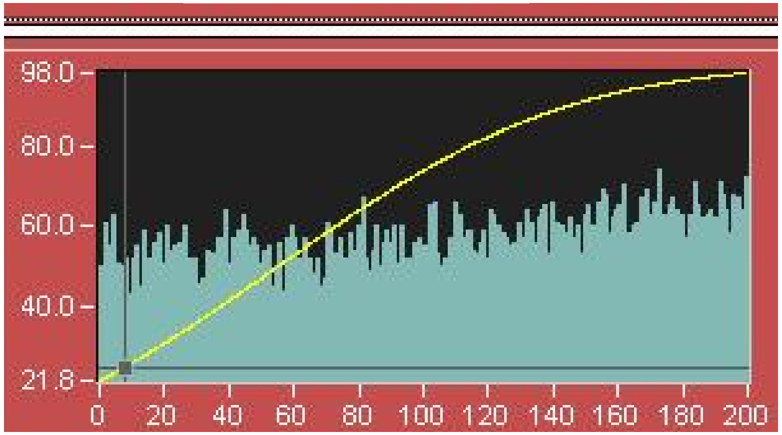
$$\sigma_{Th}^2 = \sum_{i=1}^{10} \left(\sigma_{V_{Thi}}^2 + (nU_T)^2 \left(\frac{\sigma_{I_{subi}}}{I_{sub}} \right)^2 + (nU_T)^2 \left(\frac{\sigma_{Wi/Li}}{Wi/Li} \right)^2 \right)$$

Sensor Testing: GDAC

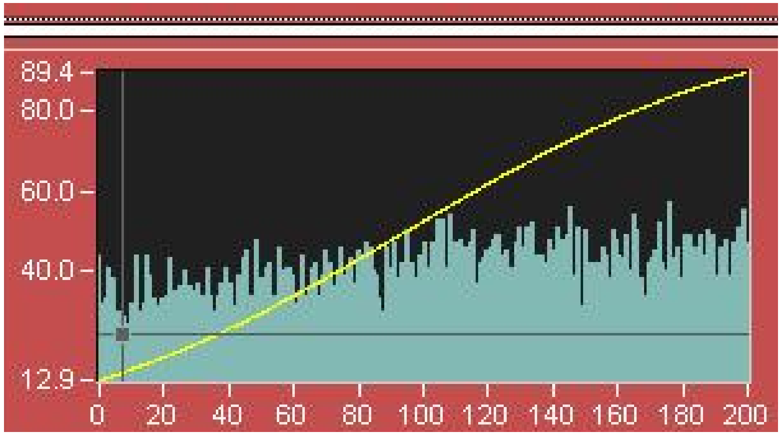
FBK-2EM2

- Example (raw) hit distributions for low GDAC (=1)
- Only a few pixels returned “valid” threshold
  - Failed fits

Col10 Row 64

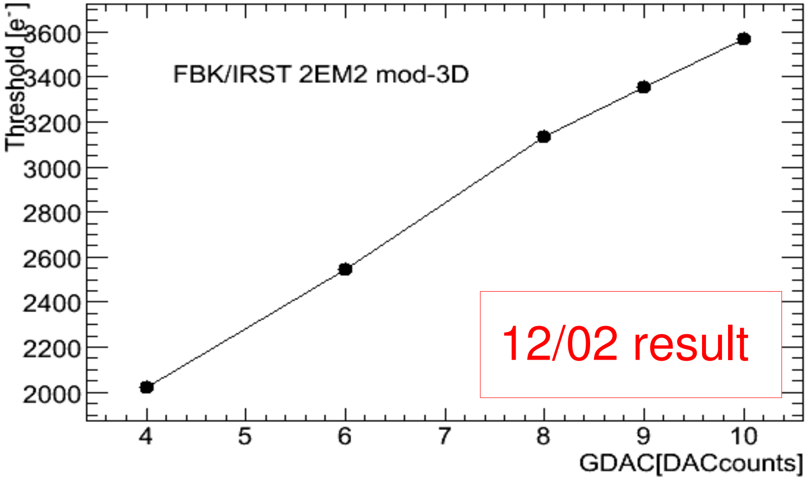


Col11 Row 33

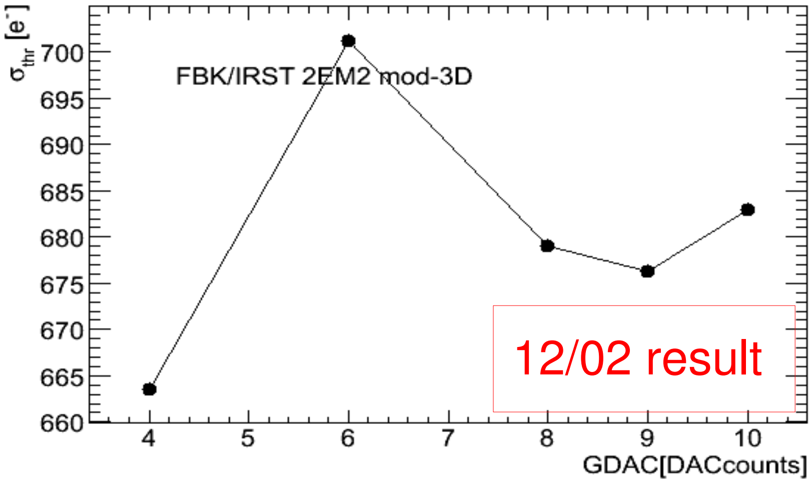


Sensor Testing: GDAC

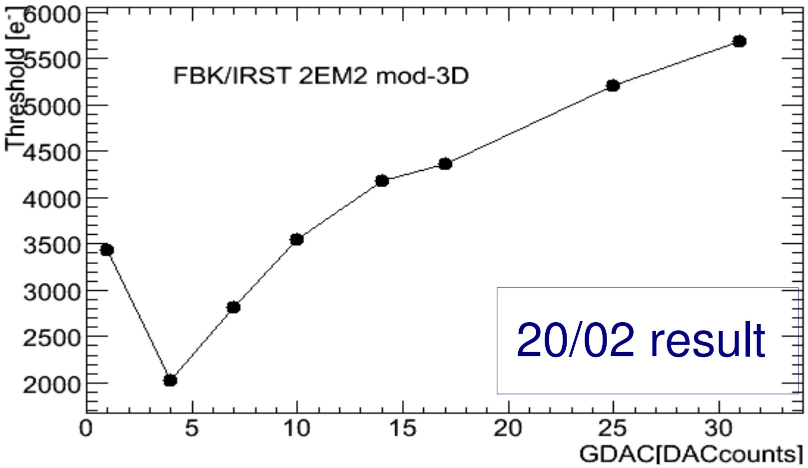
- Use the GDAC “bits” to manually change threshold (3200e-)



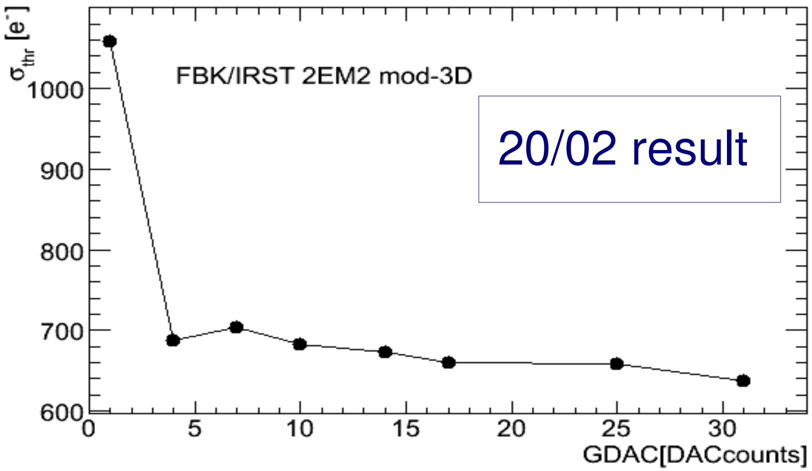
12/02 result



12/02 result



20/02 result



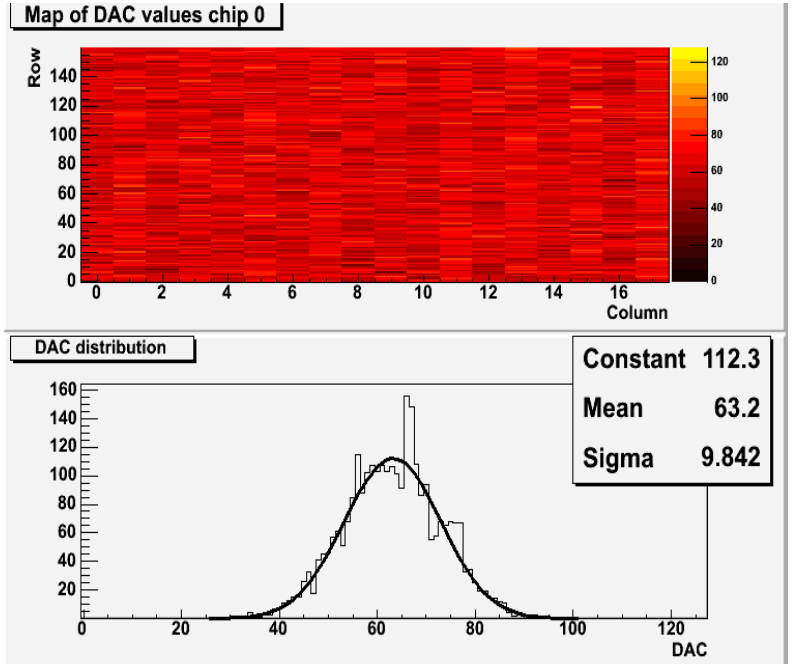
20/02 result

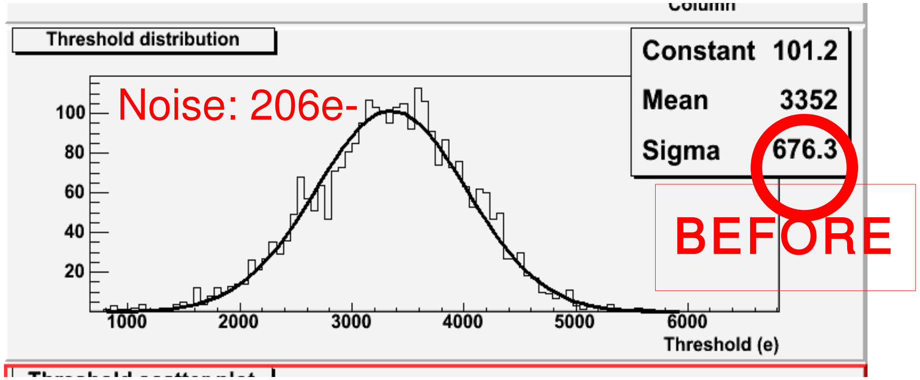
Note the different scales.

Sensor Testing: TDAC

- Run a TDAQ tuning
  - Adjusting per pixel each TDAQ “bit” to get the correct threshold (3200e-)

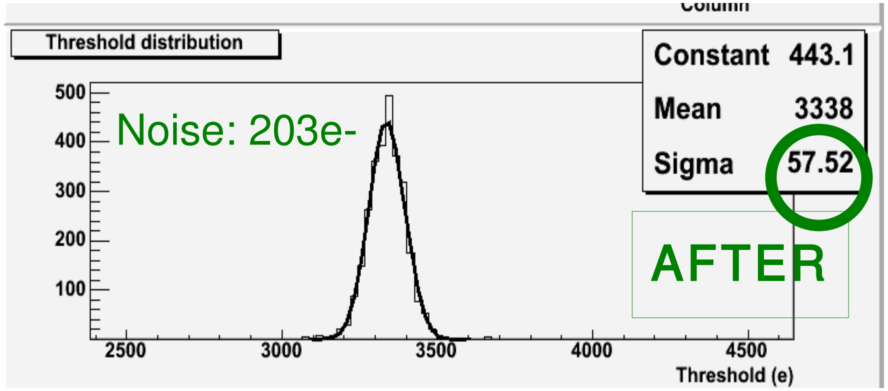
TDAC distribution





Noise: 206e-

BEFORE



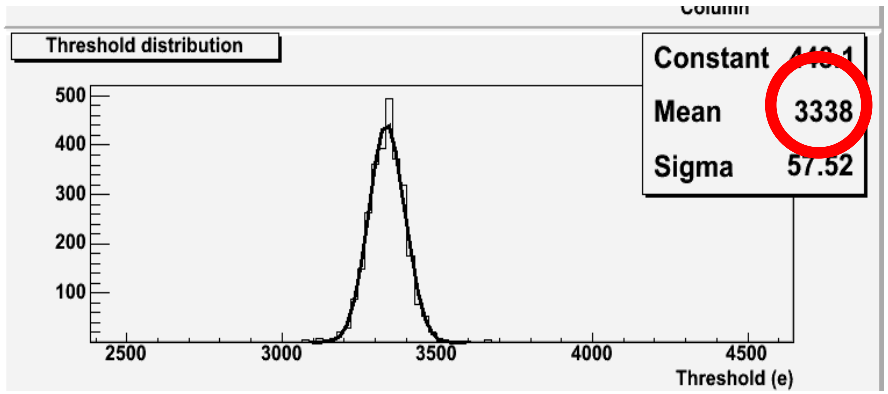
Noise: 203e-

AFTER

- Successful? TDAQ tuning
  - Width of the threshold decreases from 676.6e- to 57.62e-
  - BUT: threshold mean still not (very) close to 3200e- (....should be more precise?)

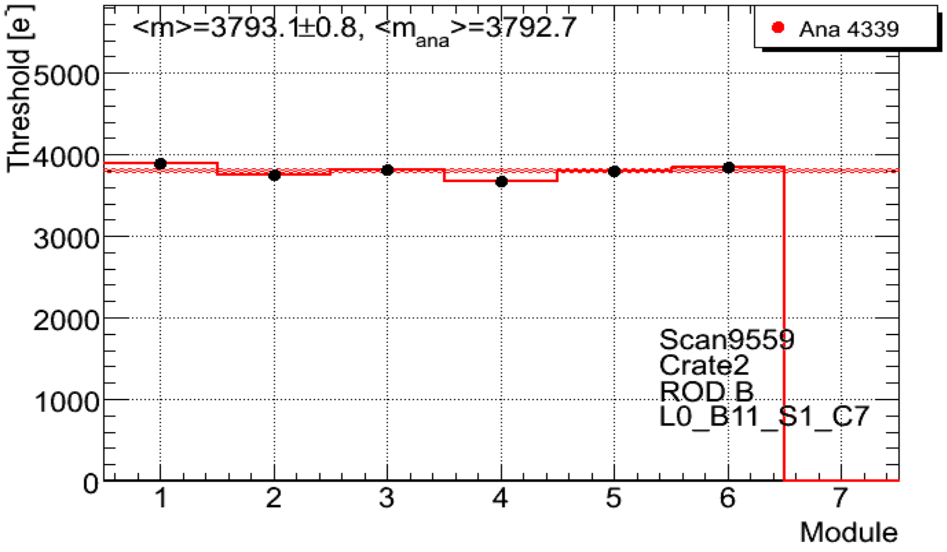
Sensor Testing: TDAC

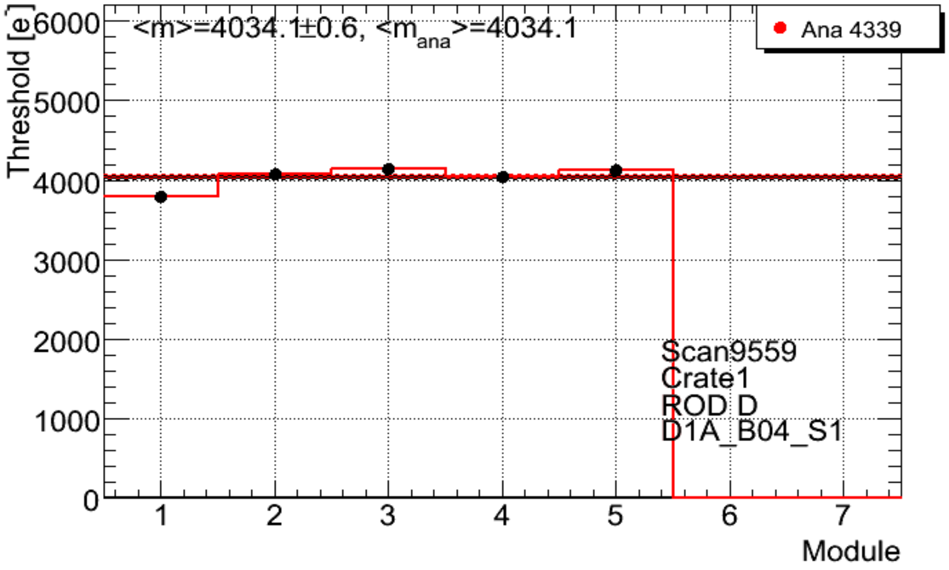
- Why is the mean threshold shifted w.r.t. The tuned value after TDAQ
  - TDAQ resolution should be 75e- and there are 2880 pixels
- Markus Keil indicated that it should be within errors after TDAQ tune
  - Remember some bug in (old) DSP code



Sensor Testing: TDAC

- Interesting use case for the visualization browser
  - Unfortunately I hadn't implemented a way to see all mean values for the whole detector or other less general way
  - Have to go via individual PP0 to PP0 (but still using the browser!)

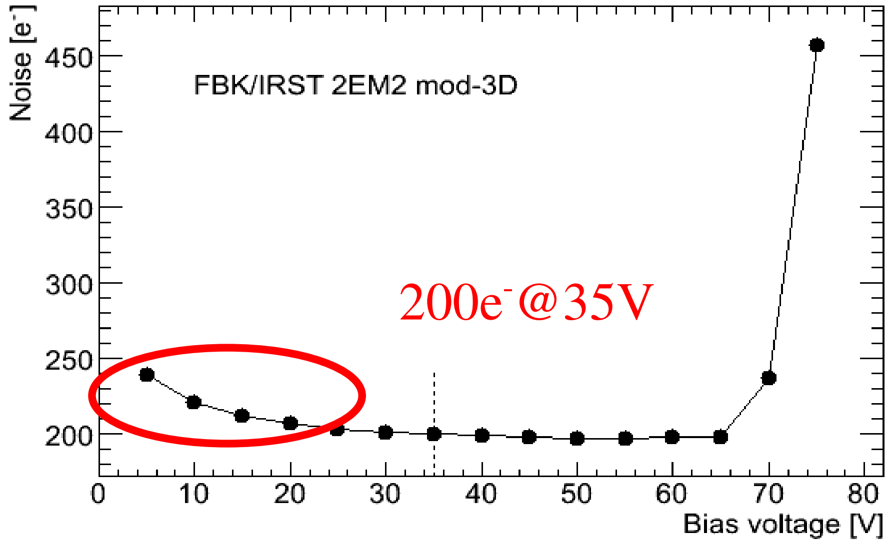




- Found some outliers (i.e. not consistent with 4000e- or bugg in DSP code?)
  - NOTE: no quality control for the scans -> another topic for special visualization discussion

Sensor Testing: Noise vs bias

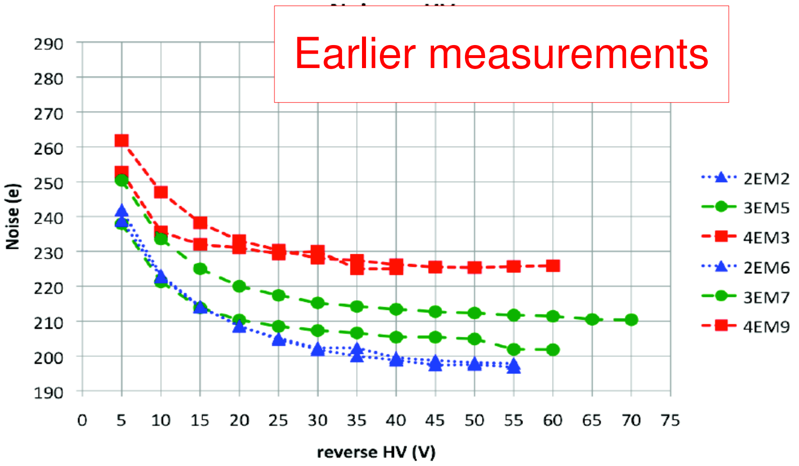
- Measure the noise (from threshold scan) as a function of the high voltage bias

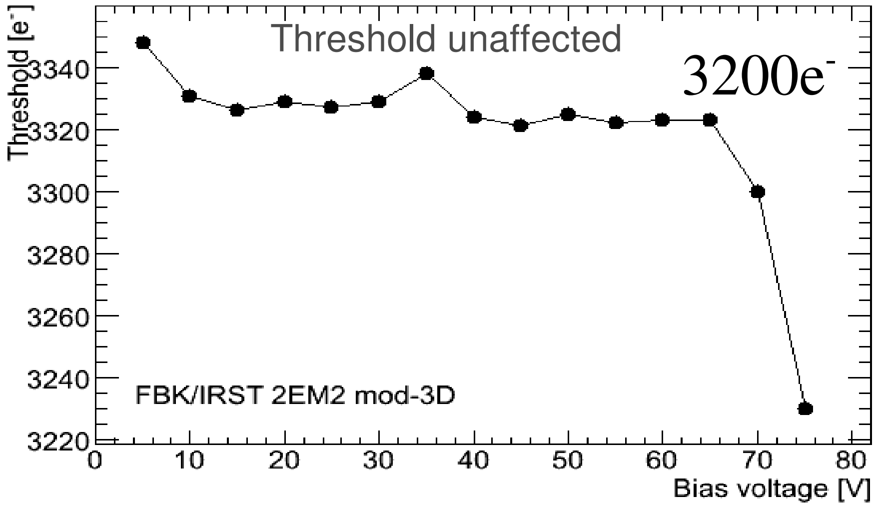


200e⁻@35V

- Consistent with earlier measurements
- Run-away at ~70V (as before)

  Earlier measurements up to 55V
- Fitted threshold plummets at ~70V

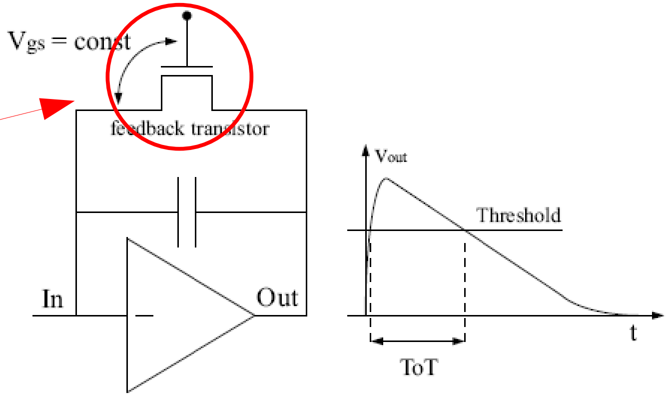

Earlier measurements


Threshold unaffected

3200e⁻

Time-Over-Threshold

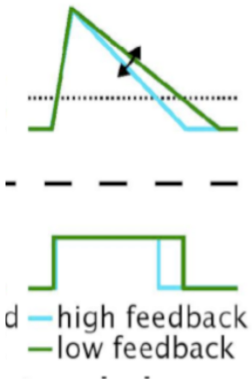
- Provides pulse height (indirect) information
- Depends on:
  - Deposited charge, Threshold, Feedback current



- FE pre-amplifier output is triangular
  - Constant discharge of capacitor
  - Time spent over threshold (appr.) ~ pulse height/charge

- Two step calibration
  1. ToT response to m.i.p. charge is made uniform by adjusting the feedback current
  2. Calibrate the ToT as a function of the charge (not done yet)

feedback current dependence



Repeat "X" times

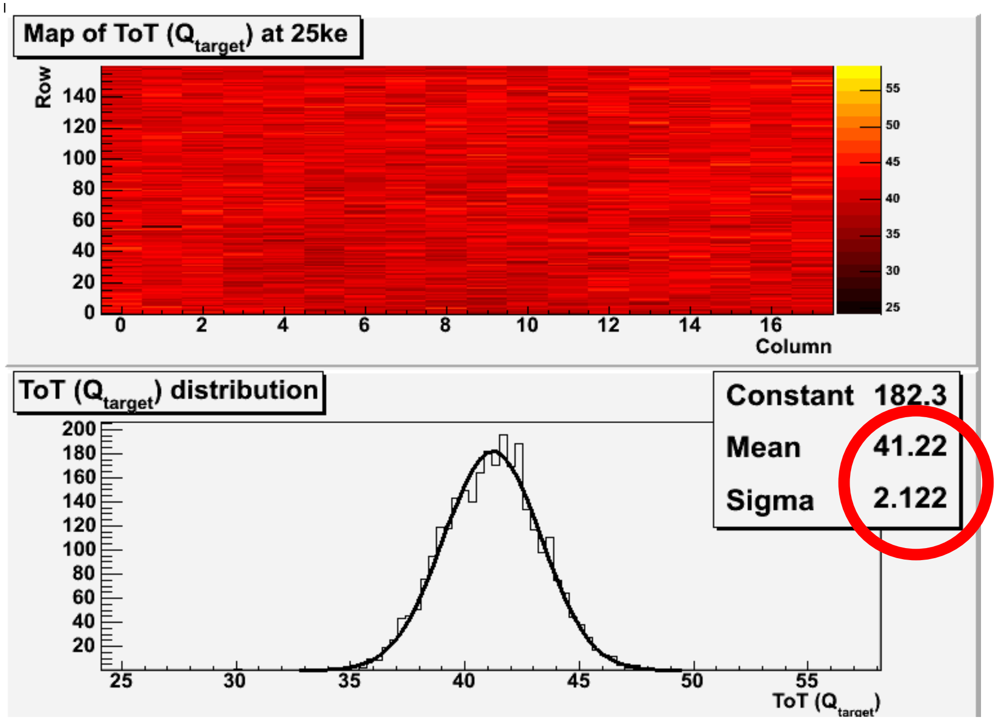
- Step 1:
  - Inject 20ke- (25ke-)
  - Adjust the feedback current so that average ToT is 30 (60) clock cycles
- Why 30 clock cycles in the current detector?
  1. Preamplifier output needs time to return to baseline
  2. Efficiency for large range of deposited charges

  ⇨ Gives "full" efficiency for approximately 4×(m.i.p. charge)

L1 Latency ~ 3.2μs
~ 128 clock cycles

Sensor Testing: ToT tuning

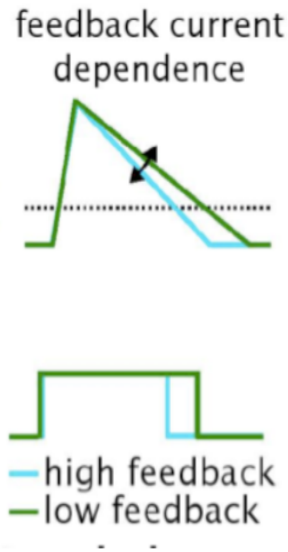
- On-chip “chopper” use capacitor(s) on each pixel to inject “known” charge
  - Two capacitors: C_{low}=8 fF and $C_{low}+C_{high}$=40 fF
  - Injected charge: $Q=VCal*C_{low}$ where VCal is determined from a X-bit number



- Tune by adjusting the feedback
  - IF
  - TrimIF
  - FDAC

IF, TrimIF } Per chip/”global”

FDAC } per pixel/”local”



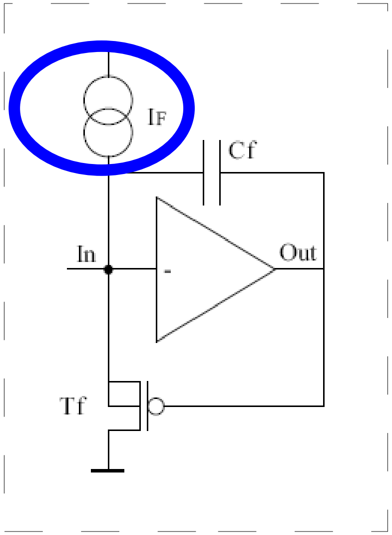
Using: 25ke- @ 60 ToT

Sensor Testing: feedback current

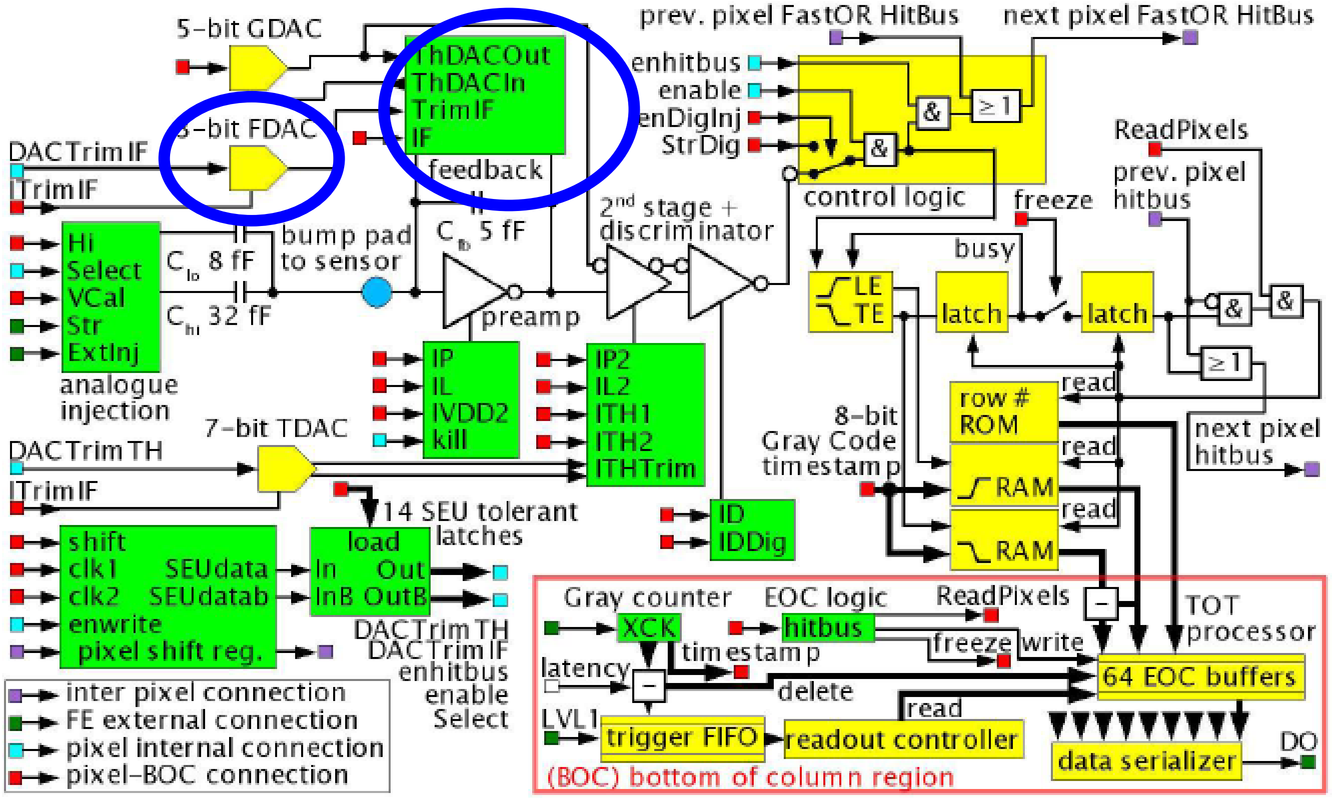
- Full FE is involved...

Global: **IF** (5-bit) Per Pixel: **FDAC** (3-bit)

TrimIF (5-bit)

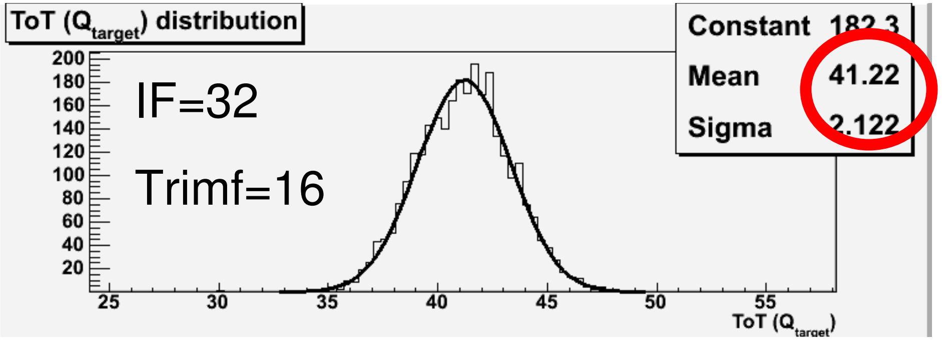


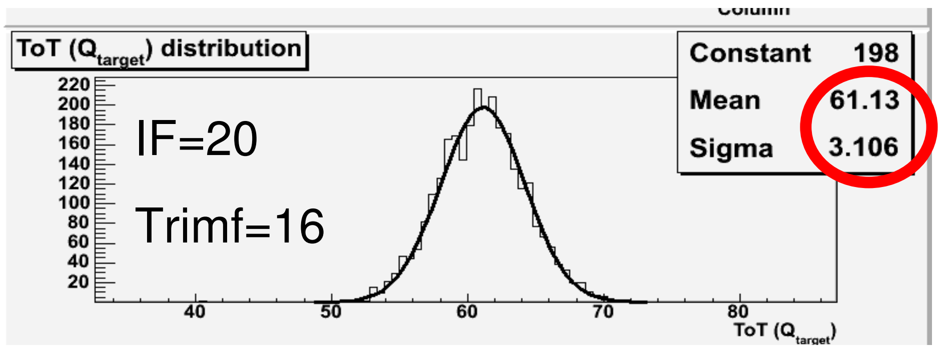
ATLAS Pixel FE channel schematic

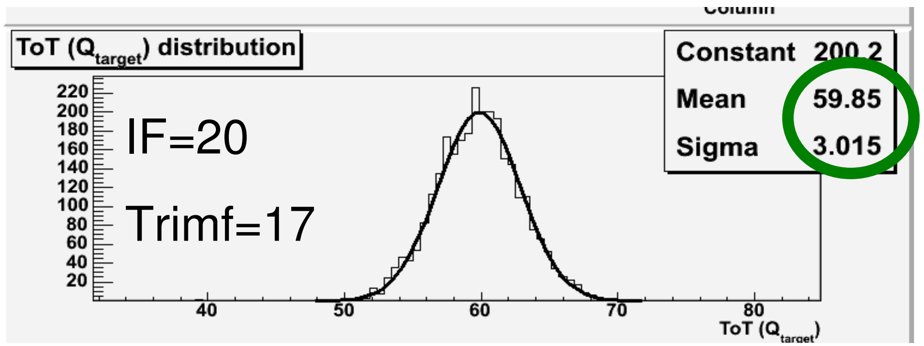


Sensor Testing: ToT tuning

- Some example distributions for different IF/TrimIF values (per FE)
  - FDAC/local bits unchanged

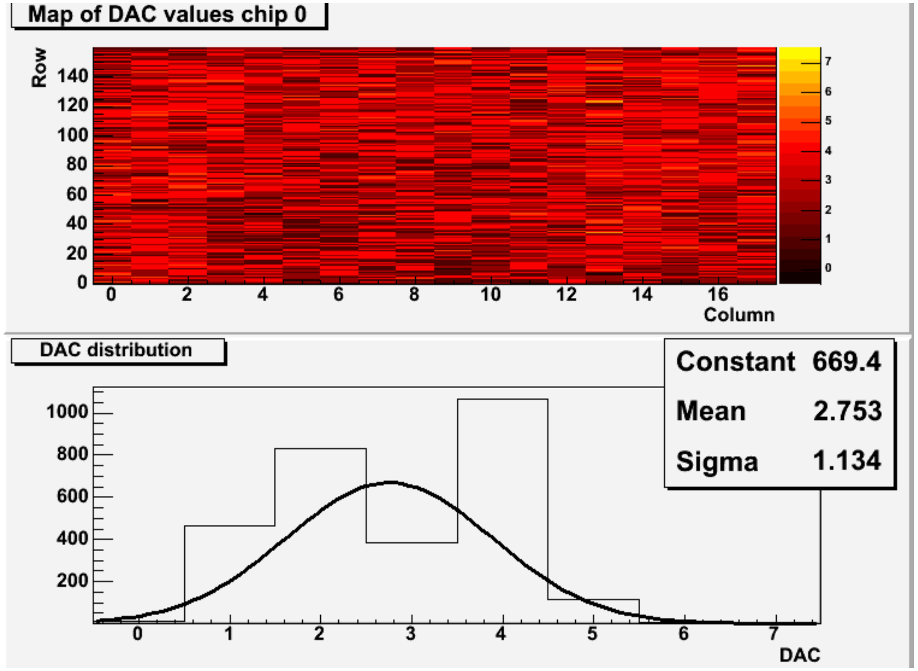


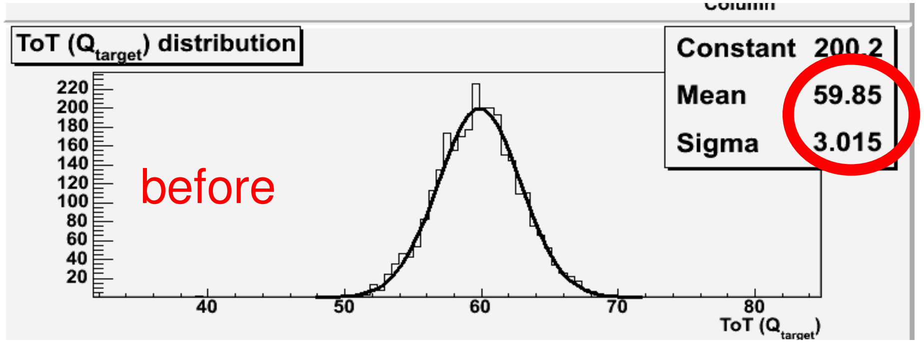


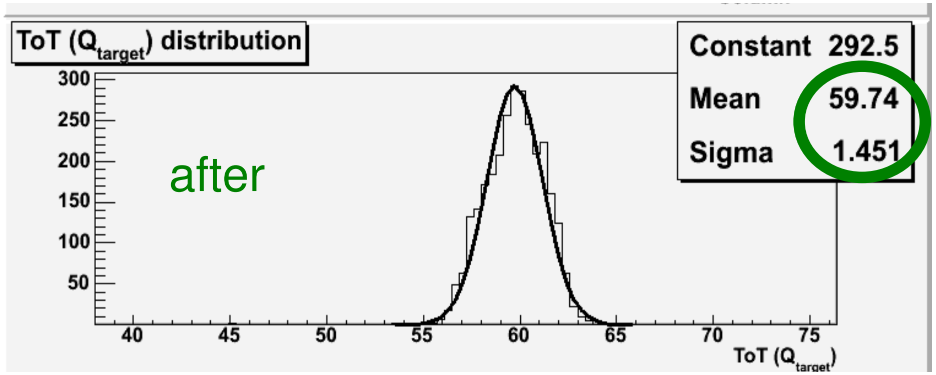


Sensor Testing: ToT (FDAC) tuning

- Tuning the FDAC bit per pixel – automatic scan







- Successful FDAQ tuning
  - Width of the ToT distribution decreases from 3.0 to 1.5

Expected width?

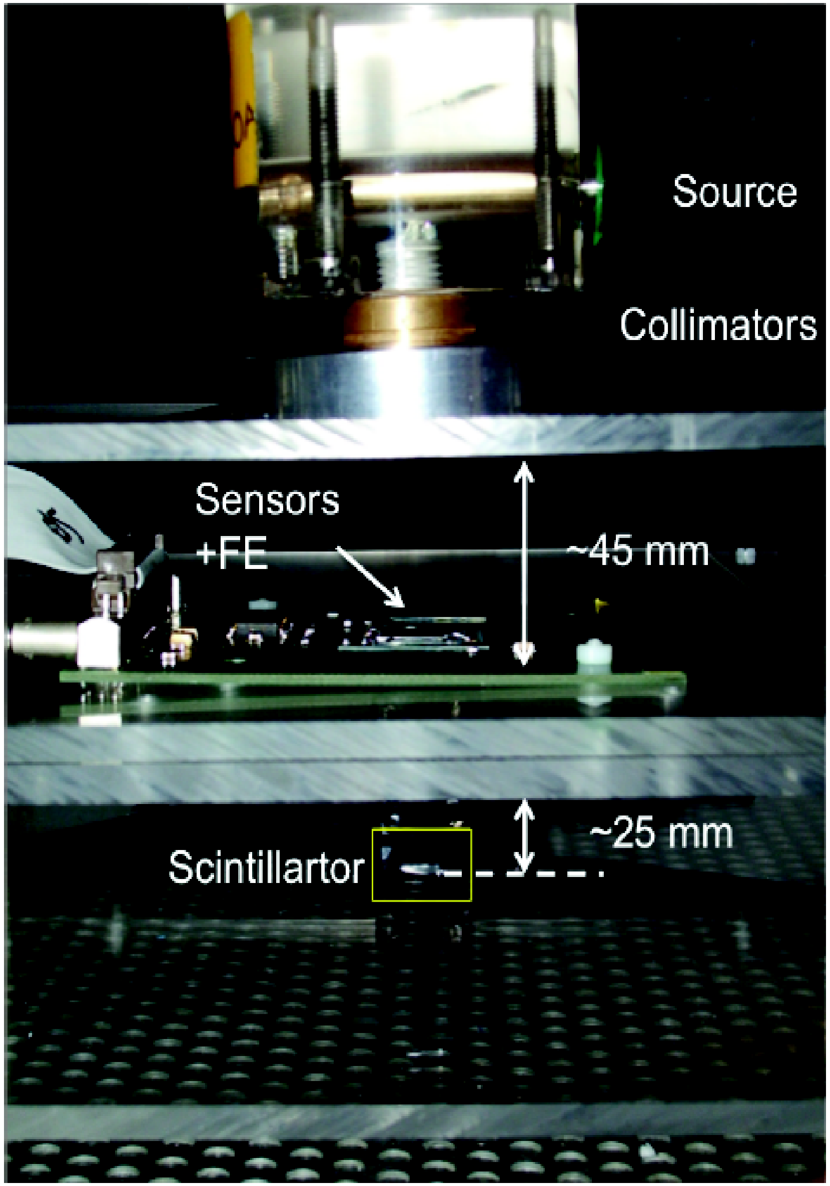
- 11 pixels had FDAC=0
  - Tuning out of range?
  - This happens in atlas pixels as well?

A. La Rosa/CERN

Source measurements

- Gamma source
  - Use sensor to reconstruct the lines of the source
  - Checks the calibration procedure
  - Requires no external trigger
  - Sources available: Am-241 and Cd-109
- mip tests
  - Checks the energy deposition and calibration
  - Is the Landau peak at the right place (compare e.g. Stanford and FBK/IRST)
  - Requires external trigger (scintillator)
- Lessons learned (1.5 days)
  - Check that there is no metallic plate between sensor and scintillator!!
  - Need to figure out how to use the planar as reference with metallic plate...

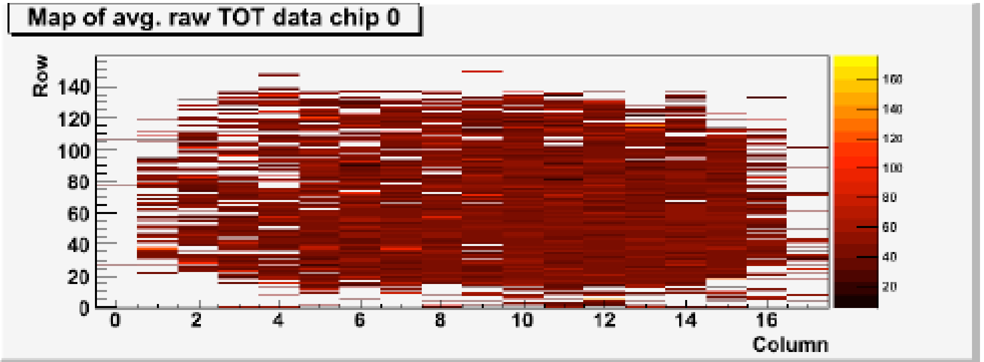
- Individual pixel show not “ideal” Landau
  - beam not collimated?

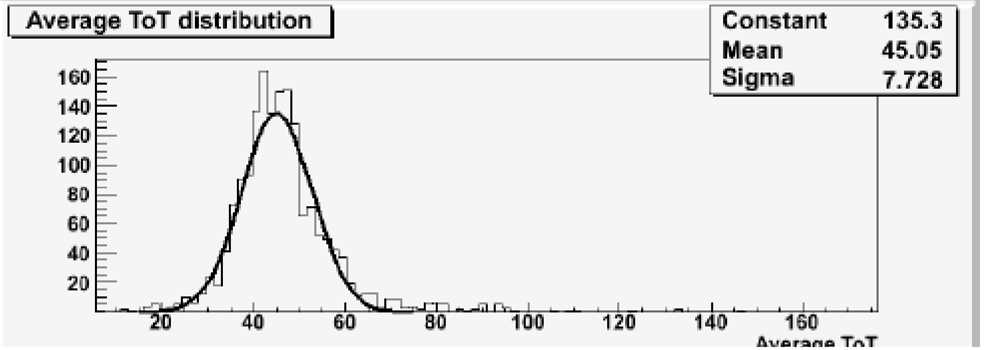


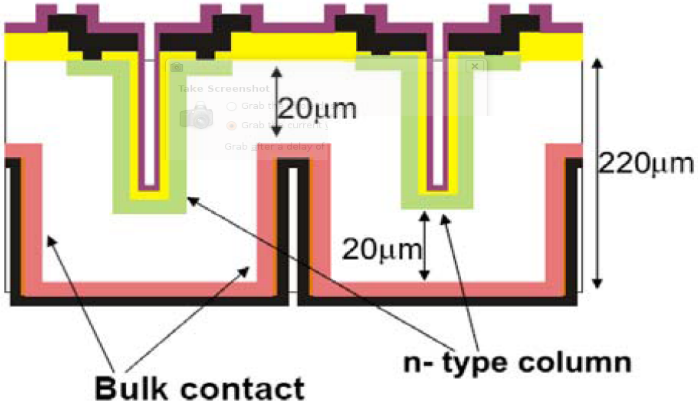
A. La Rosa/CERN

Source measurements

- Example
  - Sr-90 source and FBK-2EM2 type
  - Calibrated to 60ToT@mip
- Why peak at ToT=45
  - 3D column overlap is around 100um for the FBK-2EM2 (DDTC1)
  - Lost charges in low E-field regions?
  - Expect peak at 60ToT for full-3D...



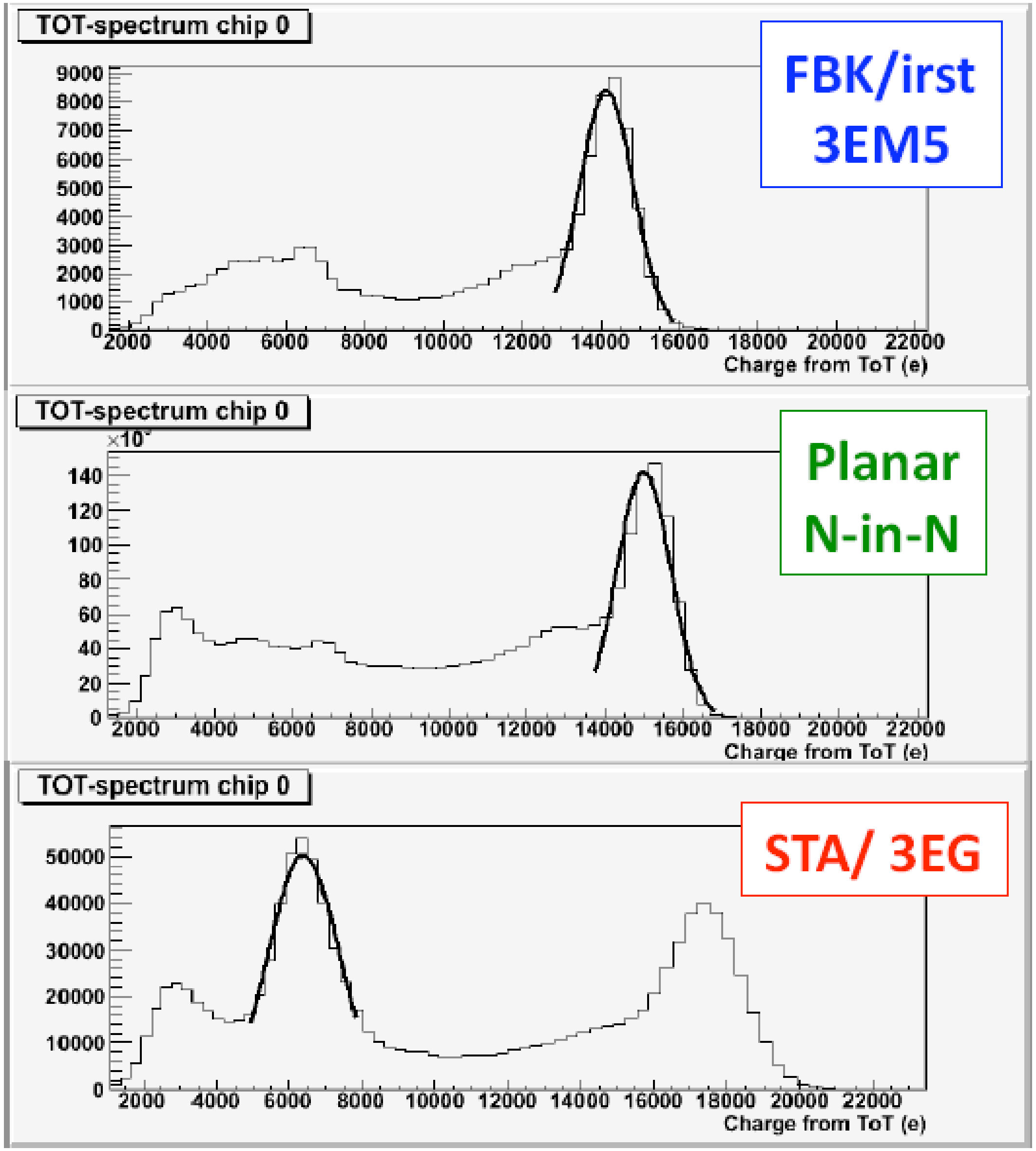




A. La Rosa/CERN

Source measurements

- Another example (Am-241 60keV peak)
  - Stanford 3D shows another peak
  - Why more prominent (only one STA/3D tested)?



Plans for lab-tests

- Test/learning activities
  - Calibrate the ToT as a function of the charge
    (Understand the external trigger delay settings in TurboDAQ)

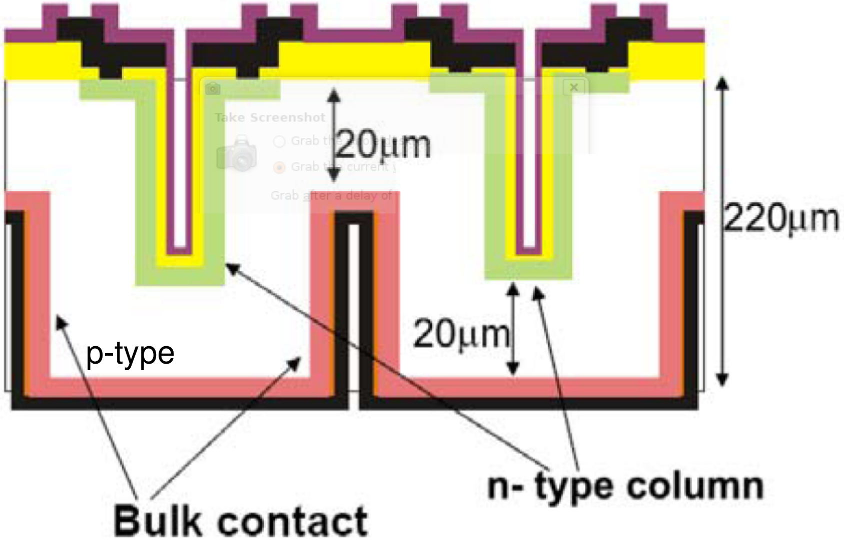
- 3D Stanford tests
  - "New" chips arrived to the lab: 2 and 4 electrode full-3D types
  - Will (I think) be used as reference in the test beam
  - Characterization starting this week
    - Find working point: threshold, ToT, noise, bias voltage, etc.
    - Source tests: gamma-sources (peak finding) + mip

Compare 2E,3E,4E

Backup

Mod-3D Sensors

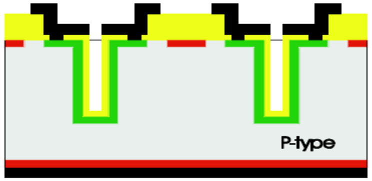
Double column, double type sensor



Not to scale

- Radiation hard
- Low depletion voltage
  - Increase E-field even after full depletion (see plot later)?
- Fast signal collection
- No support wafer needed
  - Depending on active edge...
- No active edge?
- Charge collection times in column tips
- Fabricated and tested
  - FBK/IRST (Trento)

- All very preliminary results are shown using this sensor
  - No particular reason except practical ones
- Bump bonded to ATLAS front-end chip
  - For upgrade and(?) IBL there will be a new front-end chip



Read-out both columns?

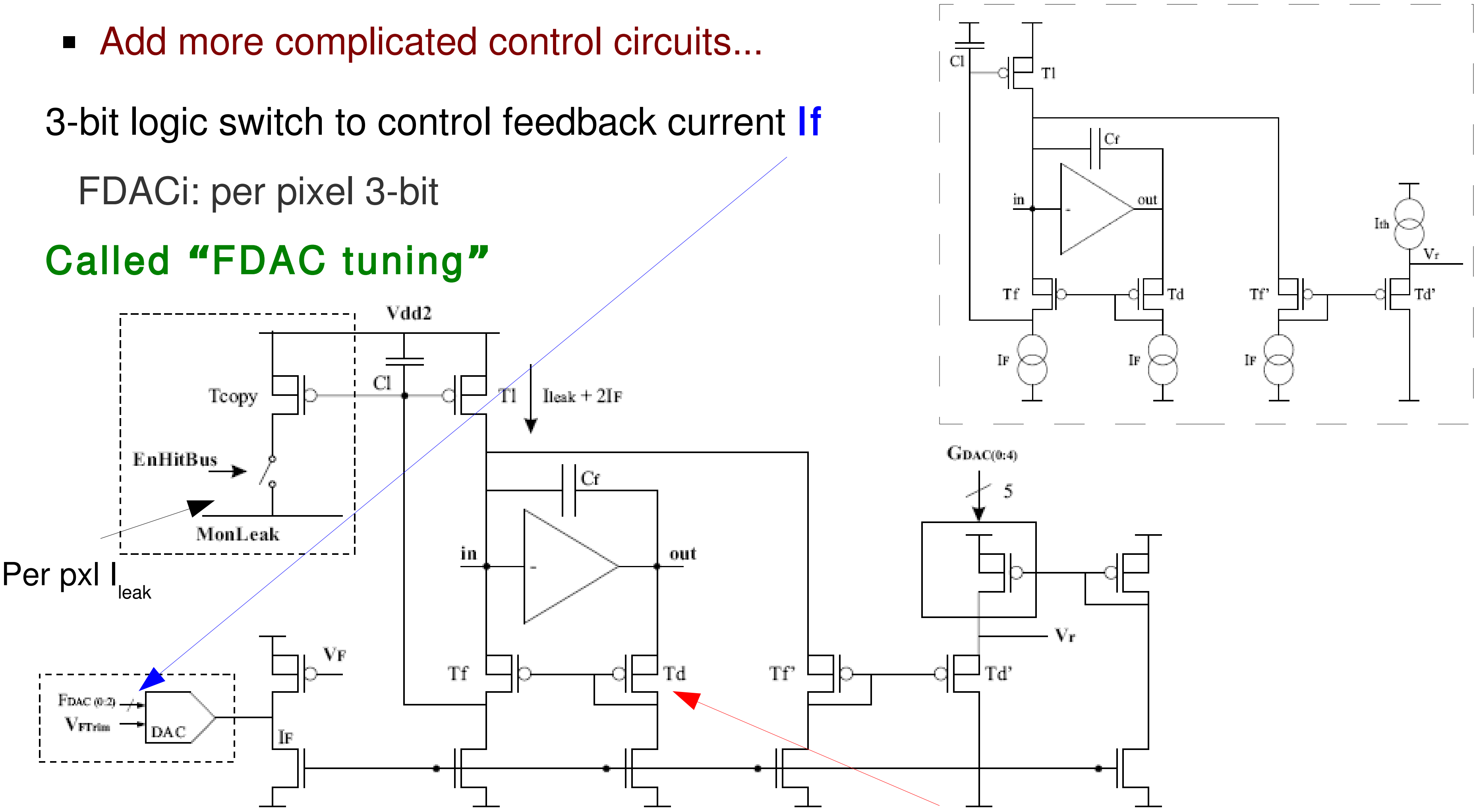
Sensor Testing: ToT tuning

- Add more complicated control circuits...

3-bit logic switch to control feedback current **If**

FDACi: per pixel 3-bit

Called "FDAC tuning"



Per pxl I_{leak}

8-bit logic switch to feed V_{Td}

Is this IF per FE chip?