

ABSTRACT

3D pixel detector system

In the next five years the LHC will be upgrade to become the super LHC, its performances will be increase. Even though LHC has not yet started, work on the upgrade of it has started. To reach this upgrade new technologies are contemplated.

Thanks to studies carried out at CERN and its partnerships, a new technology of detector was created. 3D pixel detectors may be used to replace the existing detectors situated in the experiments along the LHC.

The goal of my three months period in the Institute of Physic and Technology at the University of Bergen has been to study the 3D pixel detectors in order to build a measurement system to characterize them. We have chosen the TurboDAQ system. For the detector readout CERN laboratories advise us during the realisation of this project.

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INTRODUCTION

CERN have started planning research and development to upgrade the LHC to become SLHC in 2016. The luminosity will increase about a factor 10 to reach $10^{35} \text{cm}^{-2} \cdot \text{s}^{-1}$. Due to this, several experiments will need improvement and the ATLAS experiment will need a totally new inner tracker. Currently consist of silicon sensor the inner detector need a new higher technology.

3D silicon radiation detectors offer many advantages over planar detectors, including improved radiation tolerance and faster charge collection time.

Before choosing the new technology replacement, 3D pixel detectors have to prove itself and to be subjected to various tests.

The subatomic group in Bergen will participate in the characterization of this new technology. To do this a first step is to build a measurement system for this detector.

This report describes the construction of the 3D pixel detector system and shows the first characterization results.

The 3D pixel sensor

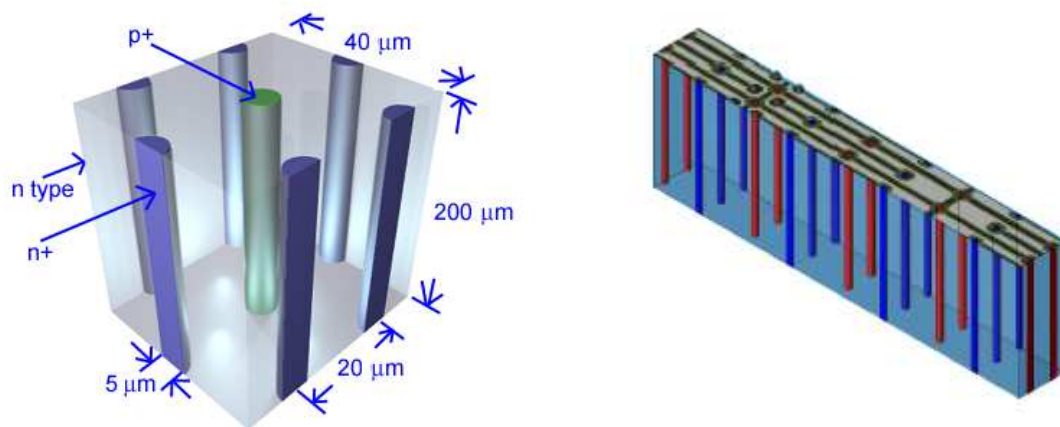


Figure A.1 : 3D pixel detector architecture

The 3D pixel detector consists of a silicon substrate with doped columns inside (cf. Figure A.1). This architecture is realized thanks to Micro Electro-Mechanical System (MEMS) and Very Large Scale Integration (VLSI) technologies. Deep Reaction Ion Etching (DRIE) is used to etch the columns. After that, a poly-silicon doped n^+ or p^+ filled the columns.

The sensors are processed on wafer, resulting in a size of approximately 1 cm^2 (cf. figure A.2). One of the companies producing these detectors is SINTEF, situated in Oslo, Norway.

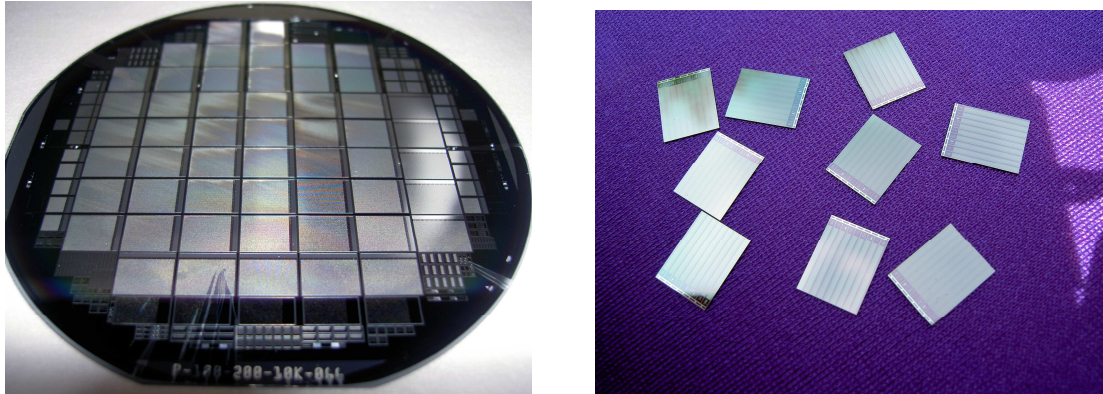


Figure A.2 : Wafer with 3D sensors

The principle of the 3D technology is simple, when a charge particle goes through the detector, electron-hole pairs are created and we observe readout current for both column types. This geometry result in many advantages compare to 2D planar detectors. (cf Figure A.3)

- **Active edge:** it is possible to etch columns very close to the edge
- **Fast signal collection:** e^- -hole pairs are created nearer to depleted area
- **Radiation hard:** Charge is collected faster
- **Low depletion voltage:** Depletion area is thinner

Moreover, the 3D pixel readout is the same than the current planar detector in ATLAS so it is easy to test these detectors and to replace the old technology by the new one.

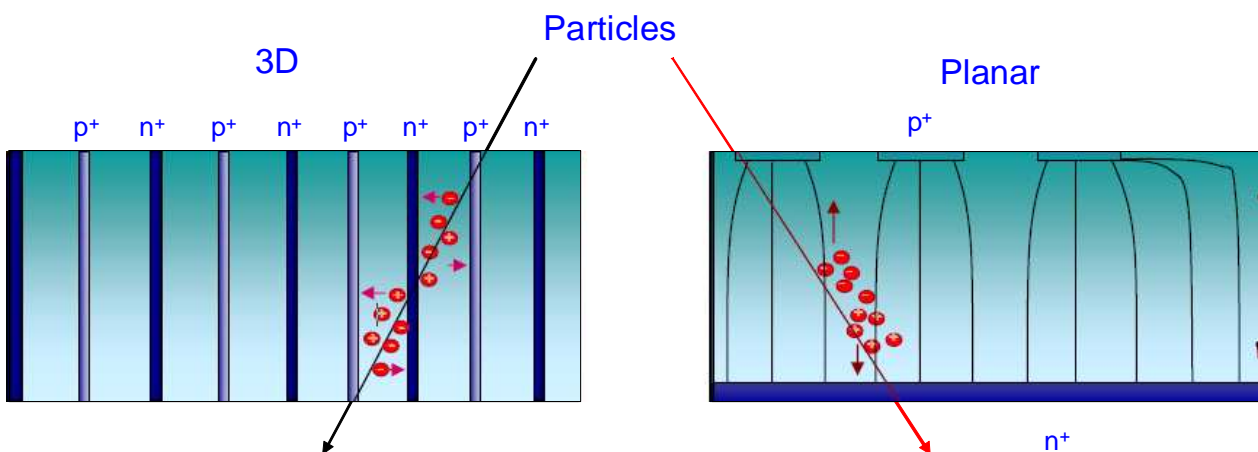


Figure A.3 : 3D detector compared to a planar detector

I. Construction of a 3D test system

In this part we explain each part of the system.

I.1. Global view

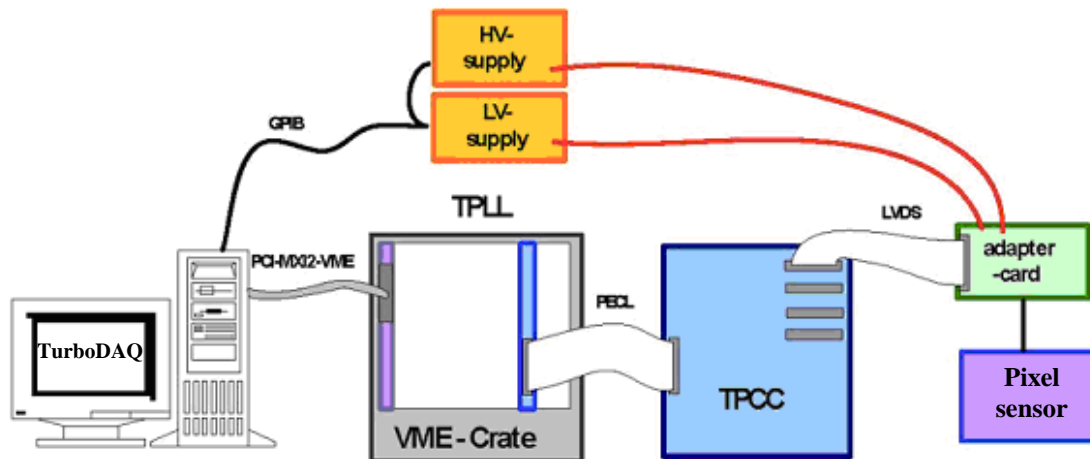


Figure I.1 : A schematic drawing of the 3D measurement system

As we can see on Figure I.1, the measurement system consist of one computer with software to pilot the system and treat the data, one VME crate with controller board and a board (TPLL) to clock the signal and transfer the data, one data acquisition board (TPCC), one electronic card to read-out the signal from the detector and three power supplies. Below is a list of the hardware and software components of this system:

- Computer HP with Windows XP machine: IFTSUB041088
- TurbDAQ 6.6 software
- PCI-MXI-2 National Instrument
- VME crate WES
- VME-MXI-2 controller National Instrument
- MXI-2 cable
- Turbo pixel low level card (TPLL)
- Turbo pixel control card (TPCC)
- 2 flat cables
- Front End electronic board
- 1 High power supply Keithley 487
- 1 Lemo cable with adaptor
- 2 Low power supply Oltronix B703DT
- 2 Shield cables for electric supply

I.2. The computer setup

We use a HP machine running under Windows XP, the number is IFTSUB041088. We have worked under the session “install” and the password has been “sinku050”.

We will see under that we install several software and driver on the computer to use the system.

I.3. PCI-MXI-2

A PCI-MXI-2 is plugged on the PCI slot 1 of the computer mother board. This card is the interface between the computer and the VME. The installation can be started from the following path:

- Computer properties
 - ↳ Hardware
 - ↳ Device Manager
 - ↳ VXI Interface

This opens the properties of the PCI-VXI card and under Driver tab we can upload the plug-and-play driver to start the installation of the PCI card.

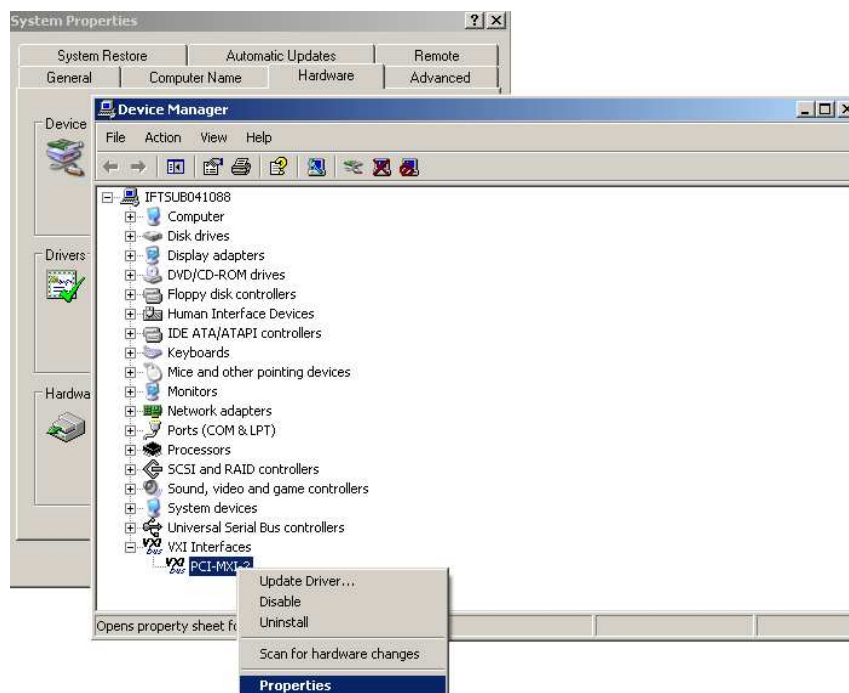


Figure I.2 : Device Manager Window

I.4. VME system

The VME controller board (cf Figure I.3), from National Instrument, has to plug in the first slot of the VME crate to control the VMEbus (Versa Modular Eurocard bus).

The connection between Computer and VME is carried out through MXI-2 cable plugged in PCI card and in the VME-MXI-2 controller board.

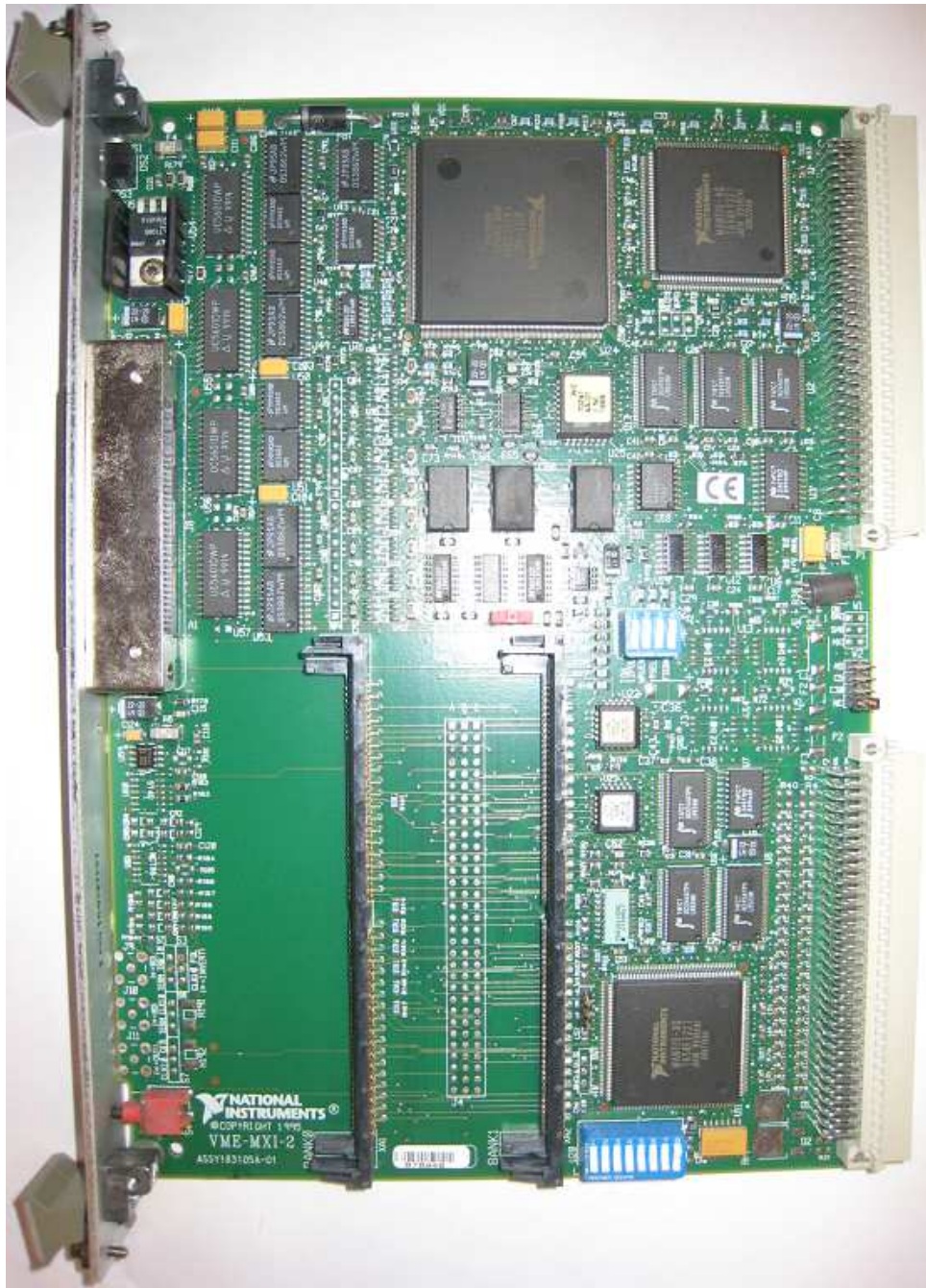


Figure I.3 : VME-MXI-2 Controller board

(Do not modify the switch on the board because it used in case of “controller board”, the switches U20 is used for slave mode of the board)



To communicate with the VMEbus via the MXI interface, we install drivers. The NI-VXI/VISA drivers include a Resource Manager, an interactive configuration and troubleshooting program, libraries of software routines for MAX programming.

First, switch-on the crate and check the led are lighted in the front of the board. Then you start the computer and launch MAX.

Shown in Figure I.5 is a screenshot from MAX, displaying how you launch the sub-routine “Resource Manager” (Resman). Tools >> NI-VXI >> VXI Ressource Manager

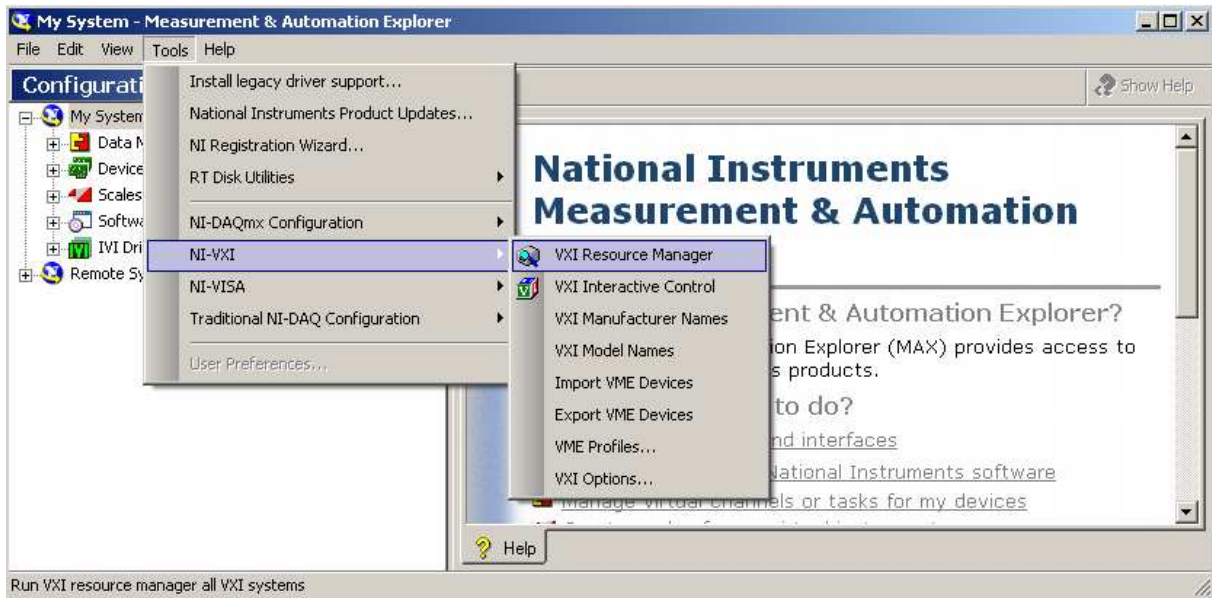


Figure I.5 : MAX screenshot of how to start Resman

After five second a tree configuration will appear in Devices and Interfaces (cf Figure I.6) and the PCI-MXI-2 card, the MXI-2 bridge and the VME controller appear when the drivers are properly installed. There is yellow exclamation mark on frame 1 due to the fact that our crate is VME, not VXI.

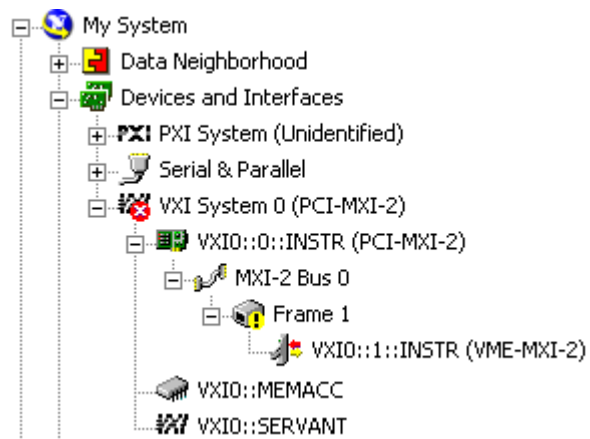


figure I.6 : Tree configuration

The next step is to add the TPLL board in this architecture. Right click on Frame 1 and click on “Create new VME device” (cf Figure I.7). A new window appears and by following the steps the device is installed.

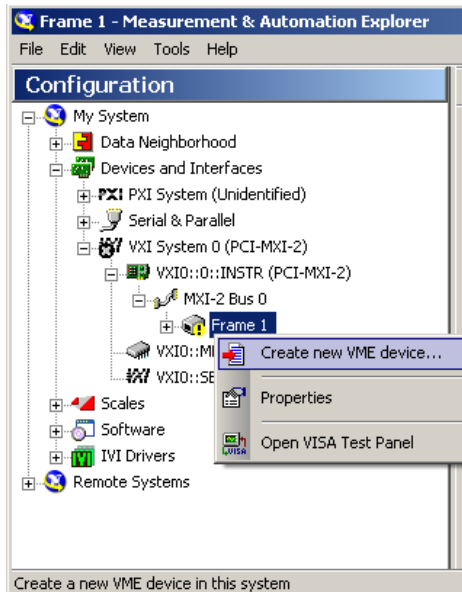


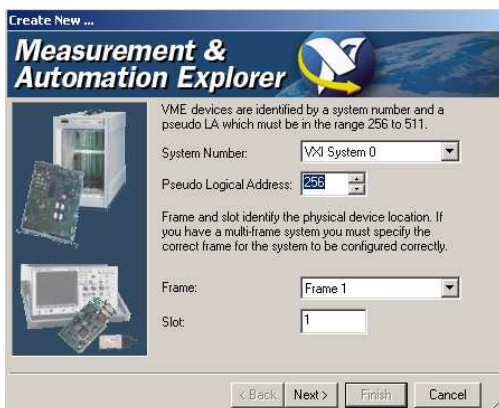
Figure I.7 : How to create a new VME device

The first step is to choose the pseudo logical address to “256” (cf Figure I.8.a). The logical address distinguishes between all the boards in the crate.

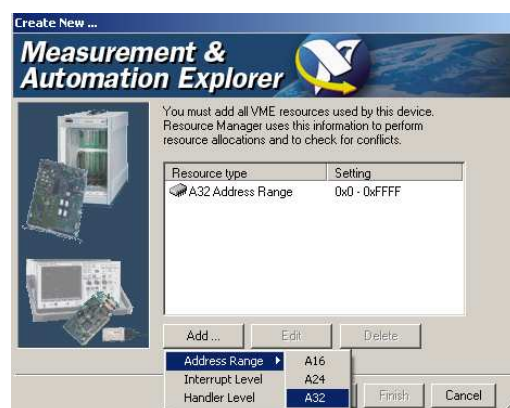
Next it is important to select Frame 1 in order to see TPLL in the same frame as the controller.

In the next windows we can choose either a new device or one already existing (Choose new device). The third step we enter a board name and a manufacturer.

The final step is to allocate free memory resources for the device (cf Figure I.8.b). For TPLL, we must select A32 address range and fill the “Setting” part with the TPLL resource. Currently the range is 0x10000000 – 0x107FFFFF.



(a)



(b)

Figure I.8 How to enter the parameters for a new VME device



At the end of this operation, the VME crate should be operational with the two boards inside and it should appear in the tree architecture in Figure I.9. Each device should have a correct resource memory.

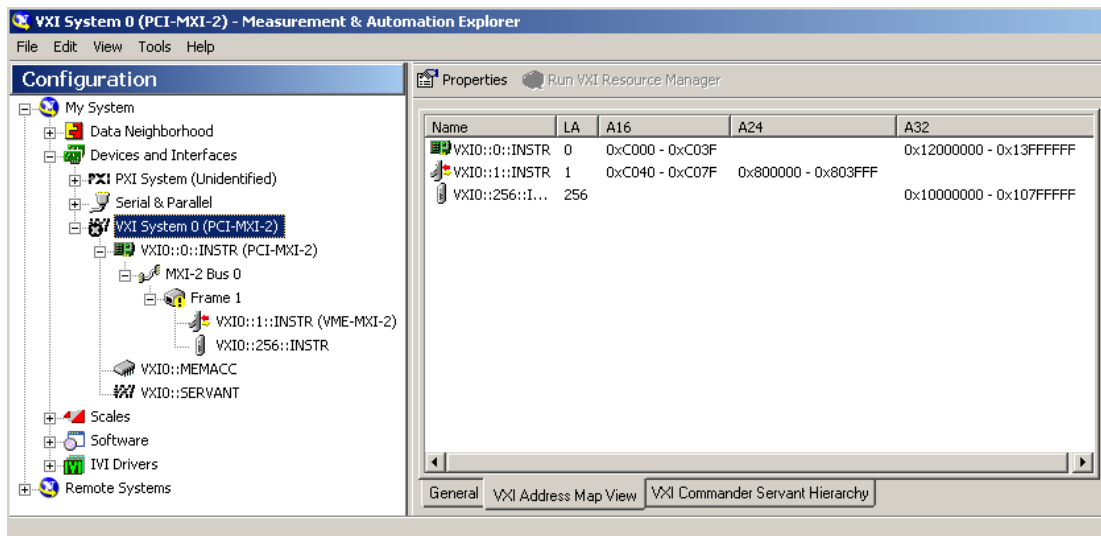


Figure I.9 : Final tree architecture

We can find all this information in the folder “3D Syst VME-MXI-2” on the desktop along with all the National instrument datasheets.

If the system needs another board (for example: cooling system), follow the same procedure to add it, but be careful to change pseudo logical address and address range (A32 0x1000...)

I.5. TPCC board

Now we are ready to plug the multicolor flat cable between the TPLL and the TPCC board (cf Figure I.10). This bridge transfers the data to the TPLL which convert it to be transmitting on the VMEbus.

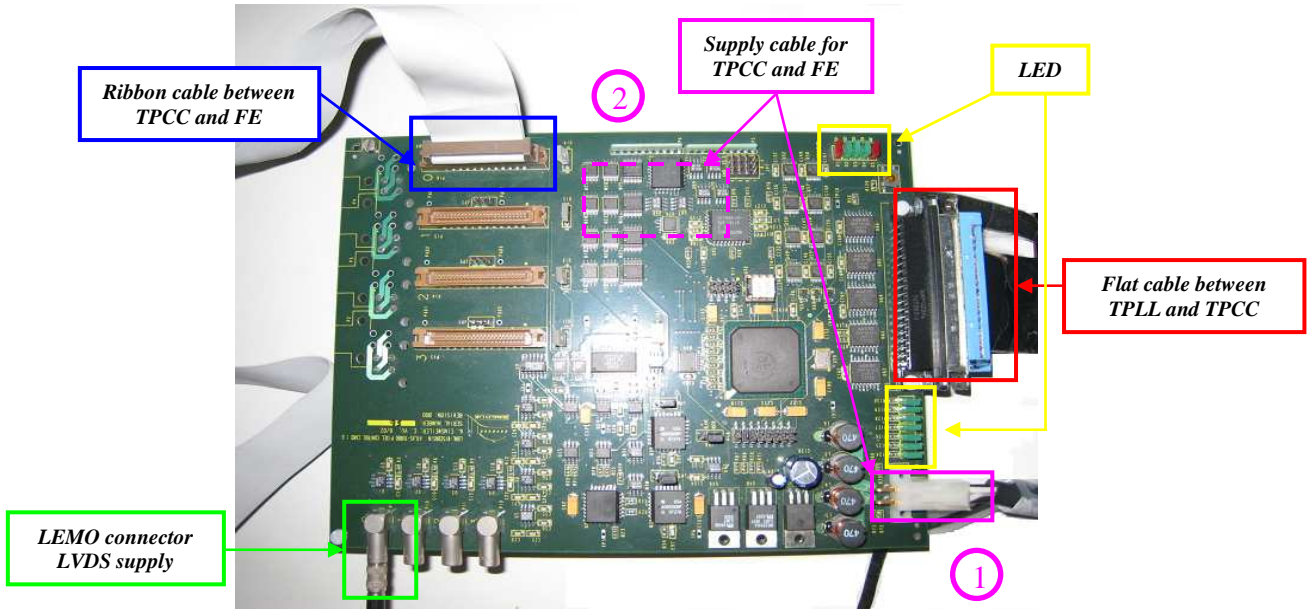


Figure I.10 : TPCC board

Contrary to TPLL board which is supplied through the VME crate, the TPCC card need four different power supplies, two digitals and two analogues. These supply the board and a part of the Front end electronic card. Two shield cables with Molex connector could be used.

Figure I.11 show the two connectors plugged in TPCC. ① TPCC supplies the TPCC board; it is connected near the multicolor ribbon cable. ② FE connector is plugged on the TPCC back and supply the Front end card.

Be careful with the power, both voltage and current it is very important to check it and respect the voltage.

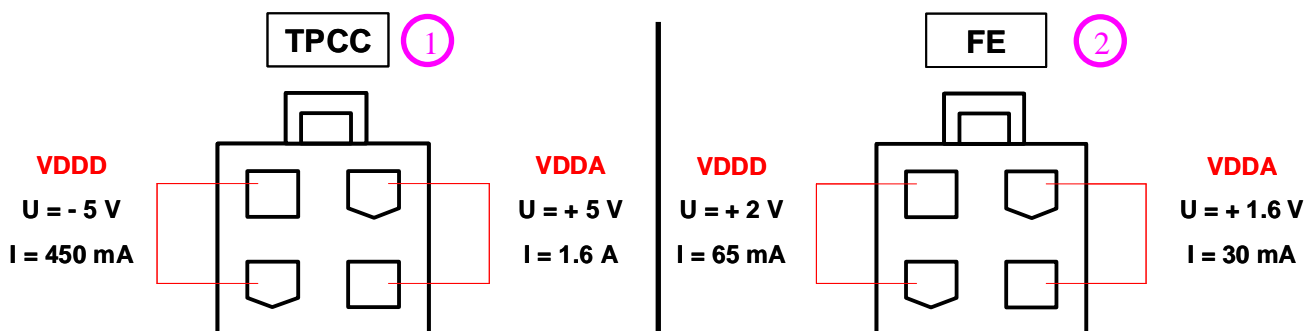


Figure I.11 : Front of the Molex connector and supply values for the two supply cables

I.6. Front End electronic card

The 3D pixel sensor is connected to the FE readout electronic using a complex soldering technique called “Bump bonding”. It needs a great accuracy; each pixel must be connected to each FE readout plot (cf Figure I.12).

Such system is located in Bonn and the 3D sensors from SINTEF are bump bonded there.

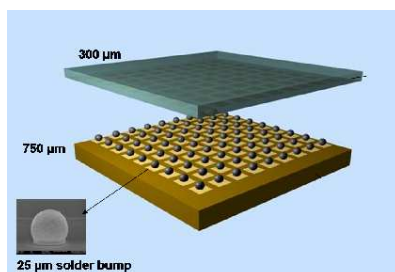


Figure I.12 : Bump bonded

The electronic board where the 3D detector is bump bonded contains tunable components in order to select the best parameter for each pixel.

Shown in Figure I.13, the 3D sensor is in the middle of the card. At the left there is the high voltage supply to deplete the sensor. To the right, there are the ribbon cable connection to plug this from the TPCC and a LEMO cable. The calibration signal goes through the LEMO cable from TPCC too.

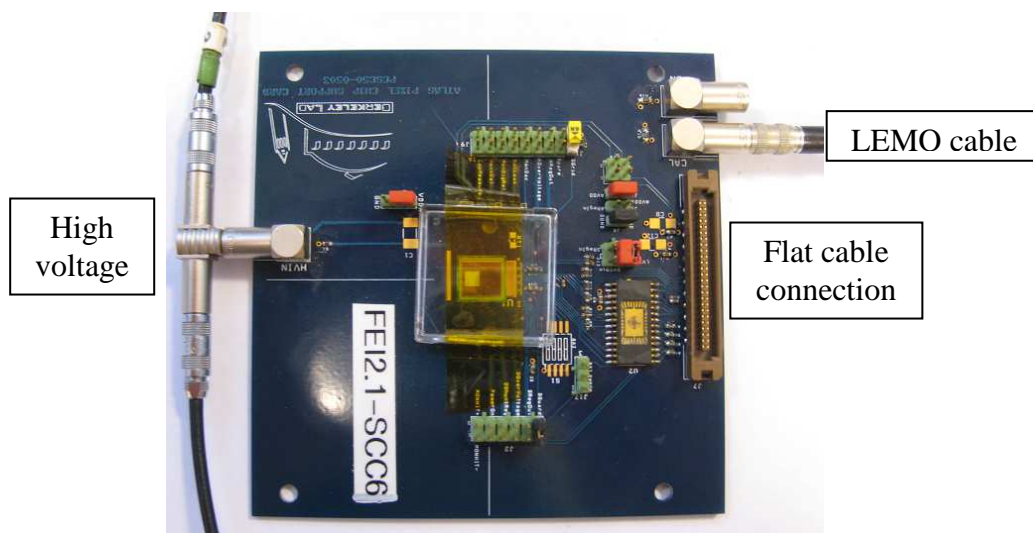


Figure I.13 : Front End electronic board

We have to be careful with the high voltage applied. The value depends on the pixel sensor type but it is always negative. For example to deplete a 3D pixel detector we supply around -30 volt instead of more than -100 volt for a 2D pixel sensor. So we add voltmeter in parallel to check this voltage.



II. TurboDAQ

The software TurboDAQ is installed on it. Currently the release 6.6 is running and all the instructions to download and to install this software are given on the Web page:

<http://pixdata.lbl.gov/html/TurboDAQ.htm>

This software permits to pilot the data acquisition and display the readout from the pixel detector. It is written in CVI language, so we need the software LabWindows CVI from NI. Currently the release 8.5 of CVI is installed on the computer. All the files concerning the software are in the folder named TurboDAQ on the desktop of the computer

II.1. TurboDAQ start

To launch the program double click on the shortcut “TurboDAQ.exe” on desktop. On Figure II.1 we observe the TurboDAQ main panel.

This panel contains all the functions that we can use with this software, but in the case of pixel sensor measurement we do not use all the tabs. Below we will describe the functions and explain the procedure used to carry out measurements.

After switching on the VME crate and the computer, “resman” needs to be launched to configure the VME bus. After that we can start TurboDAQ.

The TPCC can be powered either by an independent power supply or with a GPIB power supply linked to the computer. In the first case we adjust the voltage and current button by hand and on the second case we can open the Power console panel in TurboDAQ to tune which supply we want. In both case six LEDs near the supply connector number 1 must light and two others above the multicolor flat cable. (cf Figure II.2)

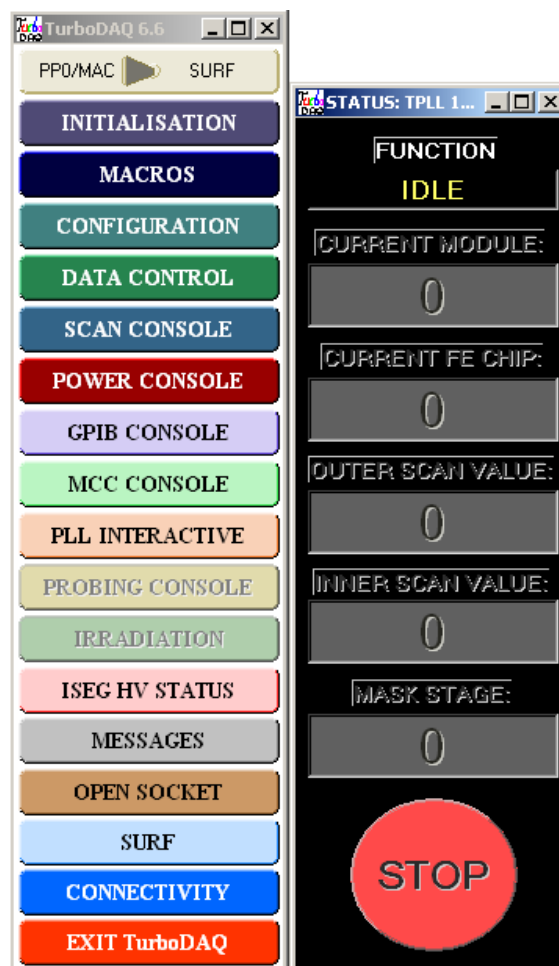


Figure II.1 : TurboDAQ main panel

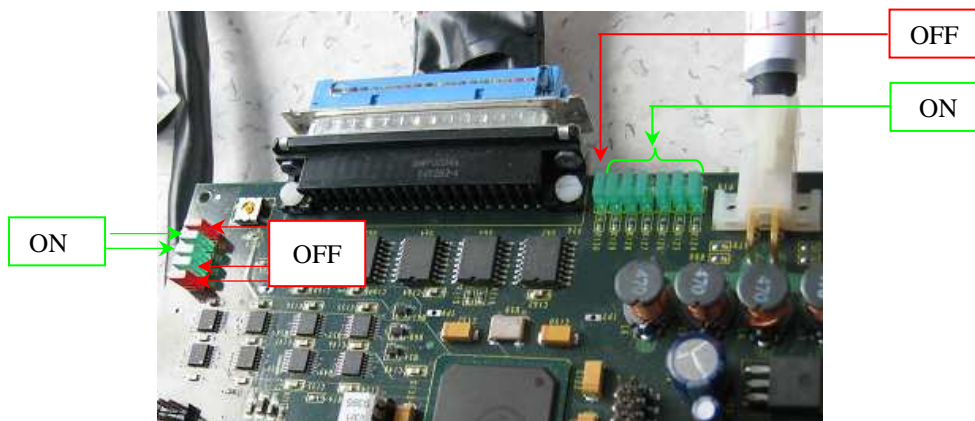


Figure II.2 : TPCC lights

If the TPCC LEDs are correctly light we open the Initialise PLL&PCC panel and push the button “Reinitialise”. If all the supply and configuration are correct, we will observe the two lights on the right of the Figure II.2 shutting down and a new orange LED switching on near the FE flat cable. Moreover the values in the Figure II.3 appeared, else an error message appears.

When this is all correct, start fitting the other panels with the necessary parameters.

First, open “Configuration” in order to define the parameters of the measurement (cf Figure II.4). Enter the assembly type and the name of the module in “Module identifier”. In case of 3D pixel single chip used, unchanged “PCC/PICT”, “Strobe setup” and “Trigger setup” values. Then select F for the “Global Address” (GA) and fill value for each parameter. A good idea is to modify them one by one and make a scan to understand their effect. After this, we can start all the three tests at the bottom of the panel, “Send module configuration”, “Test global registers” and “Test pixel registers”. The red light in the right corner must shut down and the black light must become green, else there is problem and an error message will appear. Concerning the temperature, the new TPCC board should show the correct value.

We can fill TDACS and FDACS parameters with an already complete file by a previous scan if you click on the white square just below but we will see later in this rapport.

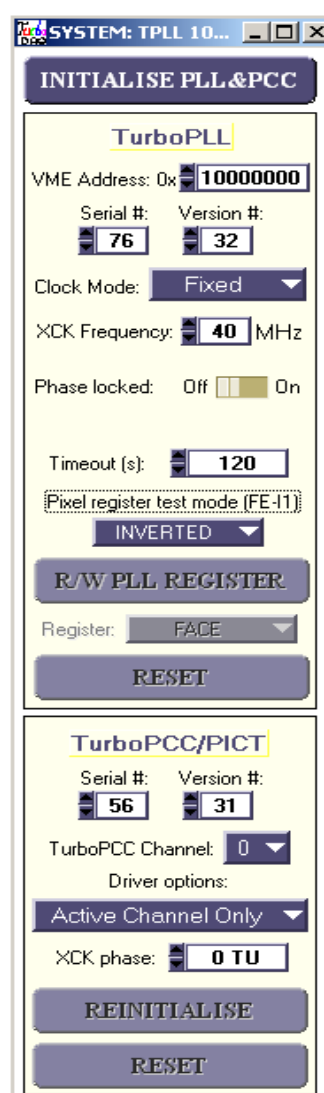


Figure II.3 : Initial panel



STATIC CONFIGURATION CONSOLE: TPLL 10000000, Module FE2.1-SCC

MODULE CONFIGURATIONS: ASSEMBLY TYPE: Front-End Single Chip Assembly (SCA) | MODULE IDENTIFIER: FE2.1-SCC

ADVANCED FUNCTIONS: SHOW STATIC MASKS AND TDACS | MASK MAKER

STROBE SETUP: DURATION: 500 | INTERVAL: 500 | MODE: Analog Internal | LE DELAY: 0 | TE DELAY: 0

TRIGGER SETUP: DELAY: 116 | CONTIGUOUS LVTS: 16 | PLL MODE: Internal | Normal | Lemo

FE CHIPS: TYPE: FE-12/3 | VCAL: 511 | LATENCY: 128 | PHI: 40MHz | ONJ: Low | MON MUX: Hitbus | HITBUS: On | TOT MODE: No Thresh | MIN TOT: 0 | TWALK TOT: 32 | 8-Bit TOT no Parity

FE CHIPS	TYPE	VCAL	LATENCY	PHI	ONJ	MON MUX	HITBUS	HITBUS	TOT MODE	MIN TOT	TWALK TOT	8-Bit TOT no Parity
0	F	64	64	64	64	64	32	16	0	0	64	64
1	1	64	64	64	64	64	32	16	0	0	64	64
2	2	64	64	64	64	64	32	16	0	0	64	64
3	3	64	64	64	64	64	32	16	0	0	64	64
4	4	64	64	64	64	64	32	16	0	0	64	64
5	5	64	64	64	64	64	32	16	0	0	64	64
6	6	64	64	64	64	64	32	16	0	0	64	64
7	7	64	64	64	64	64	32	16	0	0	64	64
8	8	64	64	64	64	64	32	16	0	0	64	64
9	9	64	64	64	64	64	32	16	0	0	64	64
A	A	64	64	64	64	64	32	16	0	0	64	64
B	B	64	64	64	64	64	32	16	0	0	64	64
C	C	64	64	64	64	64	32	16	0	0	64	64
D	D	64	64	64	64	64	32	16	0	0	64	64
E	E	64	64	64	64	64	32	16	0	0	64	64
F	F	64	64	64	64	64	32	16	0	0	64	64

MODULE TEMPERATURE: -888.80 C | UPDATE

Figure II.4 : Configuration panel

Next we open the “Data control” panel (cf Figure II.5). The only thing to do in this panel is to fill in the name and the date of the measurements.

DATA: TPLL 10000000, Module FE2.1-SCC

ACQUISITION: DFIFO Direct | 8-bit Histograms

Event Filter Off

OPTIONS: Ignore Errors | Accept All Hits

OUTPUT/FITTING OPTIONS:

- RAW HITS: OFF
- ALL BINNED HITS: OFF
- BINNED TOT: OFF
- S-CURVE FITS: OFF
- TOT CALIBRATION: OFF
- TDACS: OFF
- FDACS: OFF

DESTINATION: Relative path

MFE2.1-SCC/data/

Prefix: 2008-11-10

Status: Set 1 Test

Custom description for logfile (260 chars max)

FITTING CONSOLE

Figure II.5 : Data control panel

At the bottom of this panel there is a button called “Fitting console”. This opens a new panel (cf Figure II.6) where we adjust threshold value.



DATA FITTING CONSOLE: TPLL 10000000, Module FE2.1-SCC

CALIBRATION FE calibration data file:

External VCAL (mV/count): Custom global scale: Custom/External offset (DAC units):

FE Index:

Cinj-LO/mF	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60	4.60
Cinj-HI/mF	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7	41.7
VCAL/mV	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600	1.5600
Offset/e-	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

S_CURVE FITTING $f(Q) = \text{Error Function}$ Plateau: Chi-squared cut: Method:

TOT CALIBRATION $f(Q) = A + B/(Q+C)$ Initial Guess: A: B: C:

THRESHOLD TrimDAC (TDAC) DETERMINATION: Target Threshold: e-

FEEDBACK TrimDAC (FDAC) DETERMINATION: Match to TOT counts at e-

IN-TIME THRESHOLD: obtain chip/module mean T0 from

Mean T0 strobe delay / ns Adjusted T0 strobe delay Range was Trigger delay was Adjustment / ns

<input type="button" value="PERFORM S-FITS"/>	<input type="button" value="PERFORM TOT CALIBRATION"/>	<input type="button" value="DETERMINE TDACS"/>	<input type="button" value="DETERMINE FDACS"/>
<input type="button" value="WRITE S-FITS"/>	<input type="button" value="WRITE TOT CALIBRATION"/>	<input type="button" value="WRITE TDACS"/>	<input type="button" value="WRITE FDACS"/>

Figure II.6 : Data fitting console

In this panel we choose the target threshold for all pixels in units of electrons and the characteristic values of the FE, the capacity (Cinj-LO and Cinj-HI) and the calibration voltage which are used to tune each pixel. We must be careful with the “Feedback TrimDAC” because the value must stay around 25000 e⁻ for the measurement. Sometime, when we tune other parameter this value returns to the default value of 10.

The last panel to open is “Scan console” (cf Figure II.7). It permits to choose what scan to from a list and to launch it.

Click on the blue square button next to “SCAN CONFIG” to choose the scan you want. The most important scan is the “threshold scan internal cal” (with internal calibration).

The goal for this scan is to obtain the same threshold from each pixel as well as the electrical tuning of each pixel.

When we select threshold scan, this panel is configured by itself. We just change the scan option by selected “No LV/HV Supply Measurement” in order to do not waste time to measure the voltage supply.

At this moment we can click on “Online plot” to see immediately the results (cf Figure II.8) and launch the measurement with “Start scan”.

The threshold scan run only one minute, the 32 mask unfolds. Measurement carried out, we observe on the pixel map the threshold value. And we can modify the “Plot Mode” to view the mean Gaussian or the S-curve.

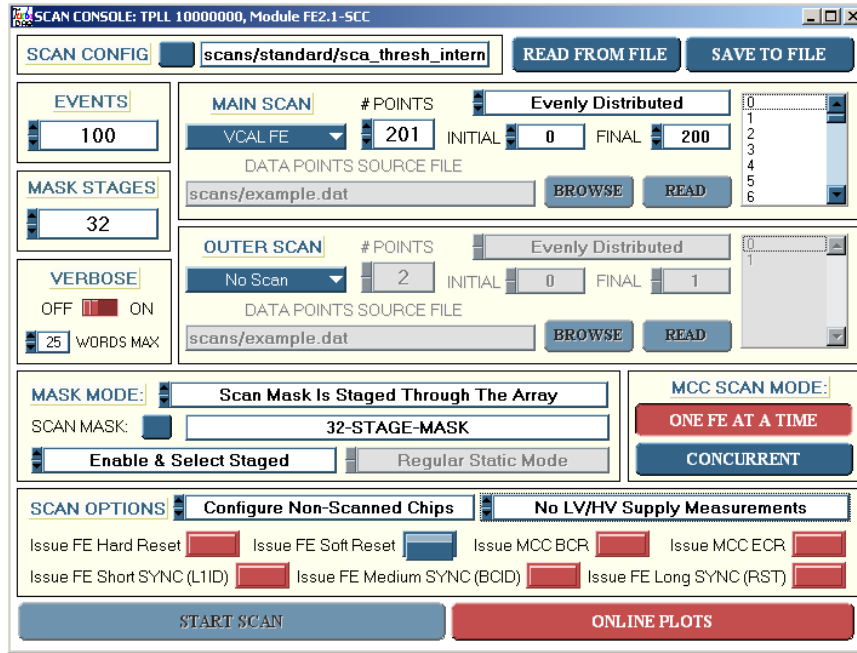


Figure II.7 : Scan consol

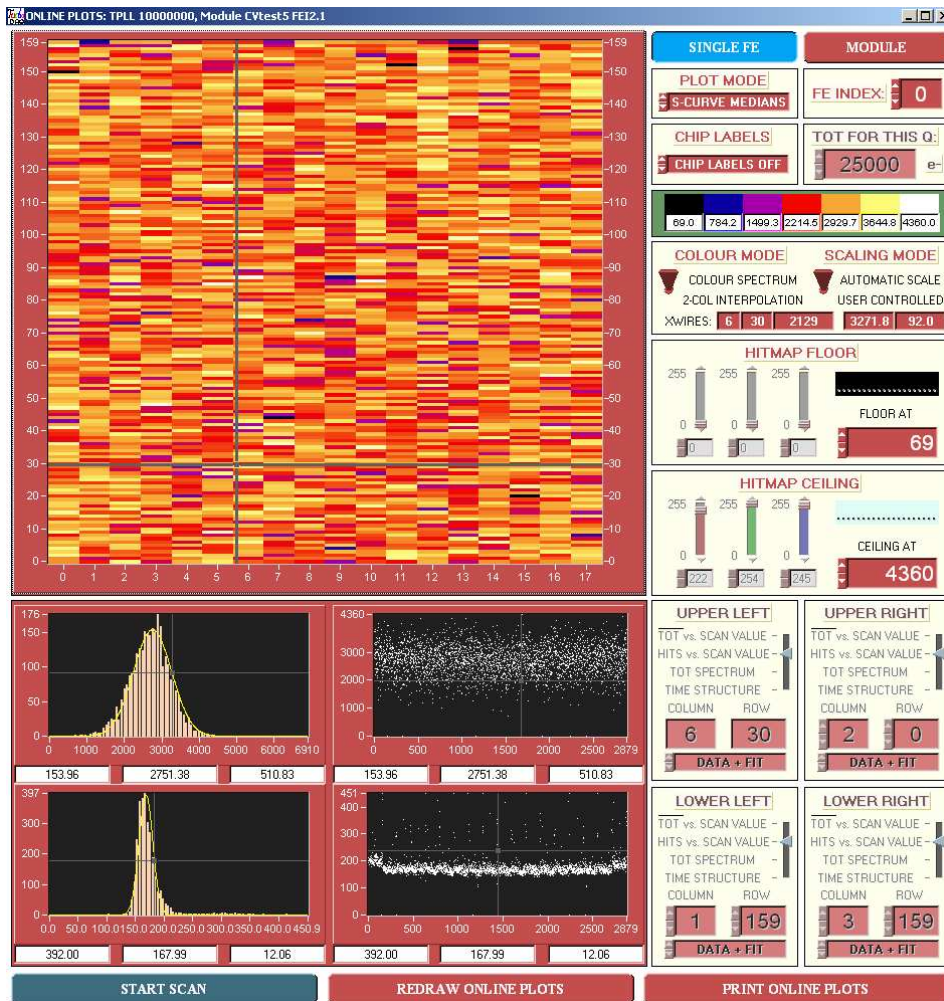


Figure II.8 : Online plot



II.2. TurboDAQ threshold calibration procedure

Before used radioactive source to send particle on the detector, we have to calibrate it. Indeed, each pixel must be tune to obtain the same threshold on the entire sensor surface, thus the detector will be efficient.

By following this procedure the pixels are tuned:

- 1) As it is written before, set the parameters and carried out the first “Threshold Scan, Internal-Cal”
- 2) Modified the parameters (for example : GDAC) until to obtain the best first Threshold scan, that is to say, mean threshold value the nearest to the target value enter in “Data fitting”
- 3) With this parameters run the scan “TDAC Tune, Internal-Cal” to obtain the first TDAC scan and the file “*namefile_tdacs_0.out*”.

All the files will store in the directory

“C:\Documents and Settings\install\Desktop\TurboDAQ\TurboDAQ_files*detector-name*\data”

In order to not erase the previous file change the Prefix name under the panel “Data control”

- 4) In “Configuration panel” set TDAC parameter, by clicking on the white square and upload the file “*namefile_tdacs_0.out*”.
- 5) Carried out the second threshold scan and observe the improvement.
- 6) With this changes run the scan “FDAC Tune, Internal-Cal” to obtain the first FDAC scan and the file “*namefile_fdacs_0.out*”.
- 7) In “Configuration panel” set FDAC parameter, by clicking on the white square and upload the file “*namefile_fdacs_0.out*”.
- 8) Carried out the third threshold scan and observe the improvement.
- 9) With this changes run one more scan “TDAC Tune, Internal-Cal” to obtain the second TDAC scan and the second file “*namefile_tdacs_0.out*”.
- 10) In “Configuration panel” set TDAC parameter one more time, by clicking on the white square and upload the second file “*namefile_tdacs_0.out*”.
- 11) Carried out the fourth threshold scan, we should obtain an uniform pixel map. Check the threshold mean value and the noise in the file “*namefile_logfile*”
- 12) Under “Configuration panel” click on “Module configurations”, fill Channel 0 with a name and save the configuration.

Now we can use this configuration each time we use the FE with the detector bump bonding on it.

We have to carry out this procedure each time we study a new detector system.

III. First results with 3D system

During the installation of Bergen system we possessed two FE. The first one, FE 4E-B, with 3D pixel sensor bump bonding and a second one, FE I2.1-SCC6, with a 2D pixel sensor bump bonding.

III.1.FE 4E-B with 3D pixel

Three configurations of 3D sensor are available, 2E, 3E and 4E. On Figure III.1 which represents our FE we have a detector with 4E configuration.

View on Figure III.2, the several configuration layouts. The more columns there are, the higher the efficiency signal is and the lower voltage supply is needed.

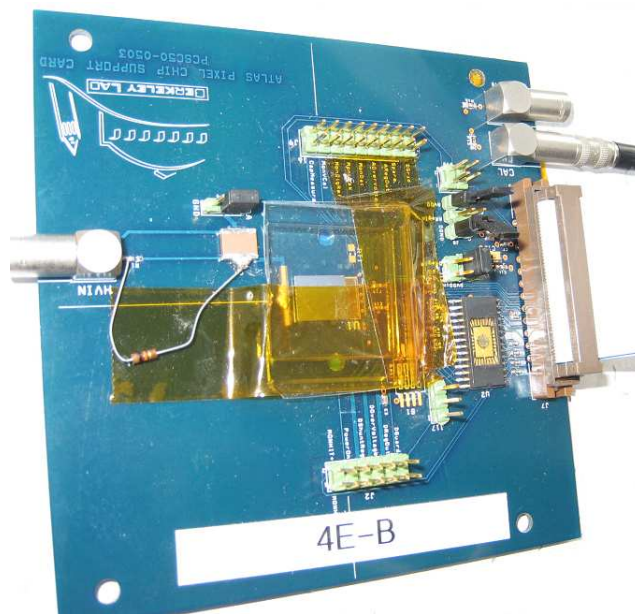


Figure III.1 : FE 4E-B

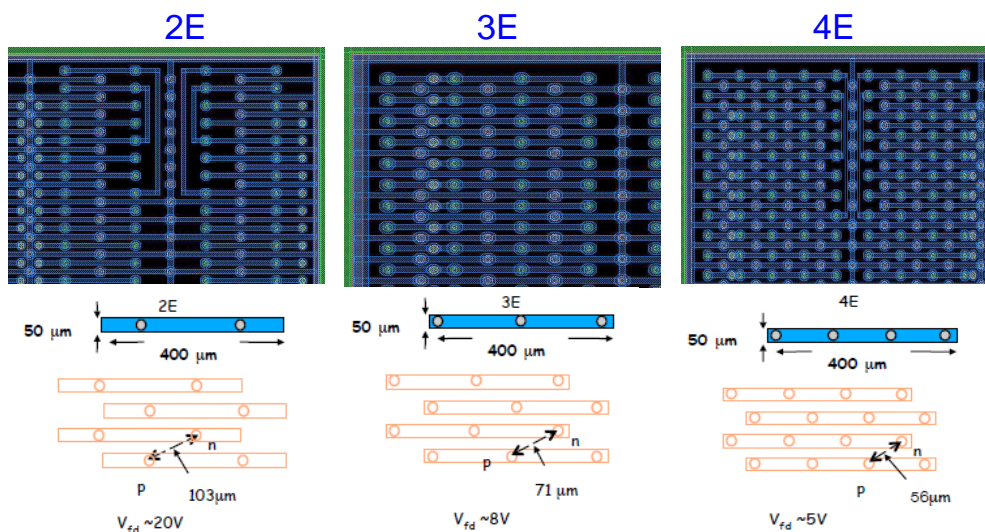


Figure III.2 : 3D configurations

Unfortunately, we encounter a problem with this FE. Indeed we have error message during the test registers under the “Configuration panel”.

We decide to observe the board with a microscope and we find the problem. Five wires bonded are broken. These wires assure the connection between the sensor and the FE.

So, thanks to CERN we repair this electronic card (cf Figure III.3) but the problem remains.

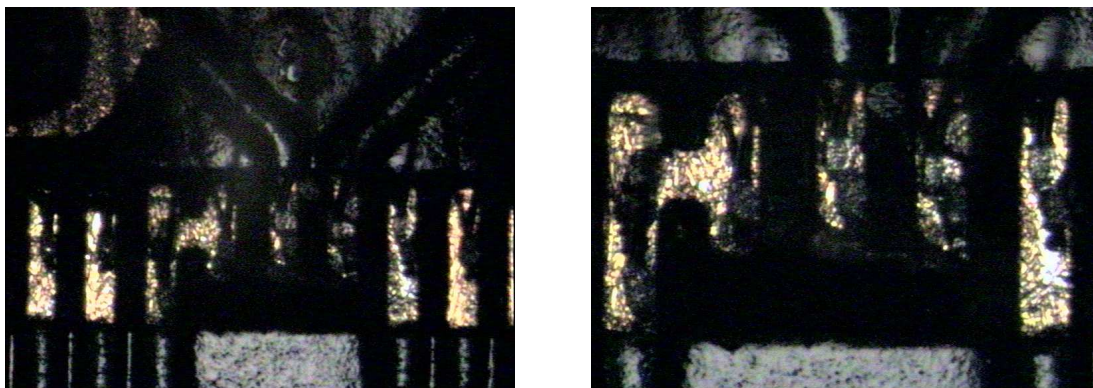


Figure III.3 : Wires bonded

III.2.FE 2I.1-SCC6 with 2D pixel

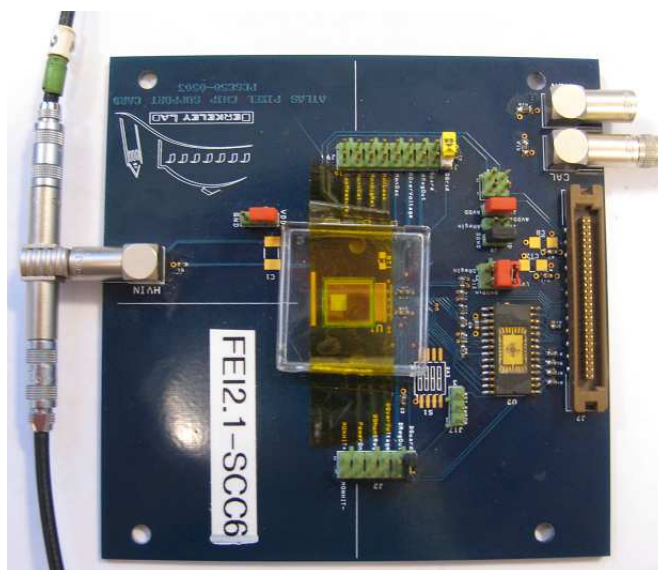


Figure III.4 : FE I2.1-SCC6

A 2D pixel is bump bonding on the FE and it exactly the same measurement under TurboDAQ.

We can see on Figure III.5 a threshold scan result. The target value is fixed at $3200 e^-$ and the sensor signal is 30 to $25k e^-$. The threshold mean value obtained is around $2700 e^-$ (in red), so we can improve this scan thanks to the several parameters. (GDAC, TDAC, FDAC, etc...)

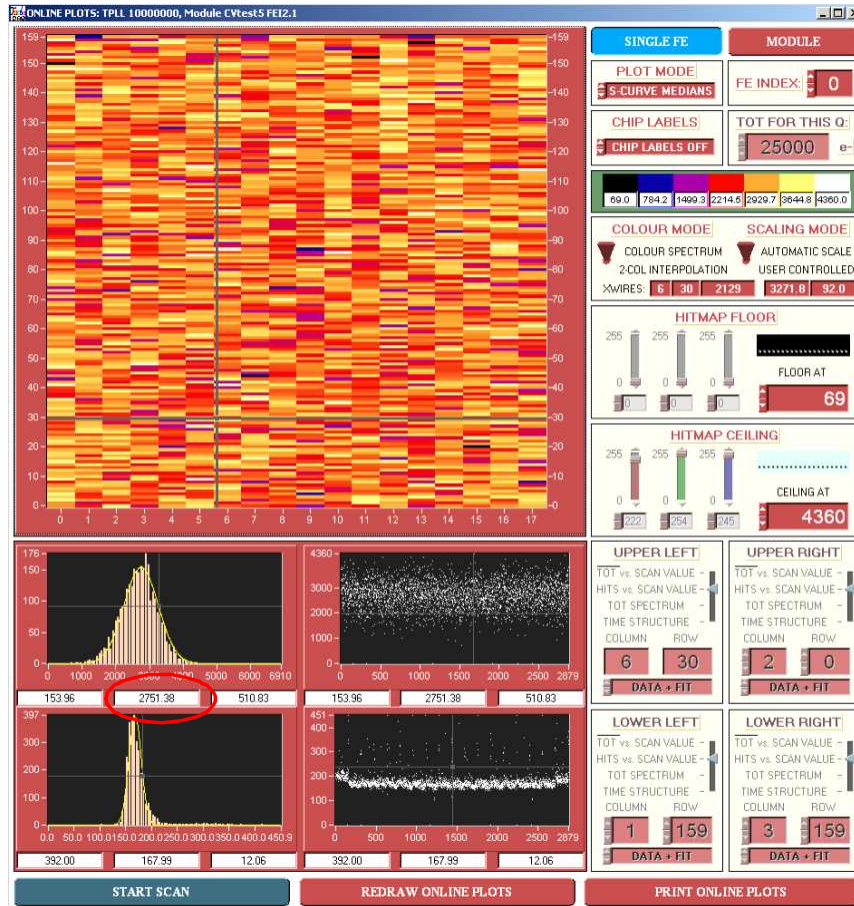


Figure III.5 : Threshold scan results

We study the GDAC parameter with this board and we obtain the results in the following tab:

GDAC	6	9	10	12	13
Threshold mean value	2151	2789	3019	3141	3457

When GDAC is fixed at 12, we obtain the nearest value to the target. So we fixed this value to continue the threshold procedure.

After, we carry out TDAC scan but a problem happen. In the file “namefile_tdacs_0.out” all the value is 127, the maximum value, so there is probably an offset somewhere but we do not manage to figure out it.

Finally, we carry out a FDAC scan and we obtain a correct “namefile_fdacs_0.out” file, so we upload this file in “Configuration panel” and we make a threshold scan. This last scan is improved by the parameter FDAC but our threshold map is not totally uniform and the threshold mean Gaussian is very large, so other parameter must be improve.

All the results are in the folder “TurboDAQ” on the 3D system computer and to have more information concerning 3D consult the folder “3D” on the same computer.



CONCLUSION

At the end of this 3 months period we manage to build a 3D measurement system thanks to card borrowed from CERN. The system operates and we manage to obtain correct scans.

Moreover, Bergen subatomic laboratory obtain some experience in pixel detectors and measurements

Now we are ready to receive module from CERN partnership as soon as we have the repaired cards from Bonn.

For my part, it was a very pleasant period and it was interesting to discover the particles physic field and particularly the 3D technology.

I would like to thanks Heidi SANDAKER because without her, I have not been here. And I would like to thanks too, all people who help me during this project: Alessandro, Bjarne, Dominik, Havard, Joern, Ole, etc...