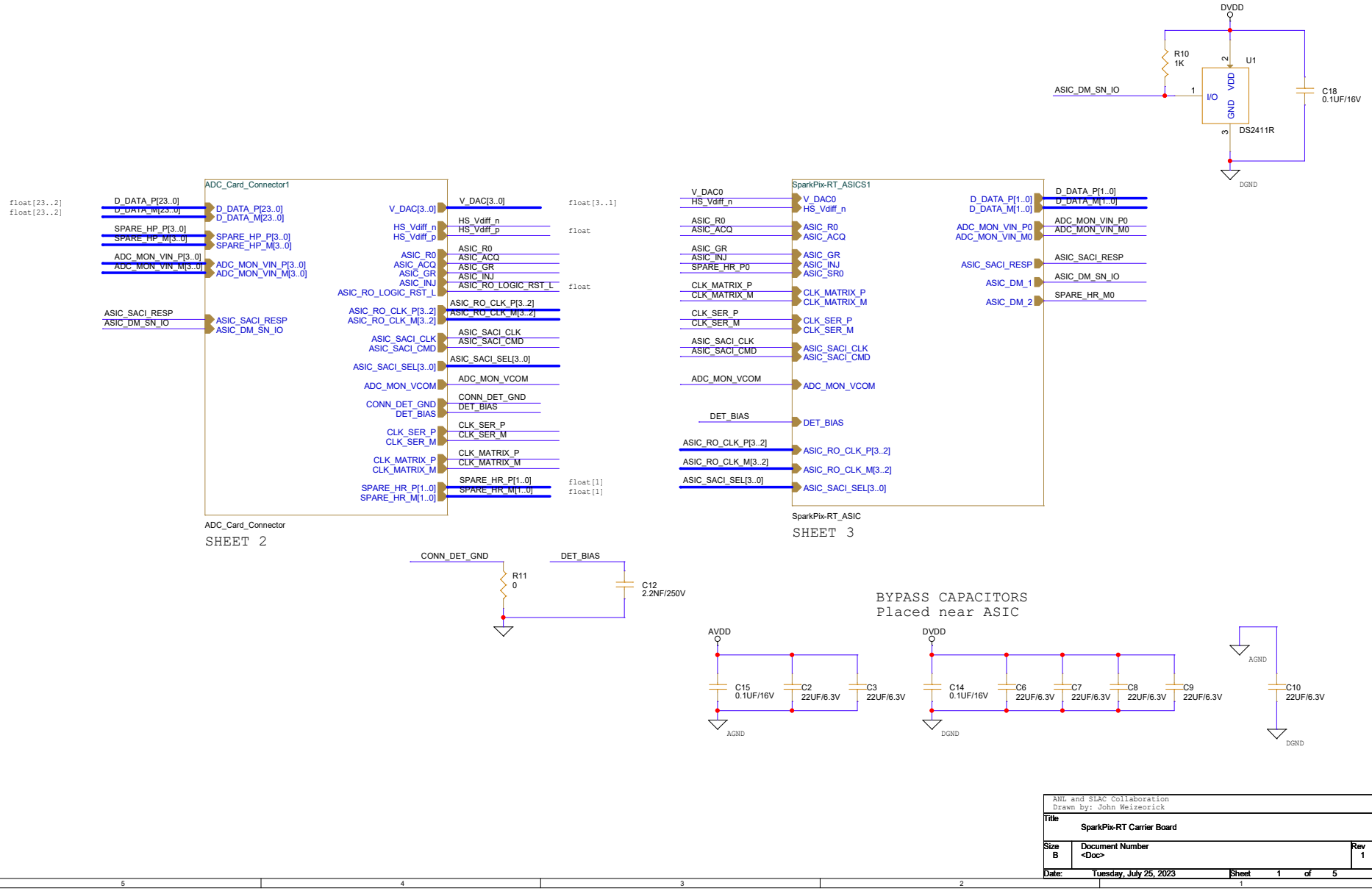
DVDD
R10
1K
U1
ASIC_DM_SN_IO
I/O
VDD
GND
DS2411R
C18
0.1UF/16V
DGND
ADC_Card_Connector1
D_DATA_P[23..0]
D_DATA_M[23..0]
SPARE_HP_P[3..0]
SPARE_HP_M[3..0]
ADC_MON_VIN_P[3..0]
ADC_MON_VIN_M[3..0]
ASIC_SACI_RESP
ASIC_DM_SN_IO
V_DAC[3..0]
HS_Vdiff_n
HS_Vdiff_p
ASIC_R0
ASIC_ACQ
ASIC_GR
ASIC_INJ
ASIC_RO_LOGIC_RST_L
ASIC_RO_CLK_P[3..2]
ASIC_RO_CLK_M[3..2]
ASIC_SACI_CLK
ASIC_SACI_CMD
ASIC_SACI_SEL[3..0]
ADC_MON_VCOM
CONN_DET_GND
DET_BIAS
CLK_SER_P
CLK_SER_M
CLK_MATRIX_P
CLK_MATRIX_M
SPARE_HR_P[1..0]
SPARE_HR_M[1..0]
float[23..2]
float[3..1]
float
float[1]
ADC_Card_Connector
SHEET 2
SparkPix-RT_ASICS1
SPARE_HR_P0
ASIC_SR0
ADC_MON_VIN_P0
ADC_MON_VIN_M0
ASIC_DM_1
ASIC_DM_2
SPARE_HR_M0
SparkPix-RT_ASIC
SHEET 3
R11
0
C12
2.2NF/250V
BYPASS CAPACITORS
Placed near ASIC
AVDD
C15
0.1UF/16V
C2
22UF/6.3V
C3
22UF/6.3V
AGND
C14
0.1UF/16V
C6
22UF/6.3V
C7
22UF/6.3V
C8
22UF/6.3V
C9
22UF/6.3V
DGND
C10
22UF/6.3V
ANL and SLAC Collaboration
Drawn by: John Weizeorick
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High speed signals

HS_Vdiff_n
HS_Vdiff_p
HS_Vdiff_n
HS_Vdiff_p

SACI SIGNALS FROM ASIC

ASIC_SACI_RESP
ASIC_SACI_RESP

DIFFERENTIAL FROM ASIC

D_DATA_M[23..0]
D_DATA_P[23..0]
D_DATA_M[23..0]
D_DATA_P[23..0]

SPARE_HP_P[3..0]
SPARE_HP_M[3..0]
SPARE_HP_P[3..0]
SPARE_HP_M[3..0]

ADC_MON_VIN_P[3..0]
ADC_MON_VIN_M[3..0]
ADC_MON_VIN_P[3..0]
ADC_MON_VIN_M[3..0]

SPARE_HR_P[1..0]
SPARE_HR_M[1..0]
SPARE_HR_P[1..0]
SPARE_HR_M[1..0]

ADC_MON_VCOM
ADC_MON_VCOM

BIASES AND GAURD RINGS

CONN_DET_GND
CONN_DET_GND
DET_BIAS
DET_BIAS
V_DAC[3..0]
V_DAC[3..0]

DIFFERENTIAL READOUT CLOCKS TO ASICS

ASIC_RO_CLK_P[3..2]
ASIC_RO_CLK_P[3..2]
ASIC_RO_CLK_M[3..2]
ASIC_RO_CLK_M[3..2]

SACI SIGNALS TO ASIC

ASIC_SACI_CLK
ASIC_SACI_CLK
ASIC_SACI_CMD
ASIC_SACI_CMD
ASIC_SACI_SEL[3..0]
ASIC_SACI_SEL[3..0]

SINGLE ENDED TO ASICS

ASIC_INJ
ASIC_INJ
ASIC_R0
ASIC_R0
ASIC_ACQ
ASIC_ACQ
ASIC_RO_LOGIC_RST_L
ASIC_RO_LOGIC_RST_L
ASIC_GR
ASIC_GR

CLK_SER_P
CLK_SER_M
CLK_SER_P
CLK_SER_M

CLK_MATRIX_P
CLK_MATRIX_M
CLK_MATRIX_P
CLK_MATRIX_M

Serial Number

ASIC_DM_SN_IO
ASIC_DM_SN_IO

J3A

SEAF-20-10

1	A1	
2	A2	
3	A3	V_DAC1
4	A4	
5	A5	D_DATA_P9
6	A6	D_DATA_M9
7	A7	
8	A8	
9	A9	D_DATA_P4
10	A10	D_DATA_M4
11	A11	
12	A12	
13	A13	D_DATA_P6
14	A14	D_DATA_M6
15	A15	
16	A16	
17	A17	V_DAC3
18	A18	
19	A19	
20	A20	

AVDD DVDD AGND DGND
VCCA
TP3
T POINT A

J3B

SEAF-20-10

1	B1	
2	B2	
3	B3	D_DATA_P8
4	B4	D_DATA_M8
5	B5	
6	B6	
7	B7	D_DATA_P3
8	B8	D_DATA_M3
9	B9	
10	B10	
11	B11	D_DATA_P5
12	B12	D_DATA_M5
13	B13	
14	B14	
15	B15	D_DATA_P7
16	B16	D_DATA_M7
17	B17	
18	B18	V_DAC2
19	B19	
20	B20	

AVDD DVDD AGND DGND

J3C

SEAF-20-10

1	C1	
2	C2	
3	C3	V_DAC0
4	C4	
5	C5	D_DATA_P1
6	C6	D_DATA_M1
7	C7	
8	C8	
9	C9	D_DATA_P10
10	C10	D_DATA_M10
11	C11	
12	C12	
13	C13	D_DATA_P12
14	C14	D_DATA_M12
15	C15	
16	C16	
17	C17	HS_Vdiff_p
18	C18	HS_Vdiff_n
19	C19	
20	C20	

AVDD DVDD AGND DGND

J3D

SEAF-20-10

1	D1	
2	D2	
3	D3	D_DATA_P0
4	D4	D_DATA_M0
5	D5	
6	D6	
7	D7	D_DATA_P2
8	D8	D_DATA_M2
9	D9	
10	D10	
11	D11	D_DATA_P11
12	D12	D_DATA_M11
13	D13	
14	D14	
15	D15	D_DATA_P13
16	D16	D_DATA_M13
17	D17	
18	D18	ADC_MON_VCOM
19	D19	
20	D20	

AVDD DVDD AGND DGND

J3E

SEAF-20-10

1	E1	
2	E2	
3	E3	ASIC_INJ
4	E4	
5	E5	ADC_MON_VIN_P3
6	E6	ADC_MON_VIN_M3
7	E7	
8	E8	
9	E9	ADC_MON_VIN_P2
10	E10	ADC_MON_VIN_M2
11	E11	
12	E12	
13	E13	ADC_MON_VIN_P1
14	E14	ADC_MON_VIN_M1
15	E15	
16	E16	
17	E17	ADC_MON_VIN_P0
18	E18	ADC_MON_VIN_M0
19	E19	
20	E20	

AVDD DVDD AGND DGND

DVDD_IO

J3F

SEAF-20-10

1	F1	
2	F2	
3	F3	CLK_SER_P
4	F4	CLK_SER_M
5	F5	
6	F6	
7	F7	CLK_MATRIX_P
8	F8	CLK_MATRIX_M
9	F9	
10	F10	
11	F11	ASIC_RO_CLK_P2
12	F12	ASIC_RO_CLK_M2
13	F13	
14	F14	
15	F15	ASIC_RO_CLK_P3
16	F16	ASIC_RO_CLK_M3
17	F17	
18	F18	
19	F19	
20	F20	

AVDD DVDD AGND DGND

DVDD_IO

J3G

SEAF-20-10

1	G1	
2	G2	
3	G3	D_DATA_P14
4	G4	D_DATA_M14
5	G5	D_DATA_P17
6	G6	D_DATA_M17
7	G7	
8	G8	
9	G9	D_DATA_P15
10	G10	D_DATA_M15
11	G11	
12	G12	ASIC_ACQ
13	G13	
14	G14	ASIC_RO_LOGIC_RST_L
15	G15	
16	G16	D_DATA_P16
17	G17	D_DATA_M16
18	G18	
19	G19	
20	G20	

AVDD DVDD AGND DGND

DVDD_IO

J3H

SEAF-20-10

1	H1	
2	H2	
3	H3	CONN_DET_GND
4	H4	DET_BIAS
5	H5	
6	H6	ASIC_SACI_RESP
7	H7	ASIC_SACI_SEL2
8	H8	ASIC_SACI_SEL3
9	H9	ASIC_R0
10	H10	
11	H11	ASIC_SACI_CMD
12	H12	ASIC_SACI_SEL0
13	H13	ASIC_SACI_CLK
14	H14	
15	H15	ASIC_SACI_SEL1
16	H16	
17	H17	ASIC_DM_SN_IO
18	H18	ASIC_GR
19	H19	
20	H20	

AVDD DVDD AGND DGND

J3I

SEAF-20-10

1	J1	
2	J2	
3	J3	D_DATA_P18
4	J4	D_DATA_M18
5	J5	
6	J6	D_DATA_P19
7	J7	D_DATA_M19
8	J8	
9	J9	D_DATA_P20
10	J10	D_DATA_M20
11	J11	
12	J12	SPARE_HP_P0
13	J13	SPARE_HP_M0
14	J14	SPARE_HP_P1
15	J15	SPARE_HP_M1
16	J16	
17	J17	SPARE_HR_P0
18	J18	SPARE_HR_M0
19	J19	
20	J20	

AVDD DVDD AGND DGND

J3J

SEAF-20-10

1	K1	
2	K2	
3	K3	D_DATA_P23
4	K4	D_DATA_M23
5	K5	
6	K6	D_DATA_P22
7	K7	D_DATA_M22
8	K8	
9	K9	D_DATA_P21
10	K10	D_DATA_M21
11	K11	
12	K12	SPARE_HP_P3
13	K13	SPARE_HP_M3
14	K14	SPARE_HP_P2
15	K15	SPARE_HP_M2
16	K16	
17	K17	SPARE_HR_P1
18	K18	SPARE_HR_M1
19	K19	
20	K20	

AVDD DVDD AGND DGND

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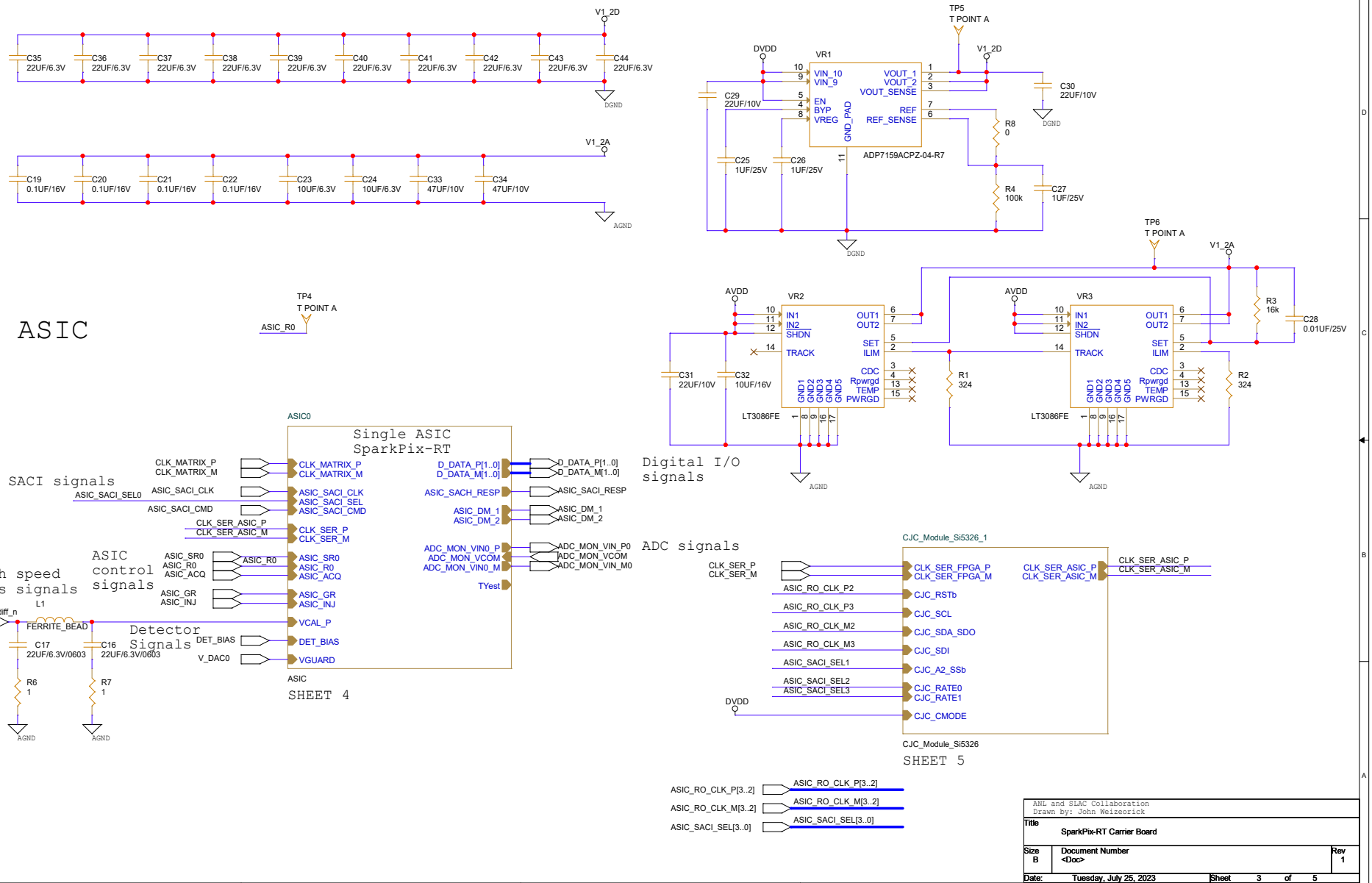
V1_2D
C35 22UF/6.3V
C36 22UF/6.3V
C37 22UF/6.3V
C38 22UF/6.3V
C39 22UF/6.3V
C40 22UF/6.3V
C41 22UF/6.3V
C42 22UF/6.3V
C43 22UF/6.3V
C44 22UF/6.3V
DGND
V1_2A
C19 0.1UF/16V
C20 0.1UF/16V
C21 0.1UF/16V
C22 0.1UF/16V
C23 10UF/6.3V
C24 10UF/6.3V
C33 47UF/10V
C34 47UF/10V
AGND
TP5
T POINT A
DVDD
VR1
VIN_10
VIN_9
EN
BYP
VREG
GND_PAD
VOUT_1
VOUT_2
VOUT_SENSE
REF
REF_SENSE
ADP7159ACPZ-04-R7
C29 22UF/10V
C25 1UF/25V
C26 1UF/25V
C30 22UF/10V
R8 0
R4 100k
C27 1UF/25V
TP6
T POINT A
V1_2A
AVDD
VR2
VR3
IN1
IN2
SHDN
TRACK
OUT1
OUT2
SET
ILIM
CDC
Rpwrgd
TEMP
PWRGD
GND1
GND2
GND3
GND4
GND5
LT3086FE
C31 22UF/10V
C32 10UF/16V
R1 324
R2 324
R3 16k
C28 0.01UF/25V
ASIC
TP4
T POINT A
ASIC_R0
ASIC0
Single ASIC
SparkPix-RT
SACI signals
ASIC_SACI_SEL0
ASIC_SACI_CLK
ASIC_SACI_CMD
CLK_MATRIX_P
CLK_MATRIX_M
CLK_SER_ASIC_P
CLK_SER_ASIC_M
ASIC_SR0
ASIC_R0
ASIC_ACQ
ASIC_GR
ASIC_INJ
ASIC control signals
High speed DACs signals
HS_Vdiff_n
L1
FERRITE_BEAD
C17 22UF/6.3V/0603
C16 22UF/6.3V/0603
R6 1
R7 1
Detector Signals
DET_BIAS
V_DAC0
VCAL_P
DET_BIAS
VGUARD
D_DATA_P[1..0]
D_DATA_M[1..0]
ASIC_SACH_RESP
ASIC_DM_1
ASIC_DM_2
ADC_MON_VIN0_P
ADC_MON_VCOM
ADC_MON_VIN0_M
TYest
Digital I/O signals
ADC signals
ASIC
SHEET 4
CJC_Module_Si5326_1
CLK_SER_P
CLK_SER_M
CLK_SER_FPGA_P
CLK_SER_FPGA_M
CLK_SER_ASIC_P
CLK_SER_ASIC_M
ASIC_RO_CLK_P2
ASIC_RO_CLK_P3
ASIC_RO_CLK_M2
ASIC_RO_CLK_M3
ASIC_SACI_SEL1
ASIC_SACI_SEL2
ASIC_SACI_SEL3
CJC_RSTb
CJC_SCL
CJC_SDA_SDO
CJC_SDI
CJC_A2_SSb
CJC_RATE0
CJC_RATE1
CJC_CMODE
DVDD
CJC_Module_Si5326
SHEET 5
ASIC_RO_CLK_P[3..2]
ASIC_RO_CLK_M[3..2]
ASIC_SACI_SEL[3..0]
ANL and SLAC Collaboration
Drawn by: John Weizeorick
Title
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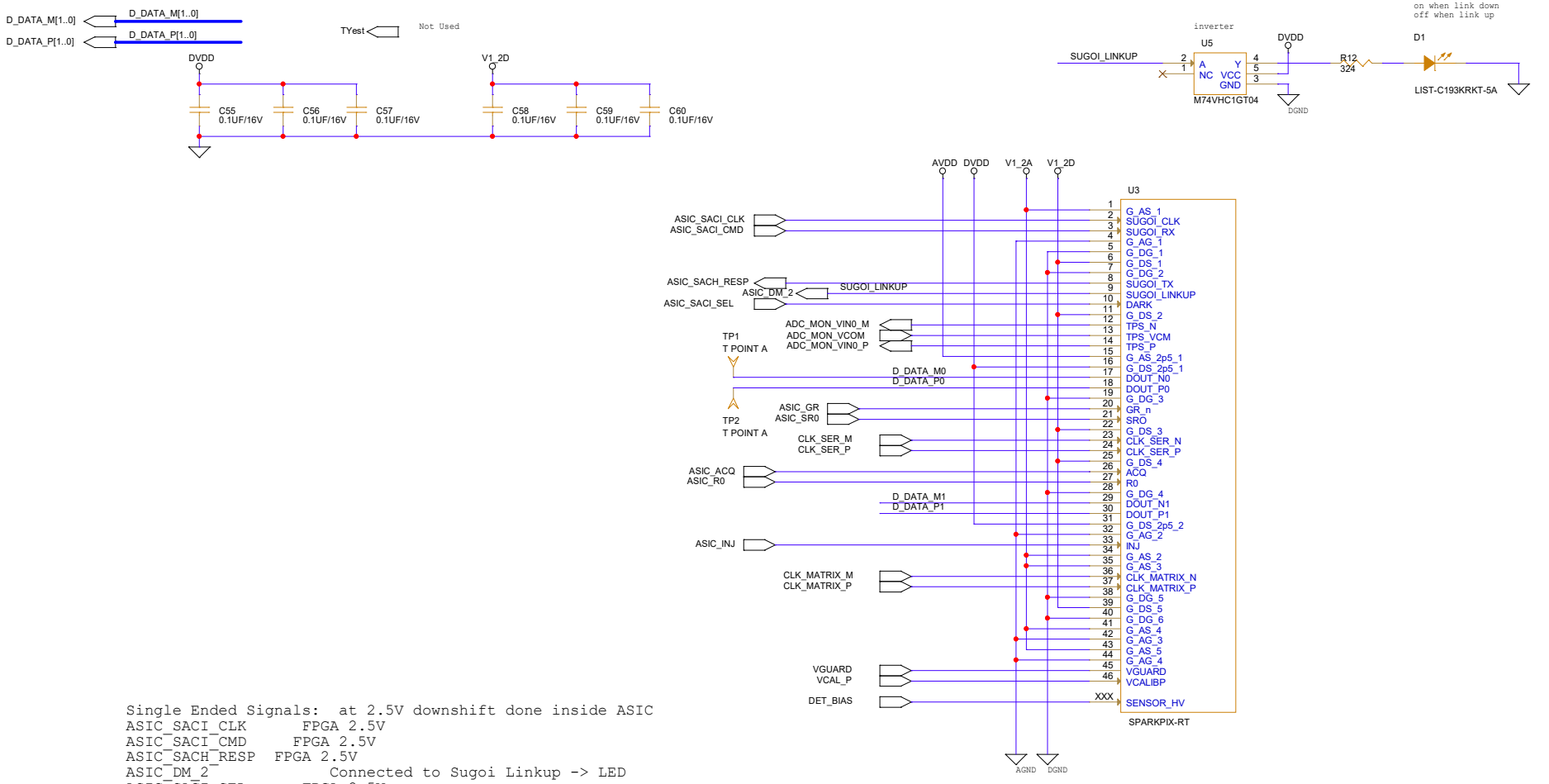

Single Ended Signals: at 2.5V downshift done inside ASIC
ASIC_SACI_CLK FPGA 2.5V
ASIC_SACI_CMD FPGA 2.5V
ASIC_SACH_RESP FPGA 2.5V
ASIC_DM_2 Connected to Sugoi Linkup -> LED
ASIC_SACI_SEL FPGA 2.5V
ASIC_GR FPGA 2.5V
ASIC_SR0 Maps to SPARE_HR_P0 which is in Bank 64 Which is 2.5V
ASIC_ACQ FPGA 2.5V
ASIC_R0 FPGA 2.5V

ASIC_INJ Maps to ASIC_SYNC which is Bank 13
Using Vdd which is either 2.5V or 3.3V

G_DS = V1_2A = 1.2V
G_AS = V1_2D = 1.2V
AVDD = 2.5V
DVDD = 2.5V

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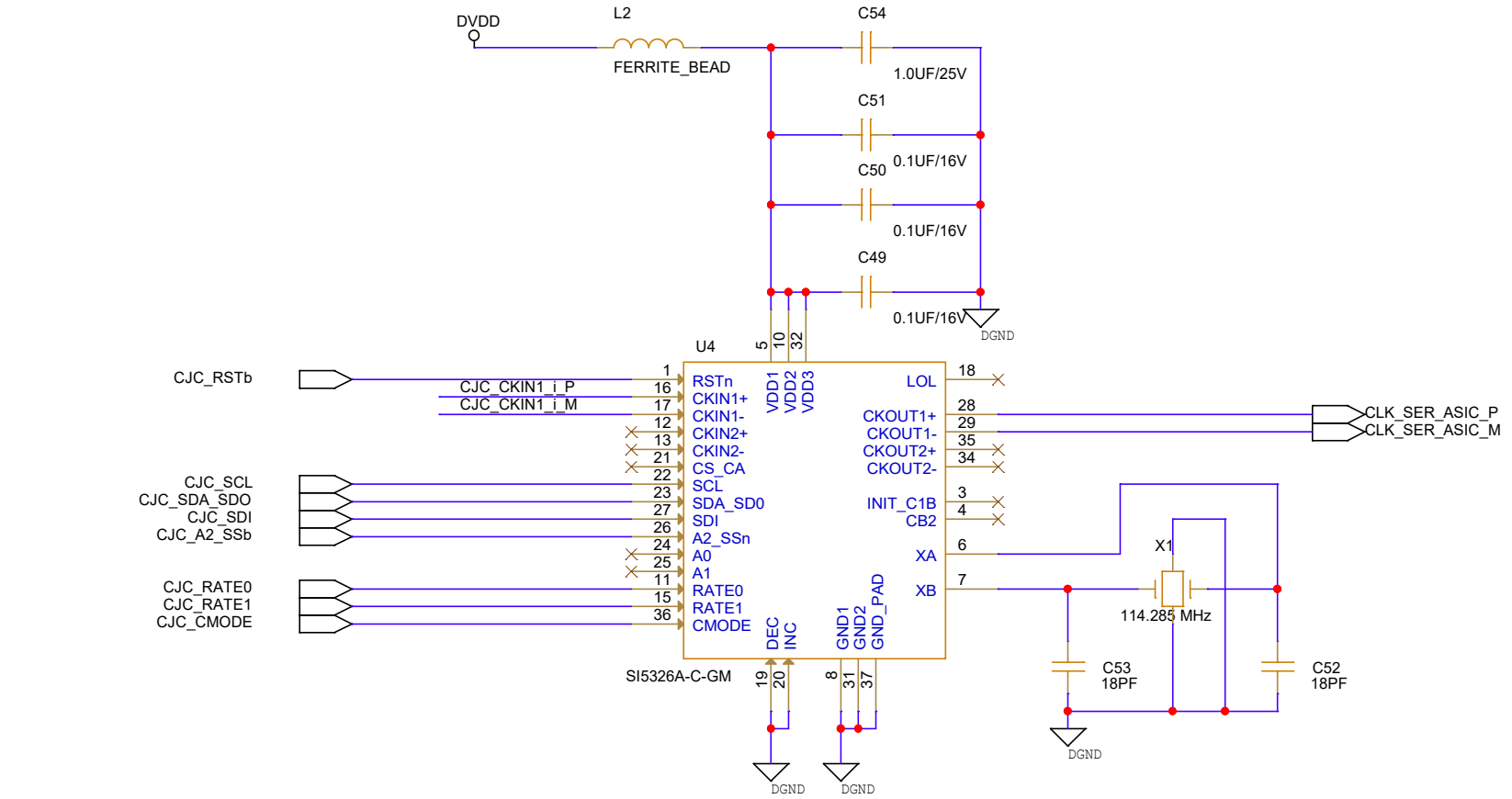

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