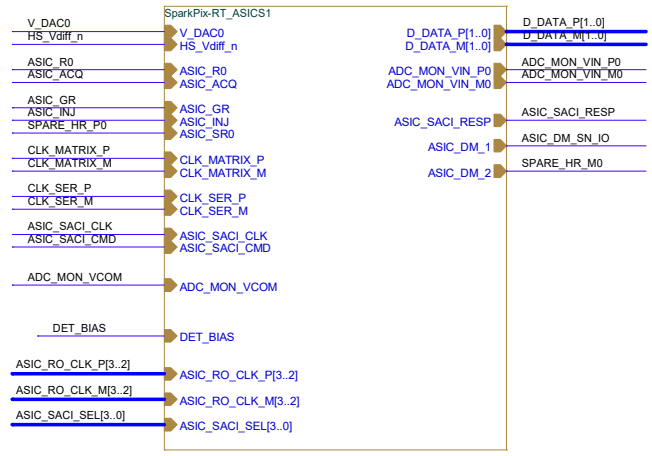
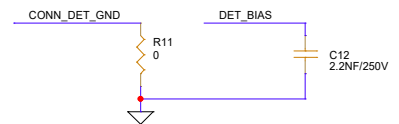
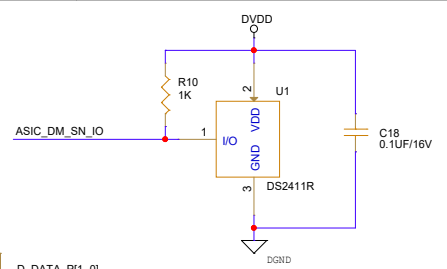


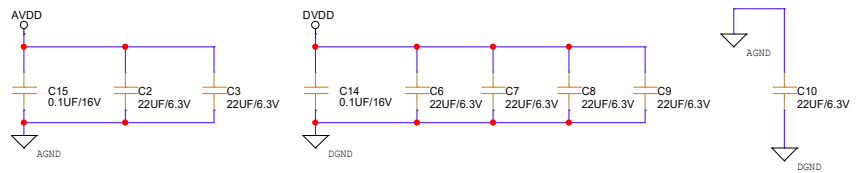
ADC\_Card\_Connector  
SHEET 2



SparkPix-RT\_ASIC  
SHEET 3



BYPASS CAPACITORS  
Placed near ASIC

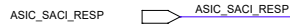


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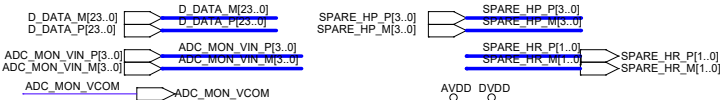
High speed signals



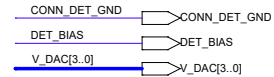
SACI SIGNALS FROM ASIC



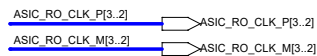
DIFFERENTIAL FROM ASIC



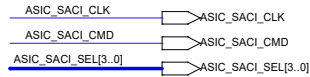
BIASES AND GAURD RINGS



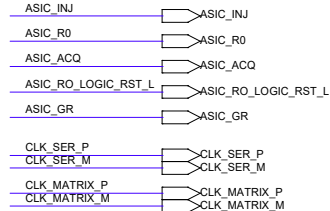
DIFFERENTIAL READOUT CLOCKS TO ASICS



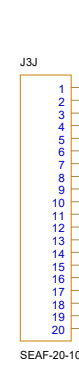
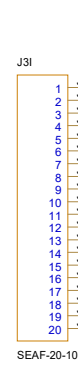
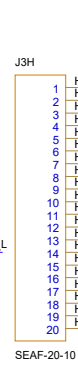
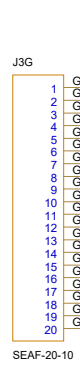
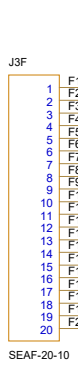
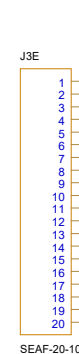
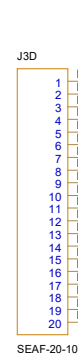
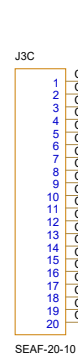
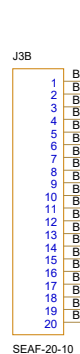
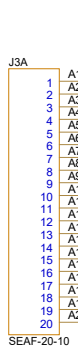
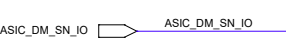
SACI SIGNALS TO ASIC



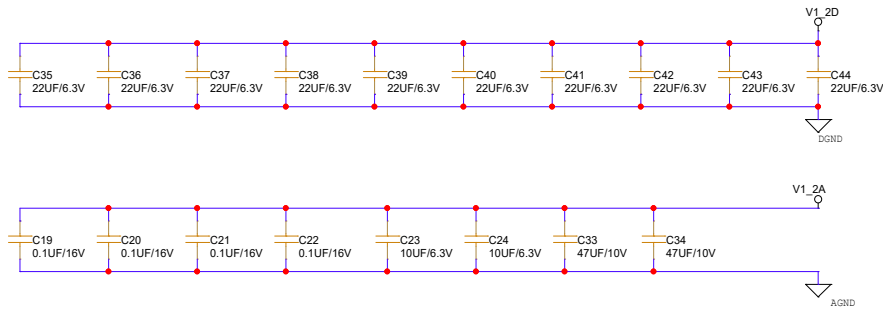
SINGLE ENDED TO ASICS



Serial Number

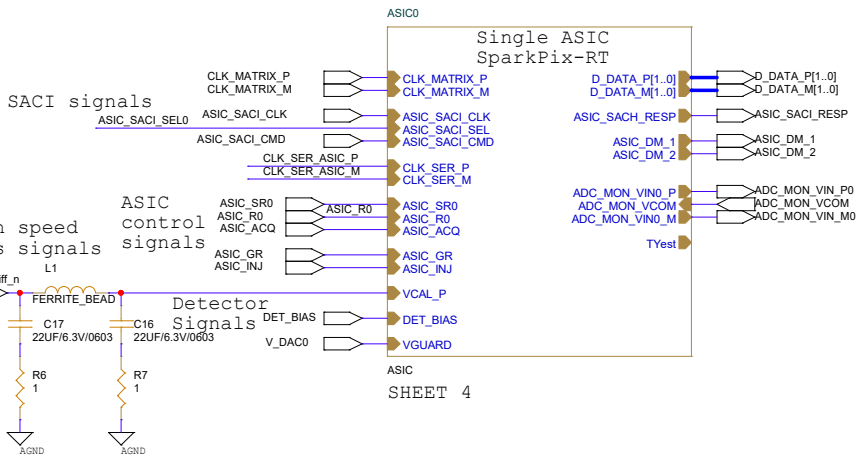


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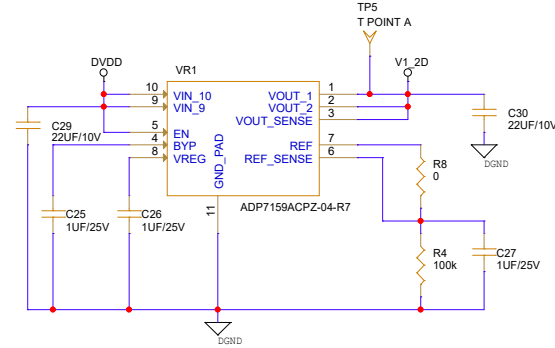


ASIC

TP4  
T POINT A  
ASIC\_R0

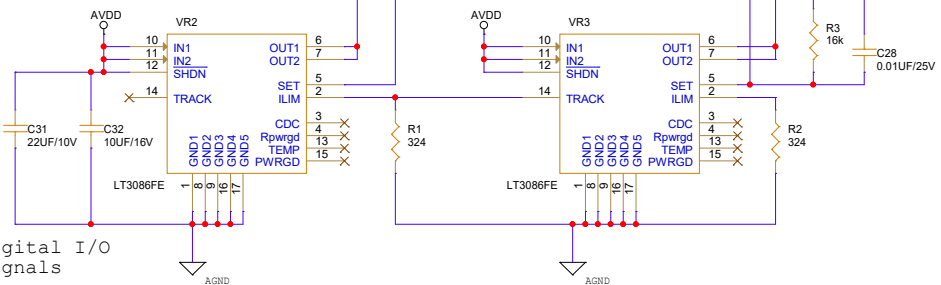


SHEET 4

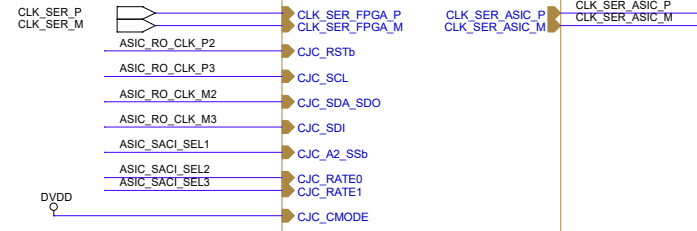


Digital I/O signals

ADC signals



CJC\_Module\_Si5326\_1

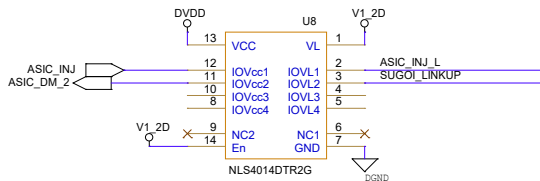
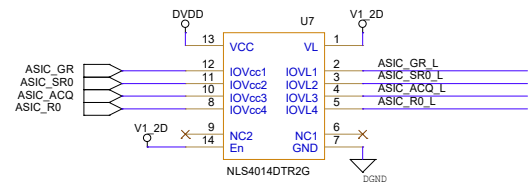
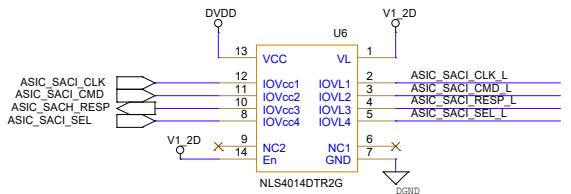
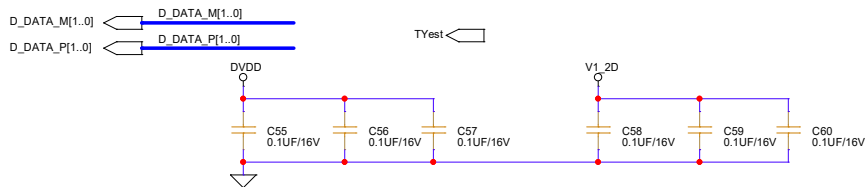


CJC\_Module\_Si5326

SHEET 5



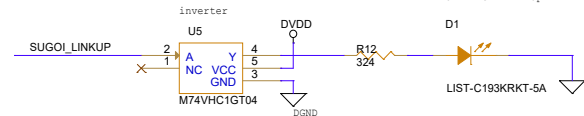
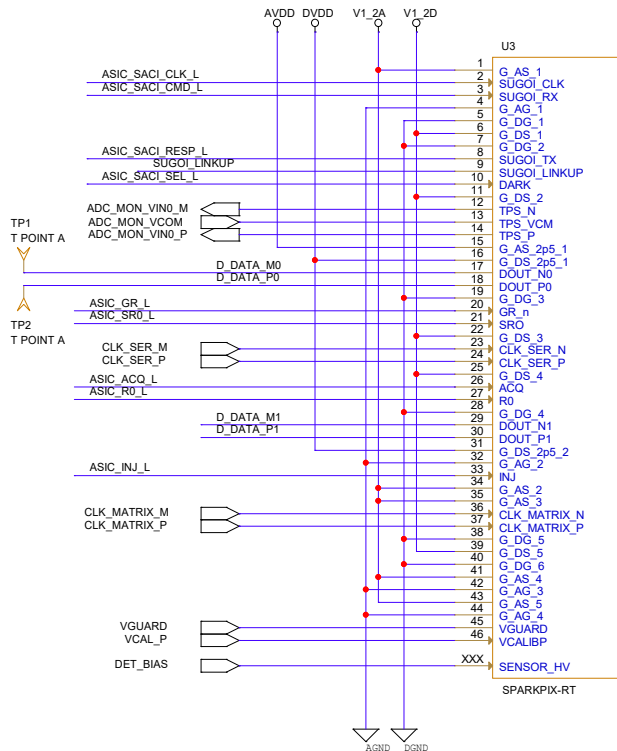
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Single Ended Signals: Level Shift 9

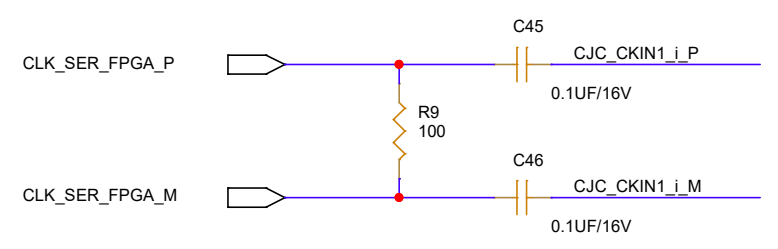
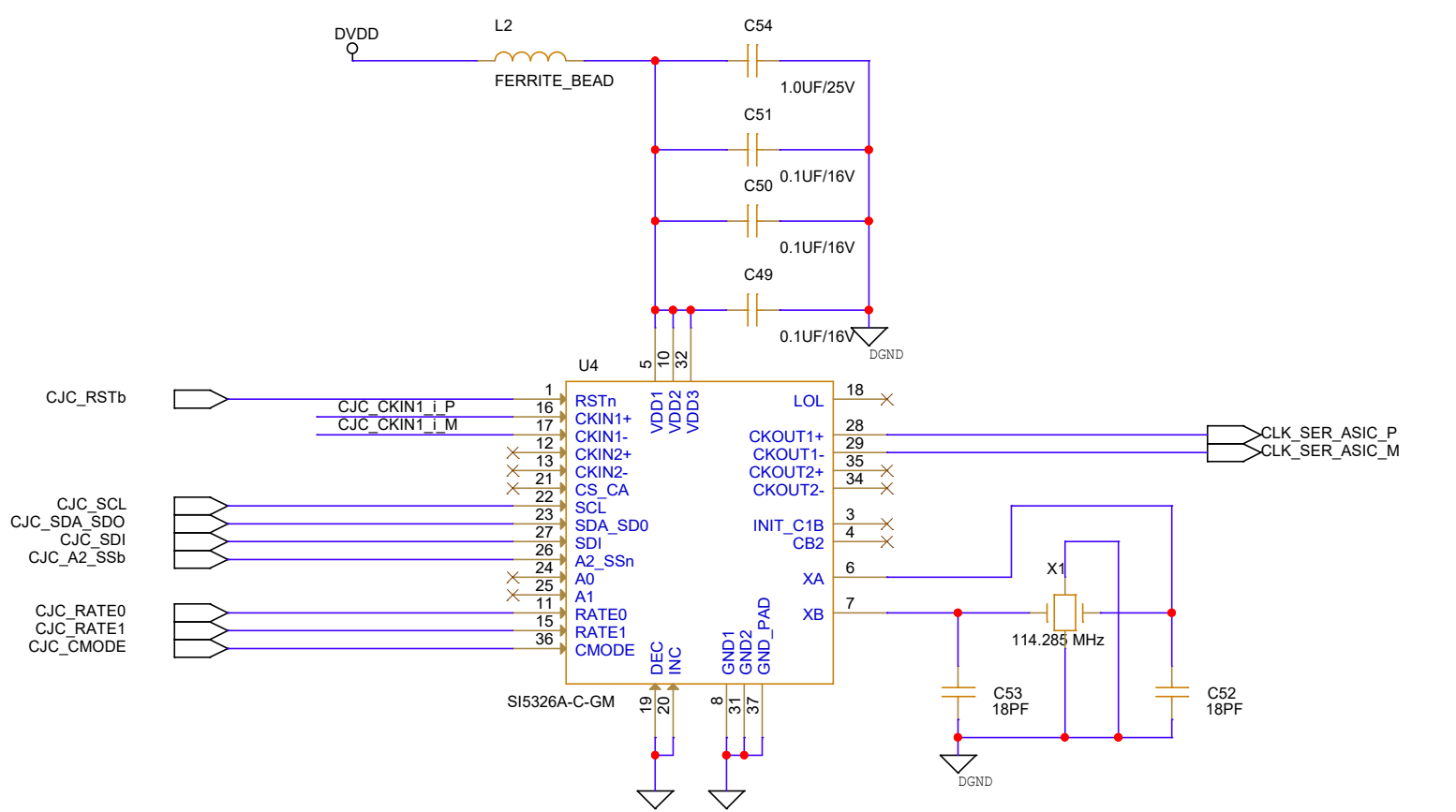
ASIC\_SACHI\_CLK FPGA 2.5V  
 ASIC\_SACHI\_CMD FPGA 2.5V  
 ASIC\_SACHI\_RESP FPGA 2.5V  
 ASIC\_DM\_1 Drives LED for Sugoi Linkup  
 ASIC\_SACHI\_SEL FPGA 2.5V  
 ASIC\_GR FPGA 2.5V  
 ASIC\_SR0 Maps to SPARE\_HR P0 which is in Bank 64 Which is 2.5V  
 ASIC\_ACQ FPGA 2.5V  
 ASIC\_R0 FPGA 2.5V

ASIC\_INJ Maps to ASIC\_SYNC which is Bank 13  
 Using Vdd which is either 2.5V or 3.3V



G\_DS = V1\_2A = 1.2V  
 G\_AS = V1\_2D = 1.2V  
 AVDD = 2.5V  
 DVDD = 2.5V

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