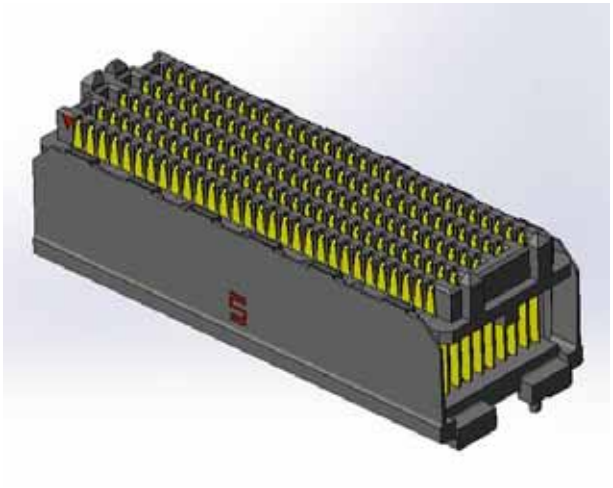
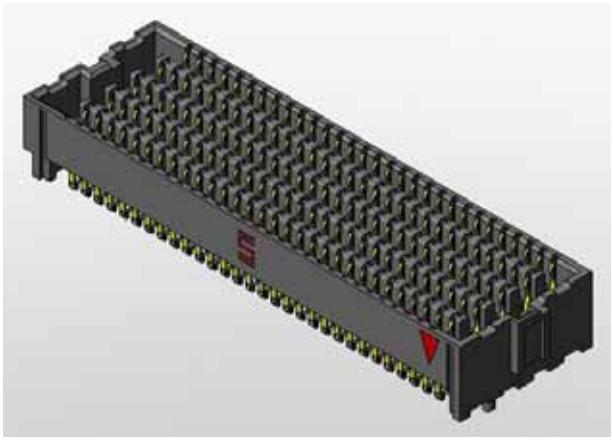
High Speed Characterization Report

SEAM-XX-11.0-X-10-2-A



Mates with

SEAF-XX-06.5-X-10-2-A



Description:
Open Pin Field Array, 1.27mm x 1.27mm Pitch
17.5mm Stack Height

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Report Revision: 3/31/2014

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

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Connector Overview

SEAM/SEAF is a 1.27mm x 1.27mm pitch interconnects system for elevated high-speed board-to-board applications. The open pin field design allows for dual signaling and is suitable for Fiber Channel, Rapid I/O, PCIe, SATA and Infiniband data rates. The SEAM/SEAF Series is available in 5, 6, 8, and 10 row open pin field arrays. Pins per row selections are 20, 30, 40, or 50. For the SEAM/SEAF series, 7mm, 10mm, 12mm, 16mm an 17.5mm stack heights are characterized. This report reflects only the hi-speed electrical characteristics specific to a mated 17.5mm stack height SEAM/SEAF test system.

Connector System Speed Rating

SEAM/SEAF Series, 1.27mm x 1.27mm (.050" x .050") pitch interconnect, 17.5mm Stack Height.

Signaling	Speed Rating
Single-Ended: 1:1 S/G	**12 GHz/ 24Gbps**
Single-Ended: 2:1 S/G	**12.5 GHz/ 25Gbps**
Differential: Optimal Horizontal	**12 GHz/ 24Gbps**
Differential: Optimal Vertical	**12 GHz/ 24Gbps**
Differential: High Density Vertical	**11.5 GHz/ 23Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board's trace loss, since a short length of trace loss is included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

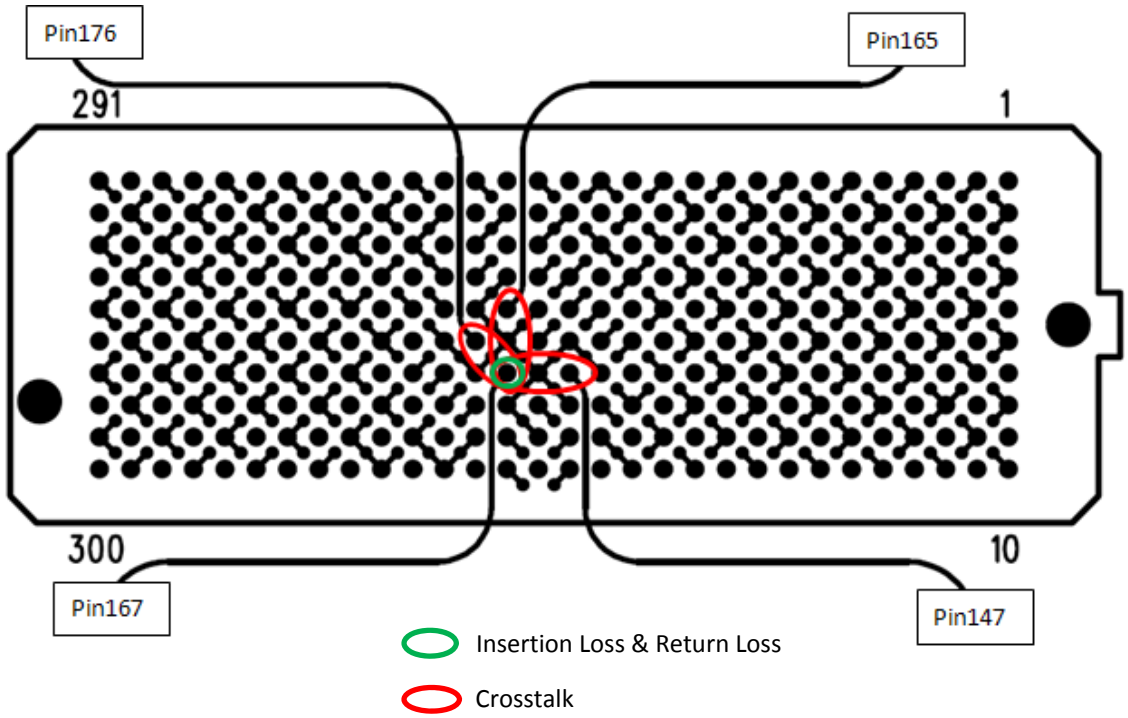
For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Frequency Domain Data Summary

Table 1 - Single-Ended 1:1 S/G Pattern Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	SEAM_167	SEAF_167	3dB@ 11.7 GHz
Return Loss	SEAM_167	SEAM_167	>10dB to 3.8 GHz
Near-End Crosstalk	SEAM_167	SEAM_147	<-20dB to 11.8 GHz
	SEAM_167	SEAM_165	<-20dB to 20 GHz
	SEAM_167	SEAM_176	<-20dB to 16.6 GHz
Far-End Crosstalk	SEAM_167	SEAF_147	<-20dB to 12.5 GHz
	SEAM_167	SEAF_165	<-20dB to 20 GHz
	SEAM_167	SEAF_176	<-20dB to 17.0 GHz

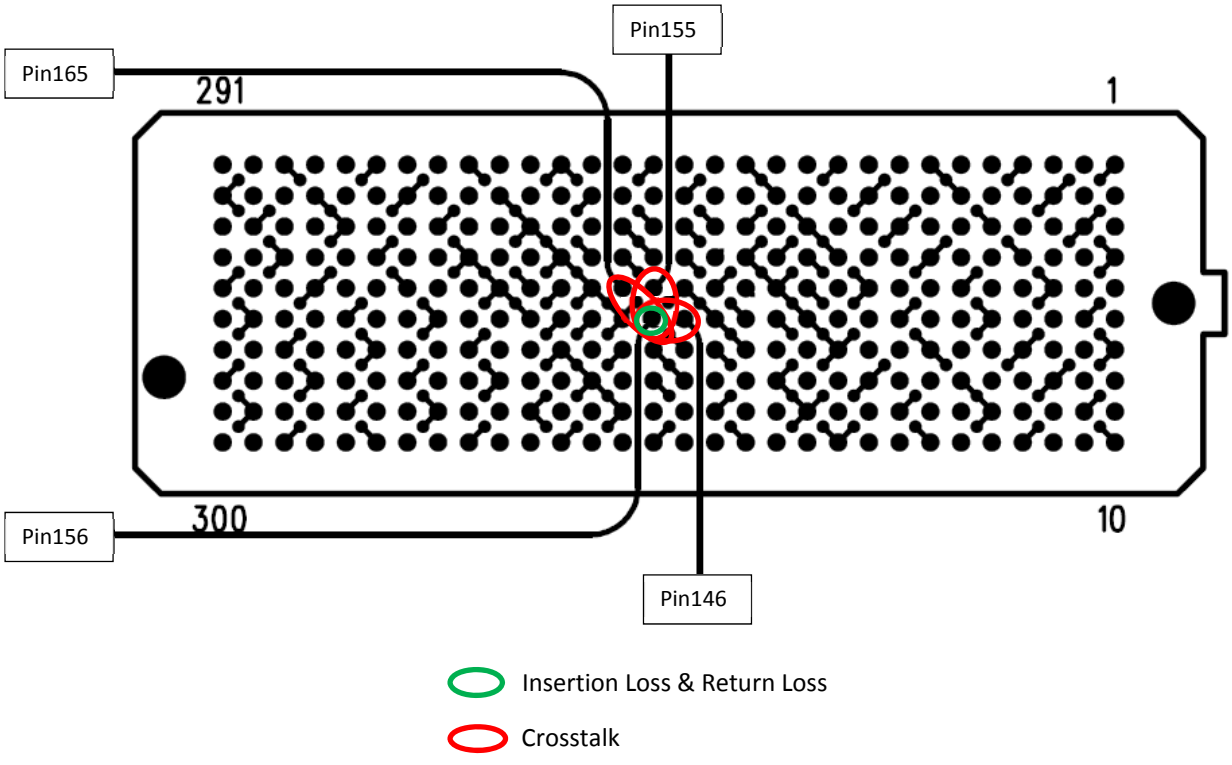
Single-Ended 1:1 S/G Pattern Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 2 - Single-Ended 2:1 S/G Pattern Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	SEAM_156	SEAF_156	3dB@ 12.4 GHz
Return Loss	SEAM_156	SEAM_156	>10dB to 3.7 GHz
Near-End Crosstalk	SEAM_156	SEAM_146	<-20dB to 0.8 GHz
	SEAM_156	SEAM_155	<-20dB to 1.4 GHz
	SEAM_156	SEAM_165	<-20dB to 14.3 GHz
Far-End Crosstalk	SEAM_156	SEAF_146	<-20dB to 6.4 GHz
	SEAM_156	SEAF_155	<-20dB to 14.0 GHz
	SEAM_156	SEAF_165	<-20dB to 17.8 GHz

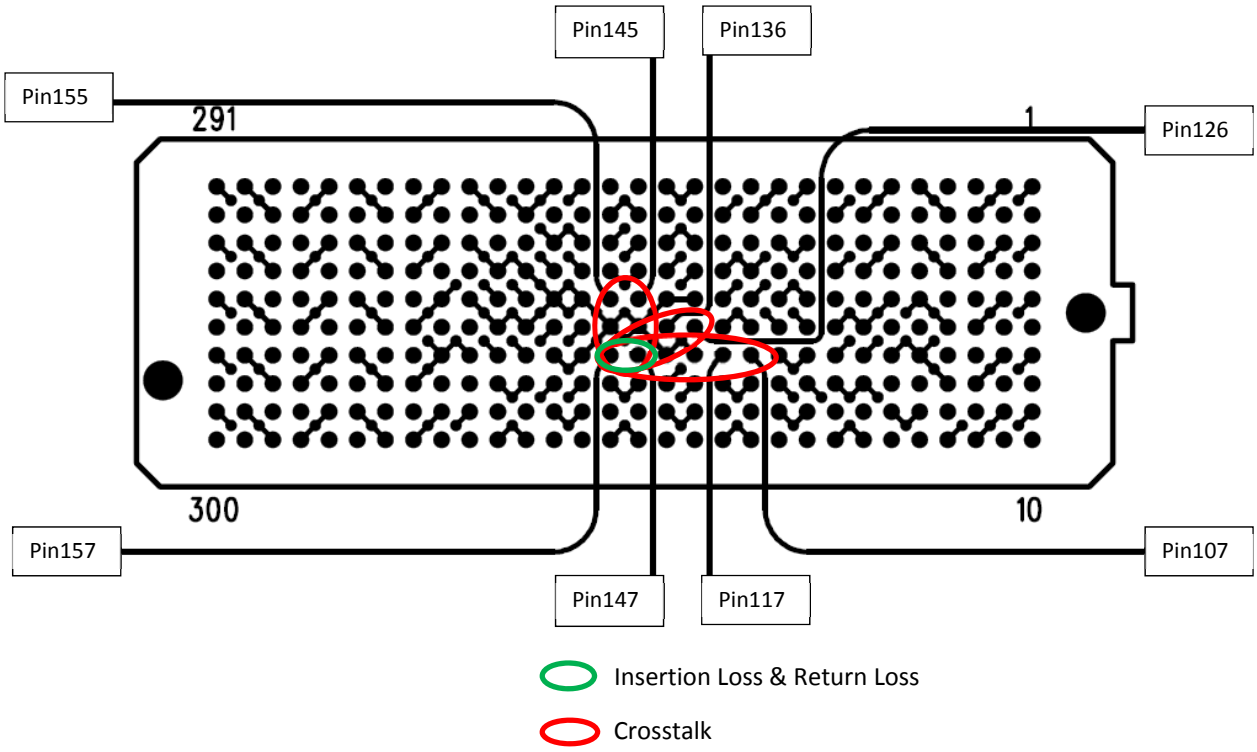
Single-Ended 2:1 S/G Pattern Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 3 - Differential Optimal Horizontal Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	SEAM_147,157	SEAF_147,157	3dB@ 11.8 GHz
Return Loss	SEAM_147,157	SEAM_147,157	>10dB to 9.5 GHz
Near-End Crosstalk	SEAM_147,157	SEAM_107,117	<-20dB to 20 GHz
	SEAM_147,157	SEAM_126,136	<-20dB to 20 GHz
	SEAM_147,157	SEAM_145,155	<-20dB to 20 GHz
Far-End Crosstalk	SEAM_147,157	SEAF_107,117	<-20dB to 20 GHz
	SEAM_147,157	SEAF_126,136	<-20dB to 17.0 GHz
	SEAM_147,157	SEAF_145,155	<-20dB to 20 GHz

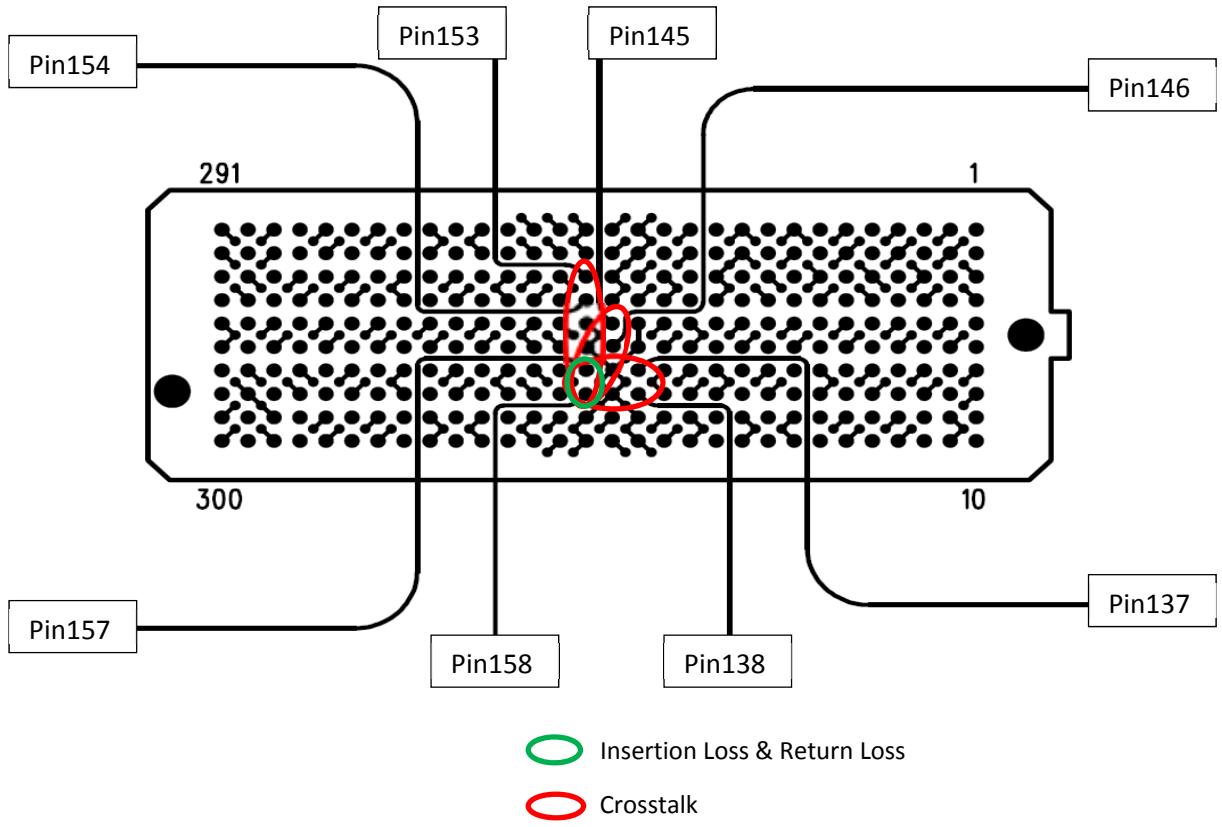
Differential Optimal Horizontal Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 4 - Differential Optimal Vertical Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	SEAM_157,158	SEAF_157,158	3dB@ 11.9 GHz
Return Loss	SEAM_157,158	SEAM_157,158	>10dB to 8.8 GHz
Near-End Crosstalk	SEAM_157,158	SEAM_137,138	<-20dB to 12.8 GHz
	SEAM_157,158	SEAM_145,146	<-20dB to 20 GHz
	SEAM_157,158	SEAM_153,154	<-20dB to 20 GHz
Far-End Crosstalk	SEAM_157,158	SEAF_137,138	<-20dB to 17.3 GHz
	SEAM_157,158	SEAF_145,146	<-20dB to 20 GHz
	SEAM_157,158	SEAF_153,154	<-20dB to 20 GHz

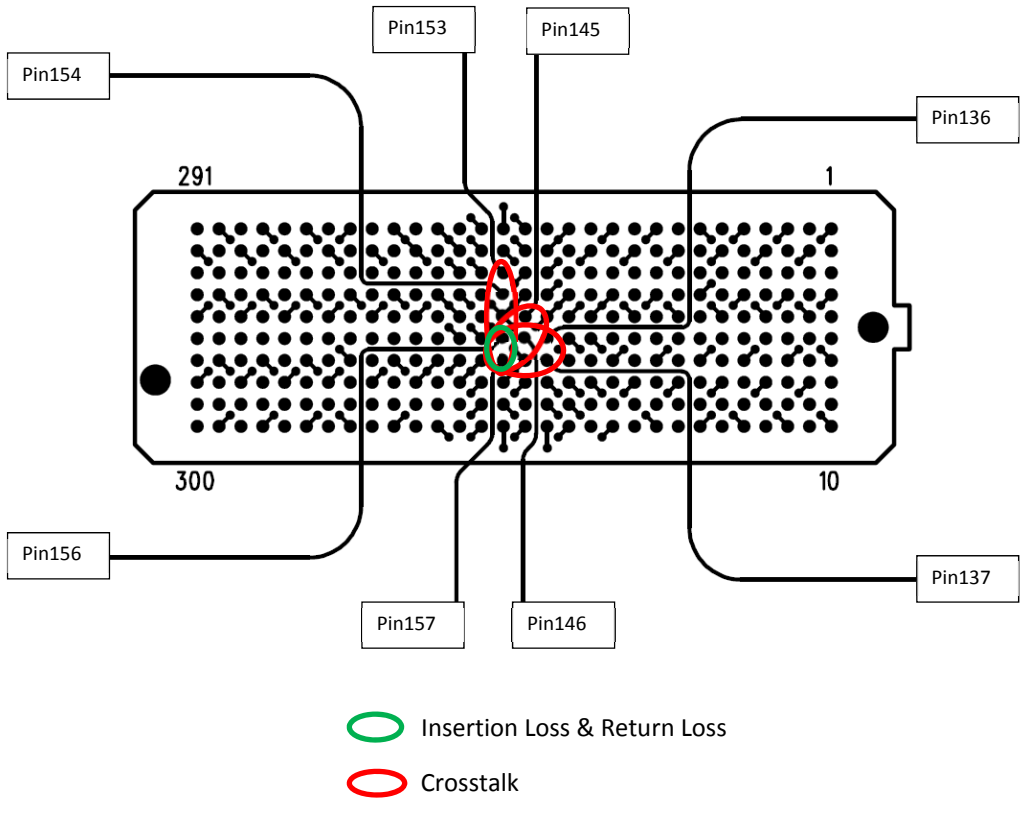
Differential Optimal Vertical Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 5 - Differential High Density Vertical Performance			
Test Parameter	**Driver**	**Receiver**	
Insertion Loss	SEAM_156,157	SEAF_156,157	3dB@ 11.45 GHz
Return Loss	SEAM_156,157	SEAM_156,157	>10dB to 6.3 GHz
Near-End Crosstalk	SEAM_156,157	SEAM_136,137	<-20dB to 20 GHz
	SEAM_156,157	SEAM_145,146	<-20dB to 16.1 GHz
	SEAM_156,157	SEAM_153,154	<-20dB to 20 GHz
Far-End Crosstalk	SEAM_156,157	SEAF_136,137	<-20dB to 20 GHz
	SEAM_156,157	SEAF_145,146	<-20dB to 20 GHz
	SEAM_156,157	SEAF_153,154	<-20dB to 20 GHz

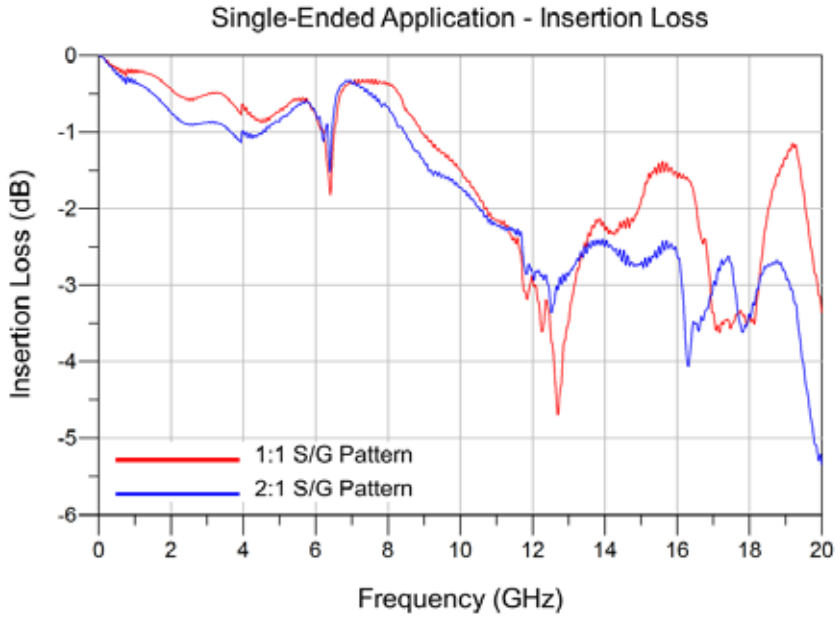
Differential High Density Vertical Pin Map

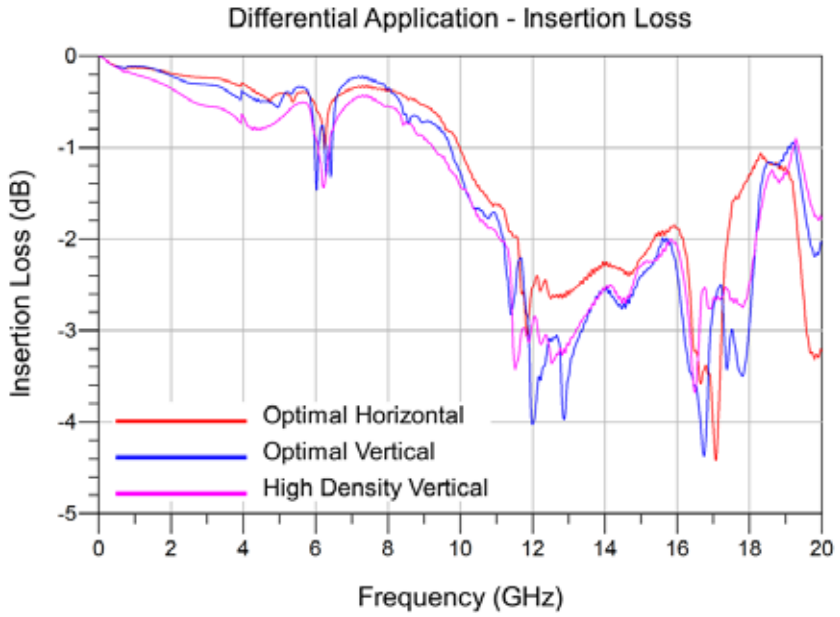


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Bandwidth Charts – Single-Ended & Differential Insertion Loss

SEAM/SEAF Array Series





Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Time Domain Data Summary

Table 6 – Single-End Impedance (Ω) – 1:1 S/G Pattern					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	62.92	61.74	60.37	55.27	52.53
Minimum Impedance	46.50	47.09	47.74	47.96	48.89

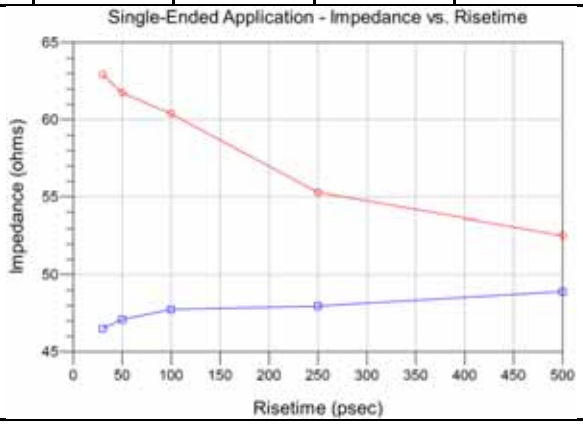
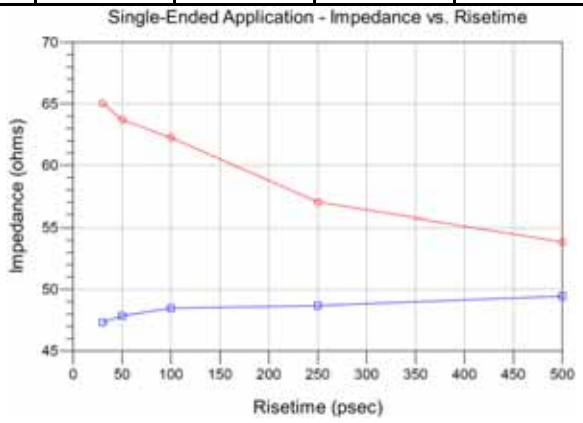


Table 7 – Single-End Impedance (Ω) – 2:1 S/G Pattern					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	65.05	63.70	62.25	57.02	53.85
Minimum Impedance	47.31	47.84	48.46	48.67	49.44



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 8 – Differential Impedance (Ω) – Optimal Horizontal					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	103.15	102.12	101.19	99.29	98.57
Minimum Impedance	85.96	87.66	91.43	94.82	95.75

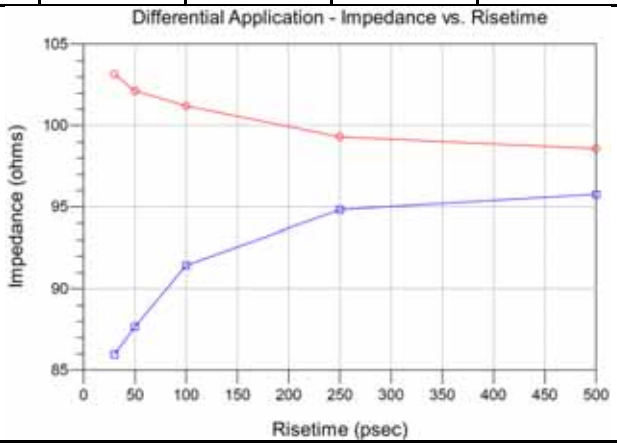
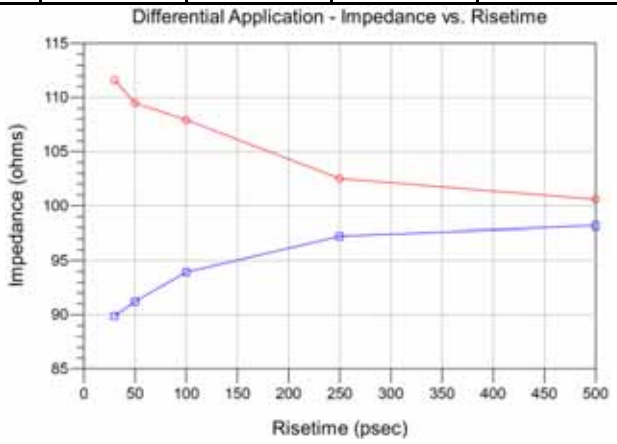
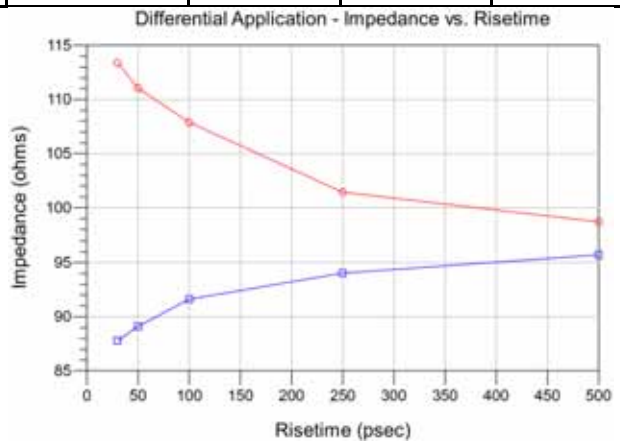


Table 9 – Differential Impedance (Ω) – Optimal Vertical					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	111.62	109.48	107.93	102.49	100.57
Minimum Impedance	89.88	91.23	93.94	97.25	98.18



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

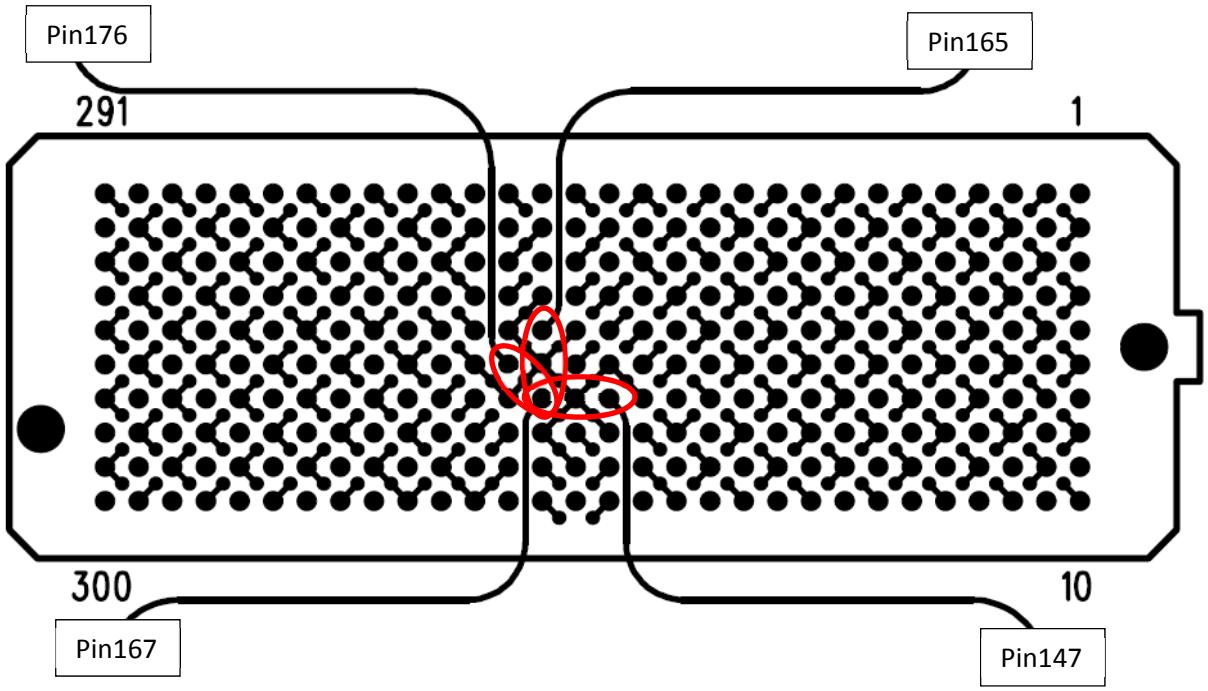
Table 10 – Differential Impedance (Ω) – High Density Vertical					
Signal Risetime	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
Maximum Impedance	113.40	111.04	107.87	101.42	98.68
Minimum Impedance	87.79	89.11	91.62	94.03	95.73



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 11 - Single-Ended Crosstalk (%) – 1:1 S/G Pattern							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	SEAM_167	SEAM_147	0.60	0.51	0.44	0.28	0.18
	SEAM_167	SEAM_165	0.28	0.24	0.18	0.12	<0.1
	SEAM_167	SEAM_176	2.41	2.33	2.19	1.40	0.82
FEXT	SEAM_167	SEAF_147	0.72	0.47	0.30	0.18	0.11
	SEAM_167	SEAF_165	0.20	0.18	0.16	0.10	<0.1
	SEAM_167	SEAF_176	1.39	0.95	0.74	0.43	0.27

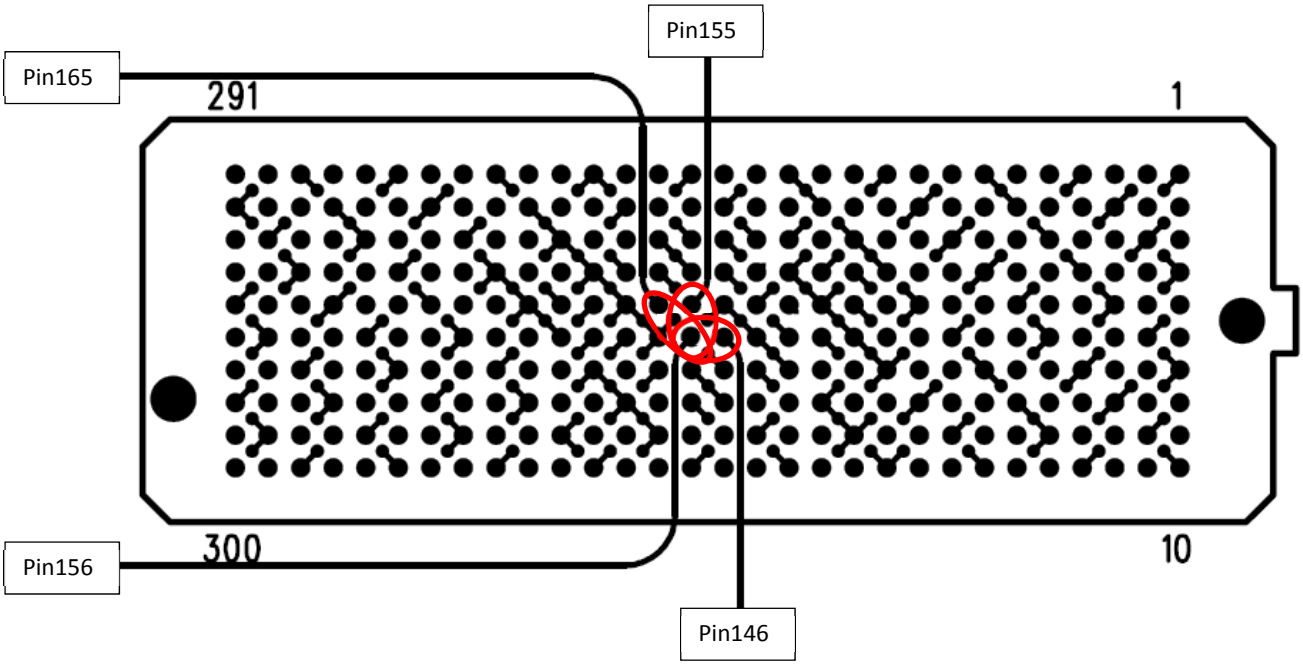
Single-Ended 1:1 S/G Pattern Crosstalk Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 12 - Single-Ended Crosstalk (%) – 2:1 S/G Pattern							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	SEAM_156	SEAM_146	13.89	13.18	12.14	7.72	4.33
	SEAM_156	SEAM_155	9.10	8.30	7.45	4.89	2.79
	SEAM_156	SEAM_165	3.62	3.38	3.14	2.17	1.31
FEXT	SEAM_156	SEAF_146	5.20	4.92	4.49	2.87	1.75
	SEAM_156	SEAF_155	5.29	3.88	3.53	2.32	1.40
	SEAM_156	SEAF_165	2.48	2.34	2.15	1.40	0.88

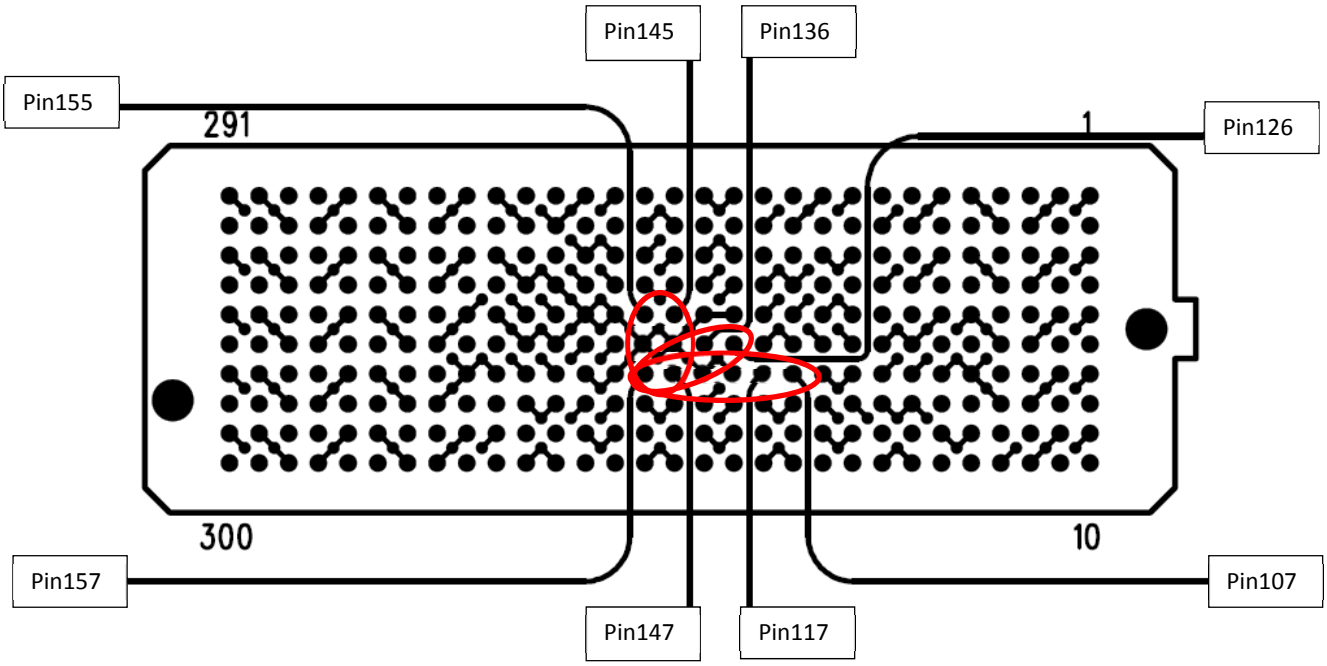
Single-Ended 2:1 S/G Pattern Crosstalk Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 13 - Differential Crosstalk (%) – Optimal Horizontal							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	SEAM_147,157	SEAM_107,117	0.29	0.15	<0.1	<0.1	<0.1
	SEAM_147,157	SEAM_126,136	0.90	0.84	0.76	0.47	0.26
	SEAM_147,157	SEAM_145,155	0.15	<0.1	<0.1	<0.1	<0.1
FEXT	SEAM_147,157	SEAF_107,117	0.73	0.48	0.25	0.11	<0.1
	SEAM_147,157	SEAF_126,136	0.38	0.16	<0.1	<0.1	<0.1
	SEAM_147,157	SEAF_145,155	0.15	<0.1	<0.1	<0.1	<0.1

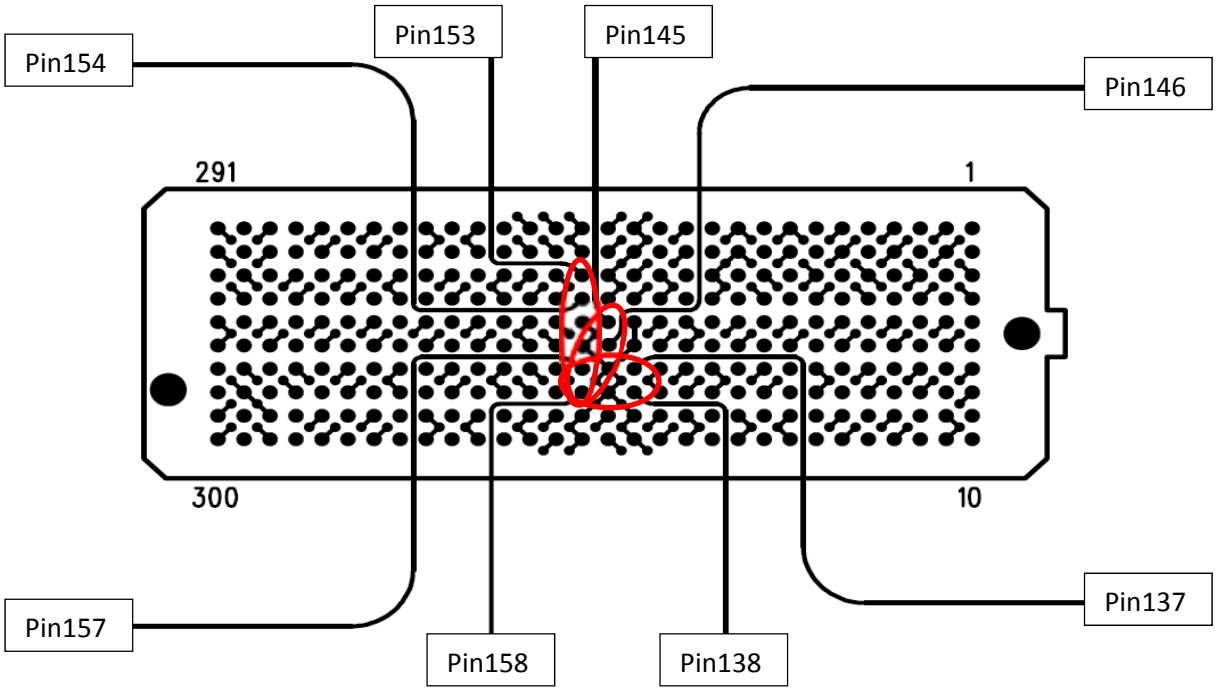
Differential Optimal Horizontal Crosstalk Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 14 - Differential Crosstalk (%) – Optimal Vertical							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	SEAM_157,158	SEAM_137,138	0.38	0.29	0.21	0.13	<0.1
	SEAM_157,158	SEAM_145,146	1.03	0.96	0.88	0.55	0.28
	SEAM_157,158	SEAM_153,154	0.23	0.13	<0.1	<0.1	<0.1
FEXT	SEAM_157,158	SEAF_137,138	0.33	0.20	0.12	<0.1	<0.1
	SEAM_157,158	SEAF_145,146	0.37	0.24	0.17	<0.1	<0.1
	SEAM_157,158	SEAF_153,154	0.28	0.18	<0.1	<0.1	<0.1

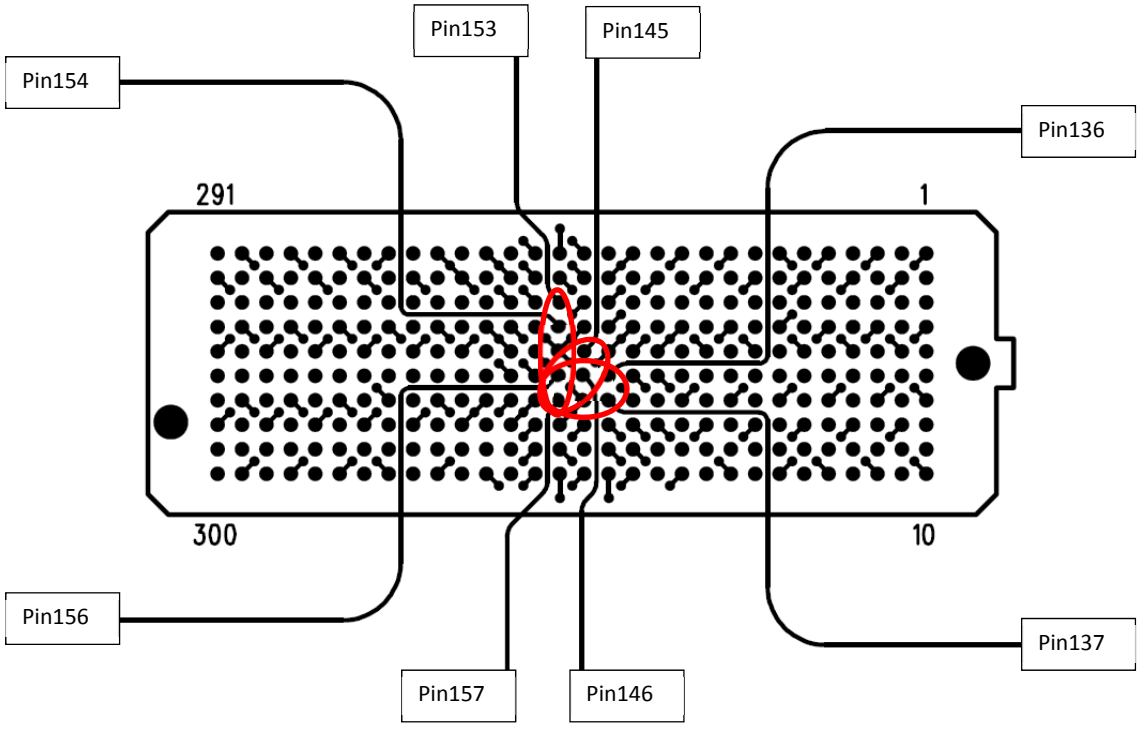
Differential Optimal Vertical Crosstalk Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 15 - Differential Crosstalk (%) – High Density Vertical							
Input(tr)	**Driver**	**Receiver**	**30 ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**
NEXT	SEAM_156,157	SEAM_136,137	0.66	0.58	0.56	0.43	0.27
	SEAM_156,157	SEAM_145,146	4.13	4.02	3.41	2.08	1.15
	SEAM_156,157	SEAM_153,154	0.13	0.12	<0.1	<0.1	<0.1
FEXT	SEAM_156,157	SEAF_136,137	0.91	0.77	0.68	0.42	0.25
	SEAM_156,157	SEAF_145,146	1.06	0.96	0.82	0.45	0.25
	SEAM_156,157	SEAF_153,154	0.21	0.15	0.10	<0.1	<0.1

Differential High Density Vertical Crosstalk Pin Map



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Table 16 - Propagation Delay (Mated Connector)	
Single-Ended: 1:1 S/G	90ps
Single-Ended: 2:1 S/G	89ps
Differential: Optimal Horizontal	84ps
Differential: Optimal Vertical	83ps
Differential: High Density Vertical	83ps

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector pair and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connector's true performance. Such connection effects are minimized by using high performance test cables and adapters. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differentially and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield, is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

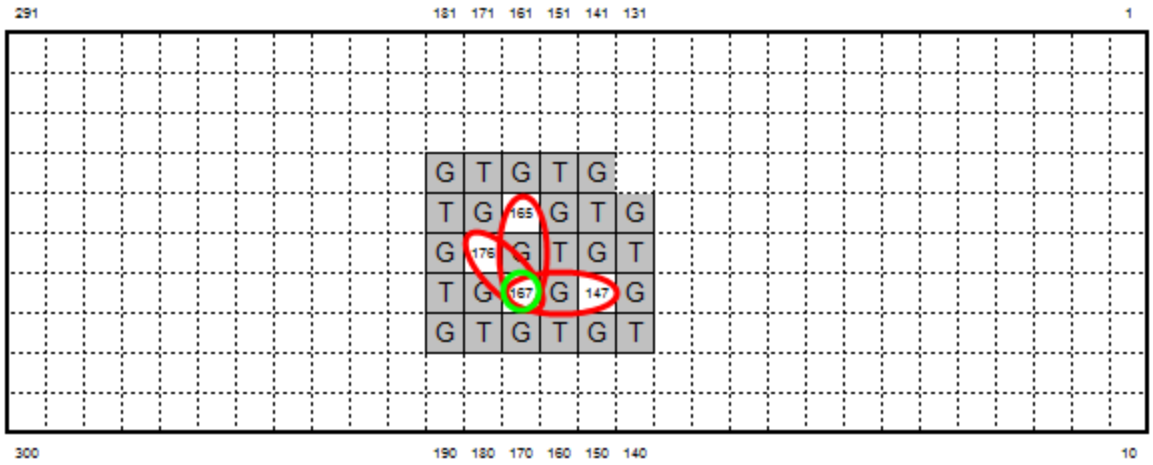
In general, the more pins dedicated to ground, the better electrical performance will be. However, dedicating pins to ground reduces signal density of a connector. Therefore, care must be taken when choosing signal/ground ratios in cost or density-sensitive applications.

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

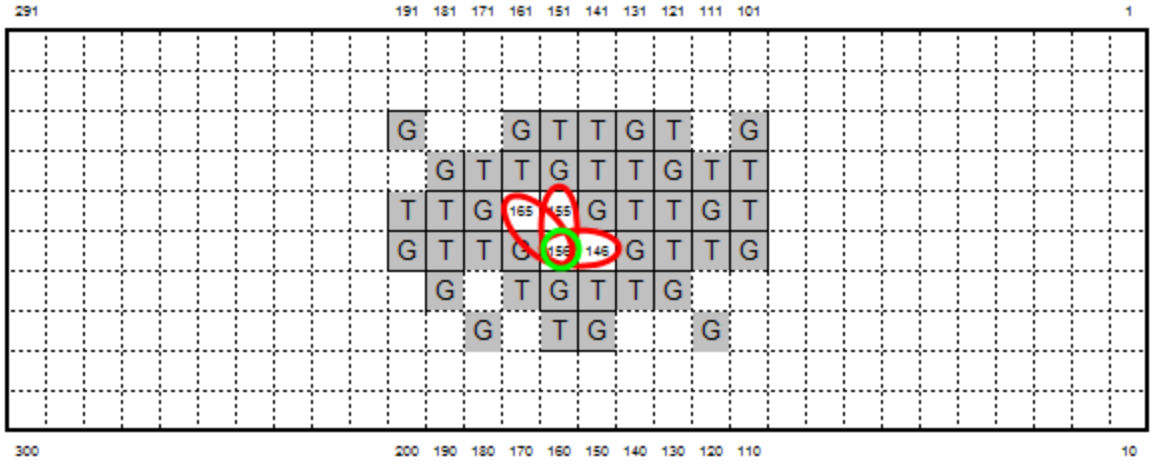
For this connector, the following array configurations are evaluated:

	Open pin field	G	Grounded pin field
	Signal pin field	T	50 ohm termination field

Single-Ended 1:1 S/G Pattern



Single-Ended 2:1 S/G Pattern



Single-Ended Impedance (denoted by green circles):

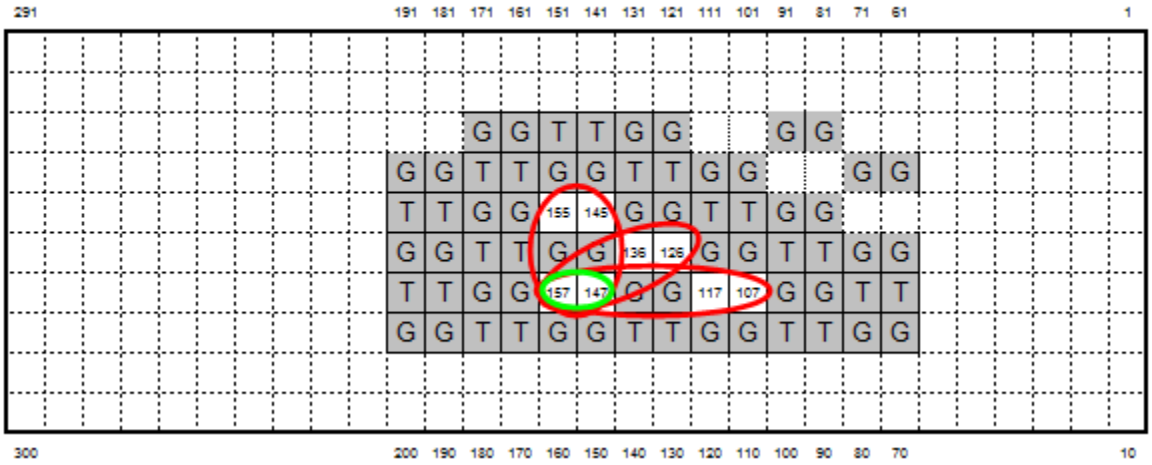
- 1:1 S/G ratio
- 2:1 S/G ratio

Single-Ended Crosstalk (denoted by red circles):

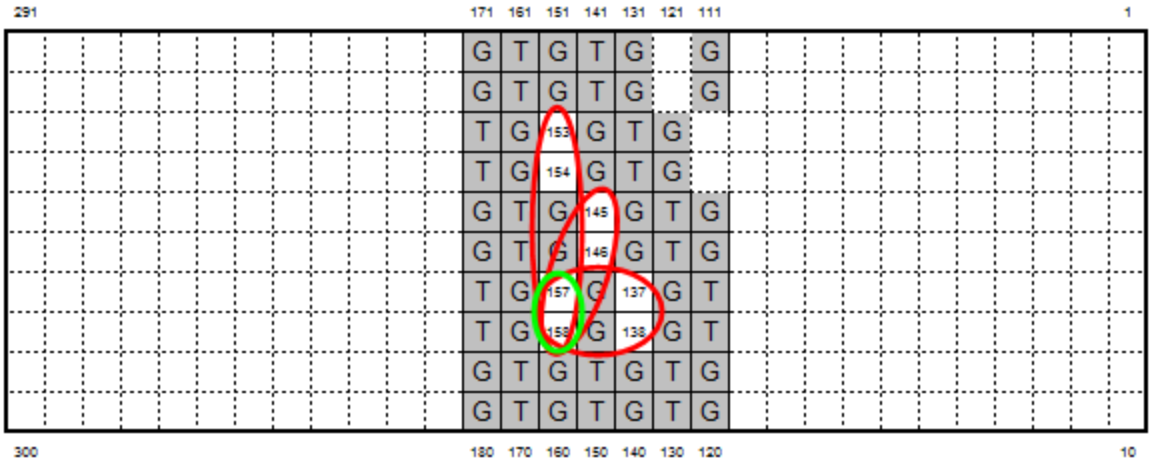
- 1:1 S/G ratio
- 2:1 S/G ratio

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Optimal Horizontal

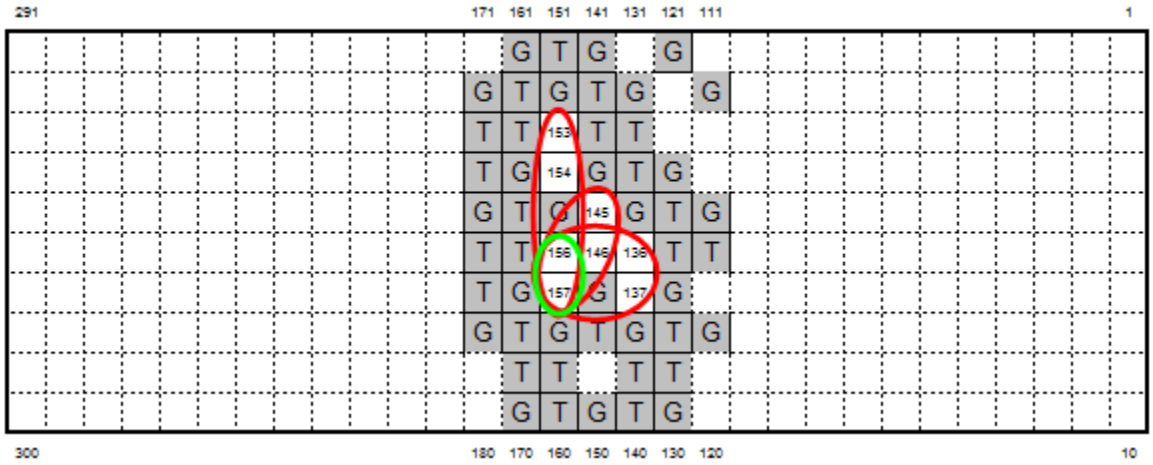


Differential Optimal Vertical



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential High Density Vertical



Differential Impedance (denoted by green circles)**:**

- Optimal Horizontal
- Optimal Vertical
- High Density Vertical

Differential Crosstalk (denoted by red circles)**:**

- Optimal Horizontal
- Optimal Vertical
- High Density Vertical

Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of “SSSS”, or four adjacent single ended signals might be encountered as opposed to the “GSG” and “GSSG” configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of the interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 ps. Generally, this should demonstrate worst-case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30ps and 500ps.

For this report, measured rise times were at 10%-90% signal levels.

Frequency Domain Data
Frequency Domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the Frequency Domain are Insertion Loss, Return Loss, and Near-End and Far-End Crosstalk. Other parameters or formats, such as VSWR or S-Parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate Impedance mismatch versus length, signal propagation time and crosstalk in a pulsed signal environment.

Impedance mismatch versus length is measured by DSA8200 Digital Serial Analyzer. Board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. The impedance data is provided in Appendix E of this report.

The measured S-Parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response for signal propagation time and crosstalk. The Time Domain procedure is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 10 mils of PCB trace on the SEAM and SEAF connector side each. Delay is measured at 100 picoseconds signal rise-time. De-

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

lay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

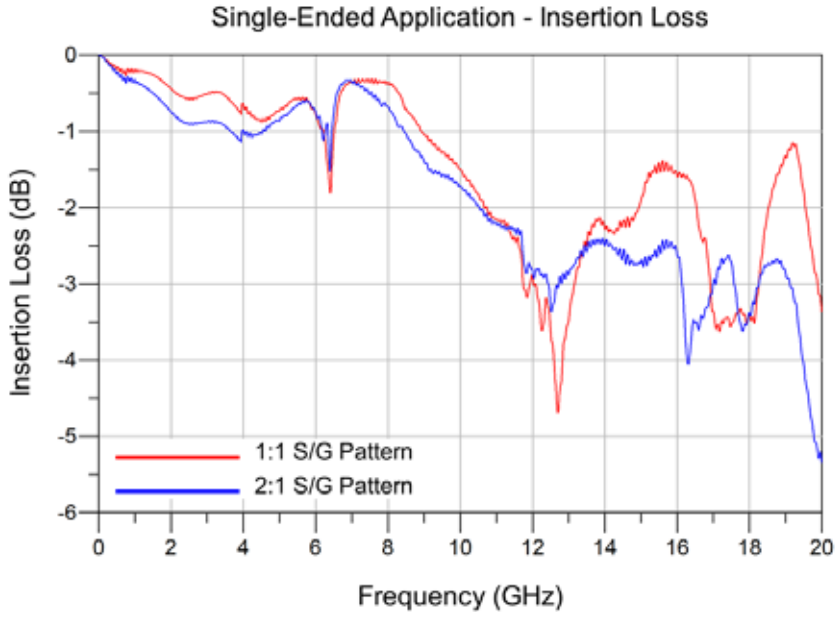
As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

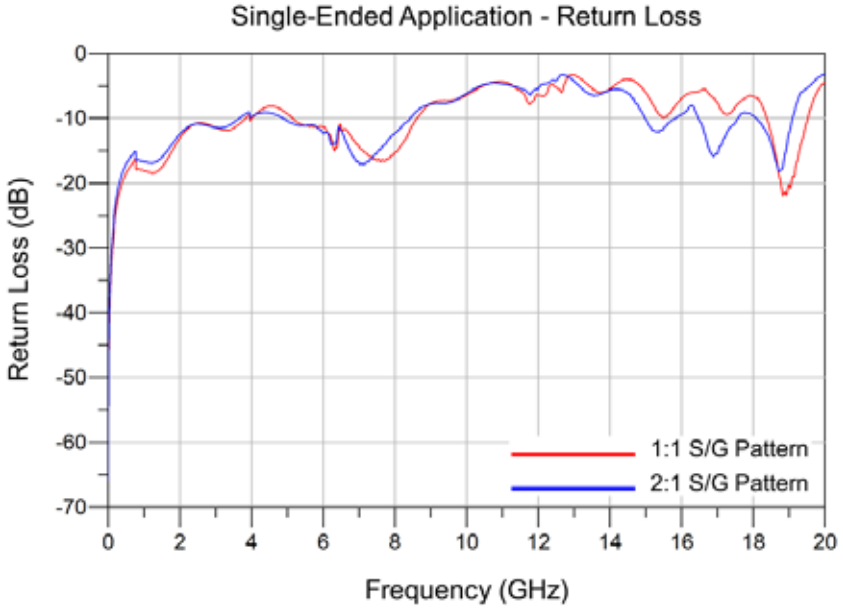
Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss

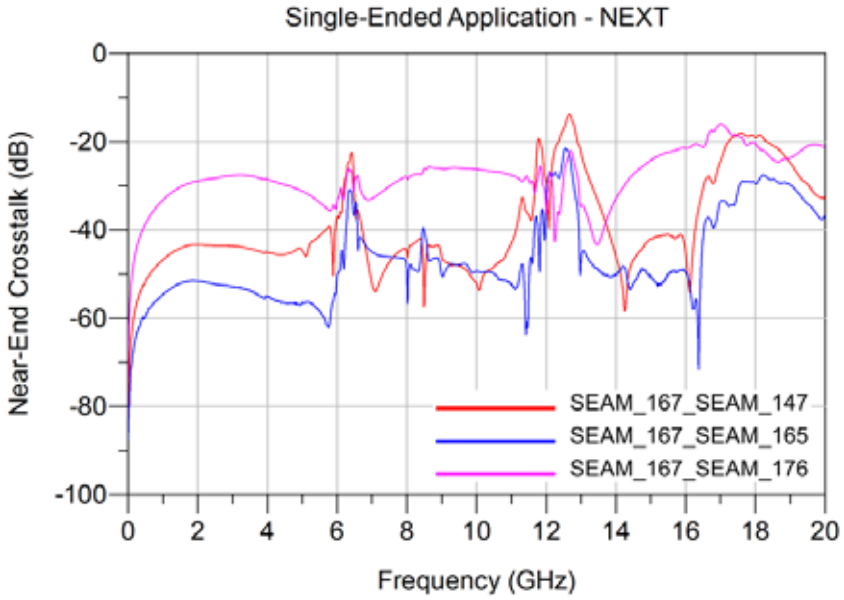


Single-Ended Application – Return Loss

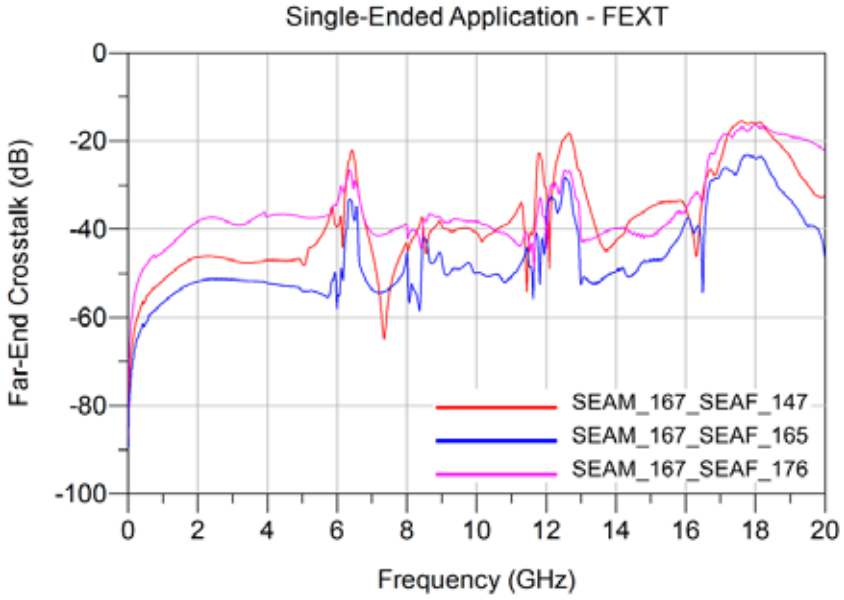


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 1:1 S/G Pattern Application – NEXT

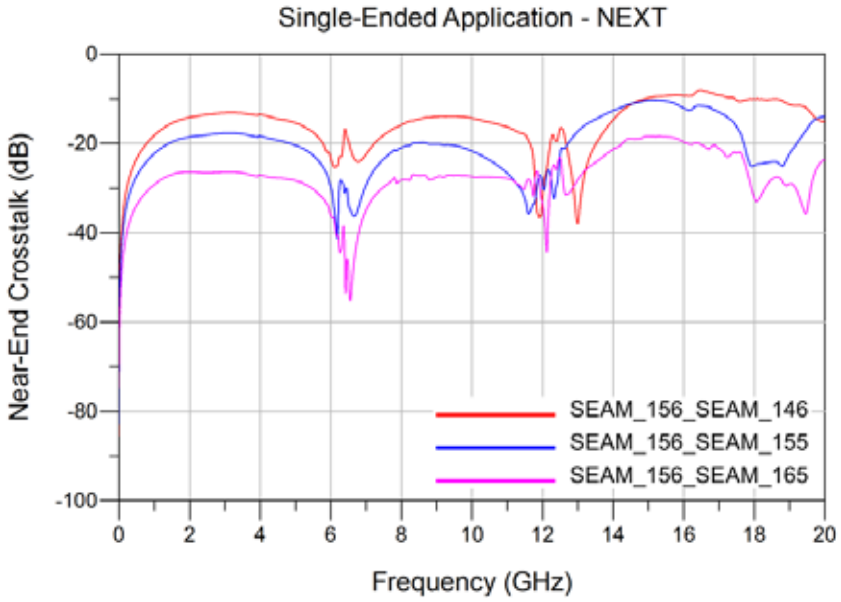


Single-Ended 1:1 S/G Pattern Application – FEXT

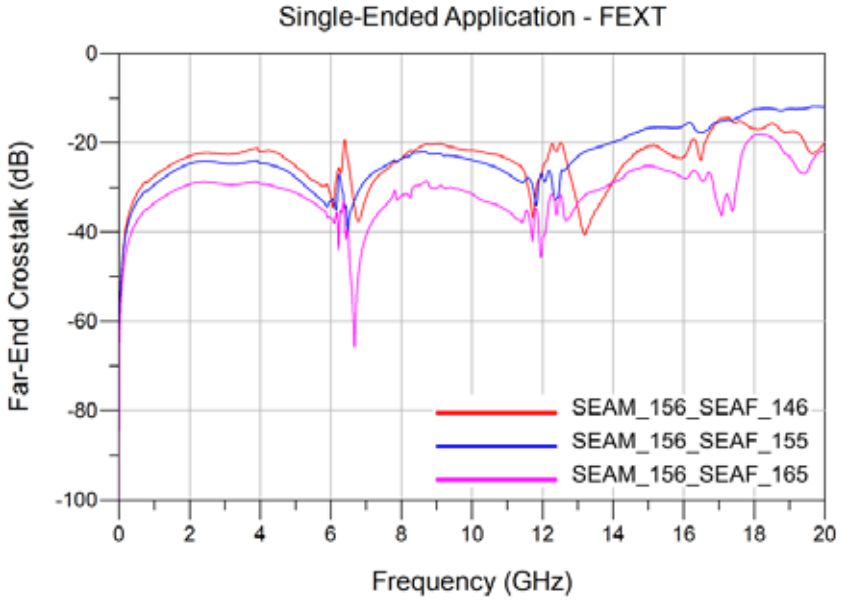


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 2:1 S/G Pattern Application – NEXT

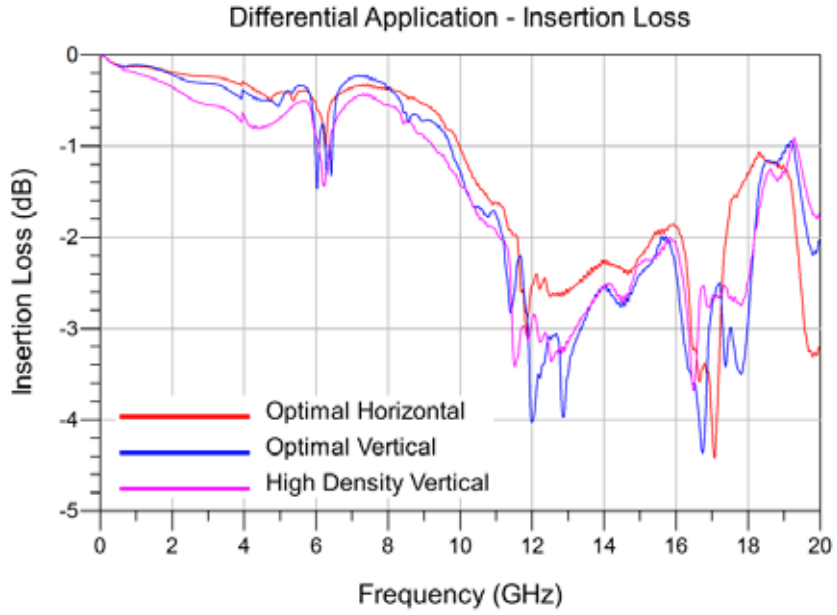


Single-Ended 2:1 S/G Pattern Application – FEXT

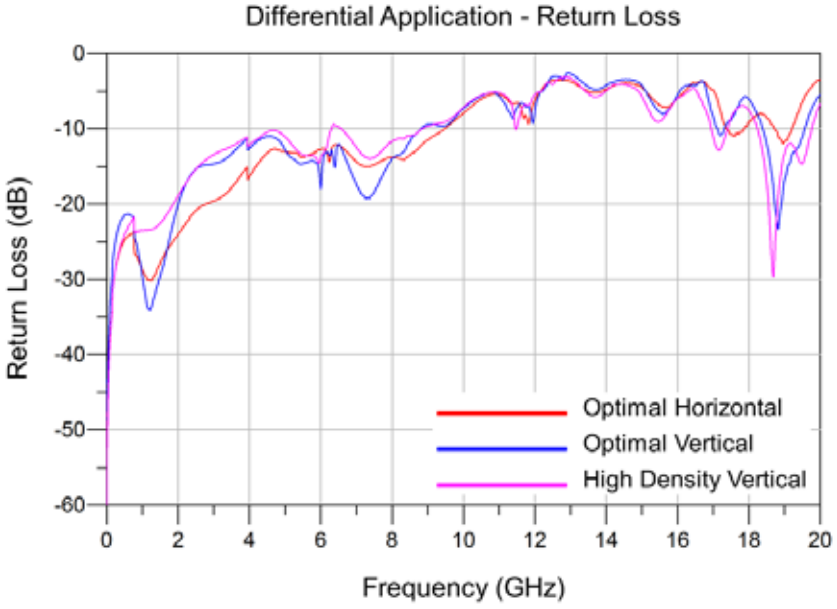


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Application – Insertion Loss

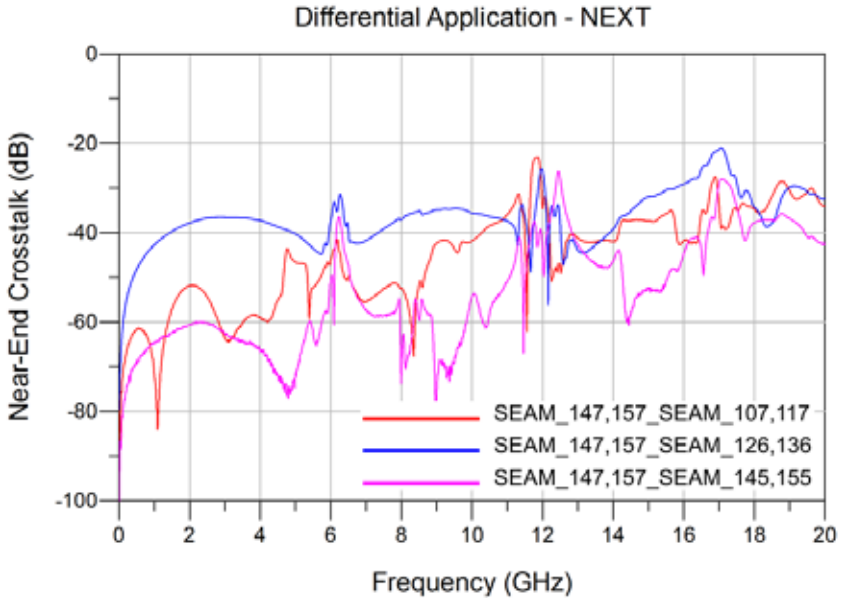


Differential Application – Return Loss

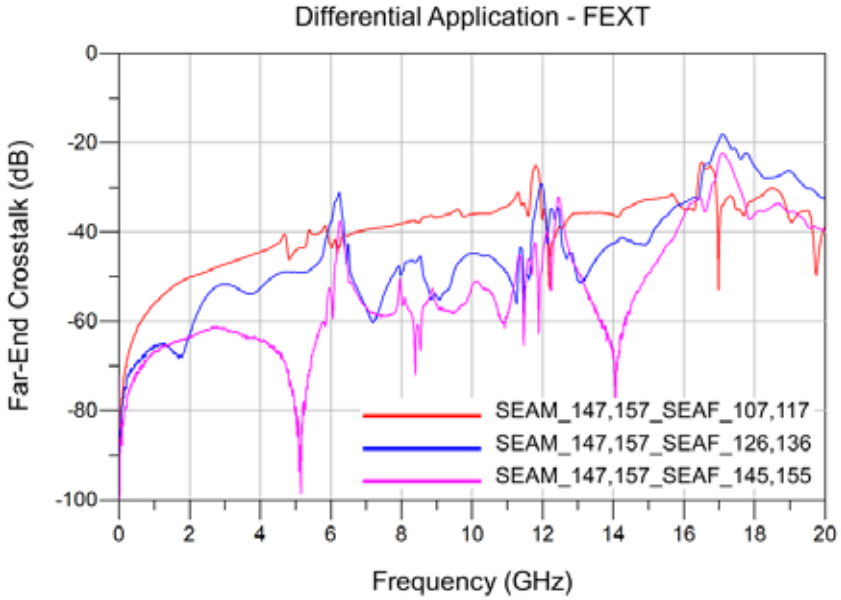


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Optimal Horizontal Application – NEXT

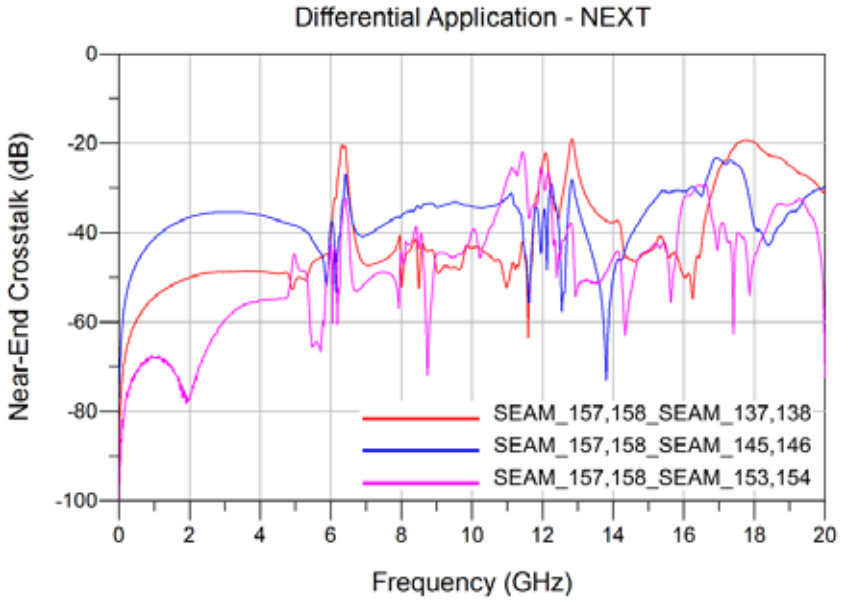


Differential Optimal Horizontal Application – FEXT

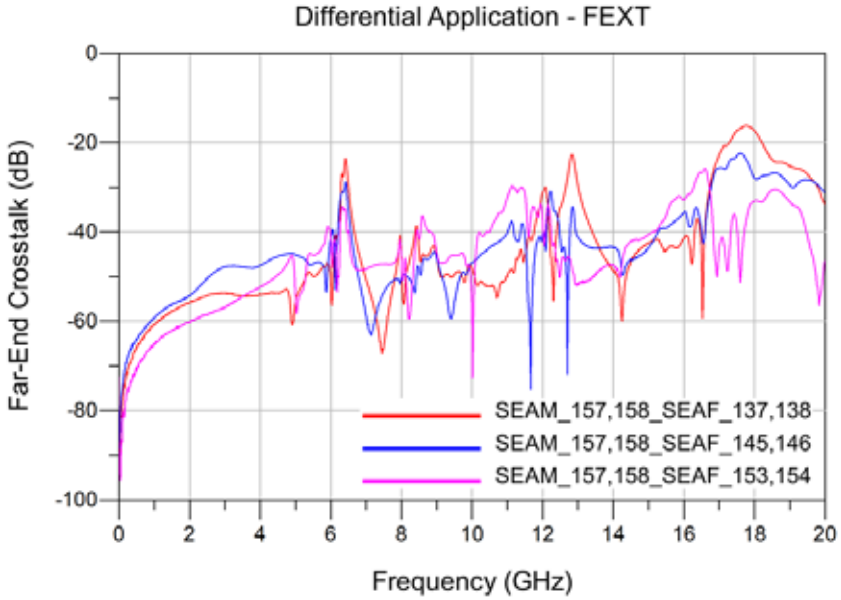


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Optimal Vertical Application – NEXT

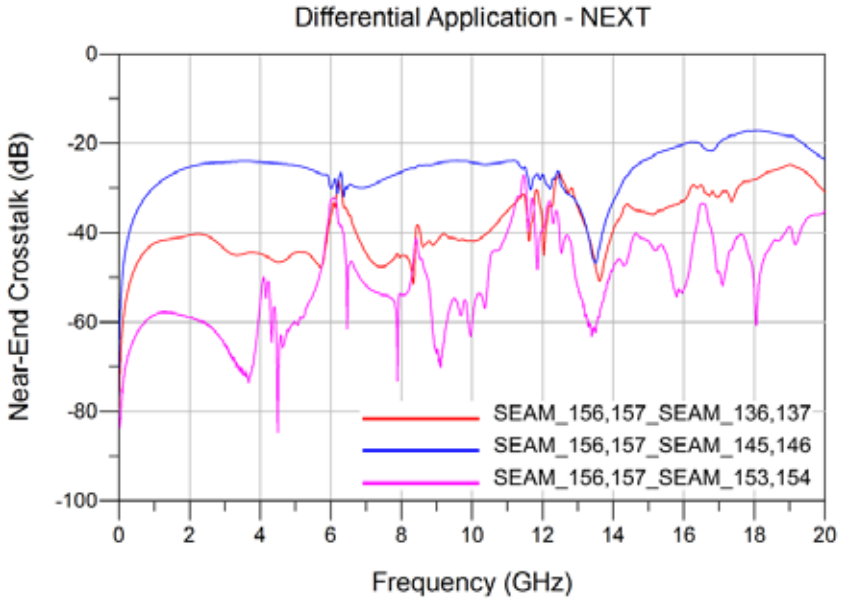


Differential Optimal Vertical Application – FEXT

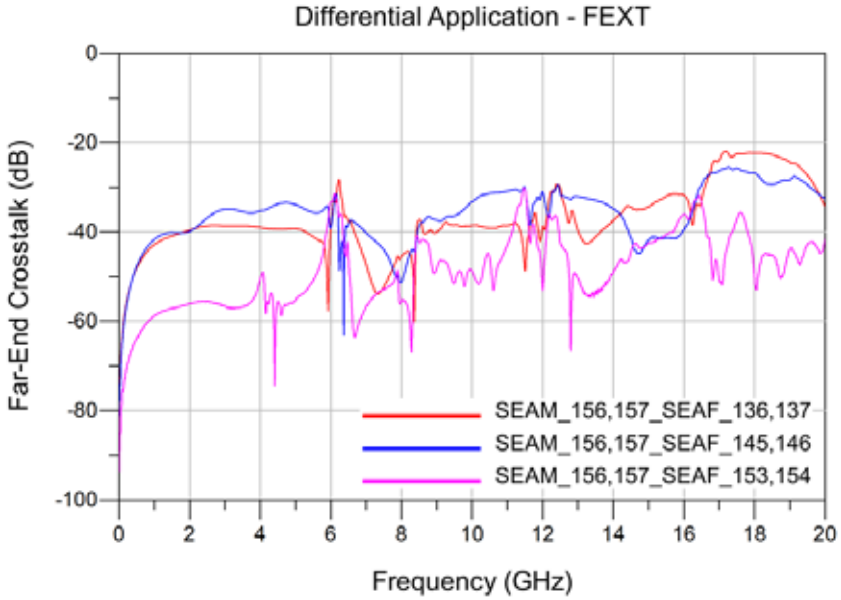


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential High Density Vertical Application – NEXT



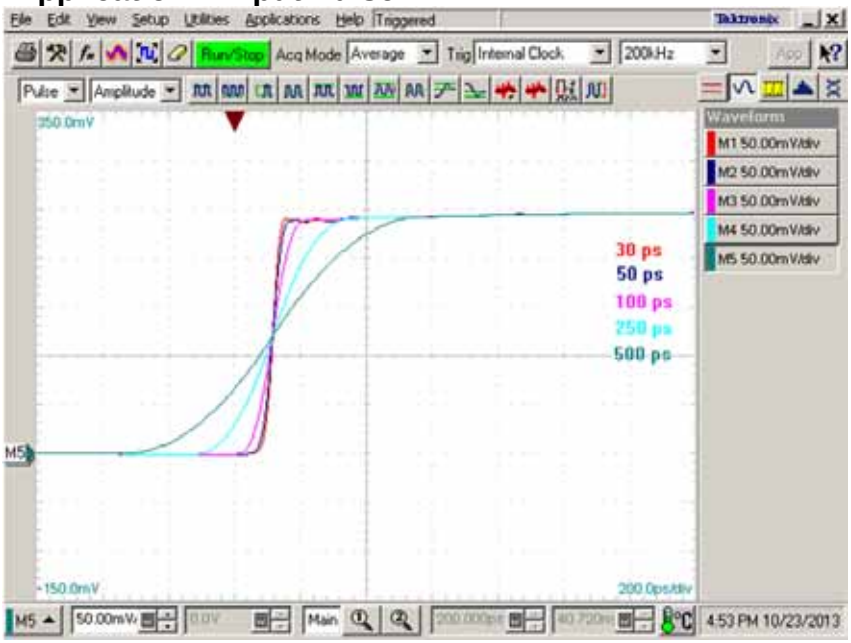
Differential High Density Vertical Application – FEXT



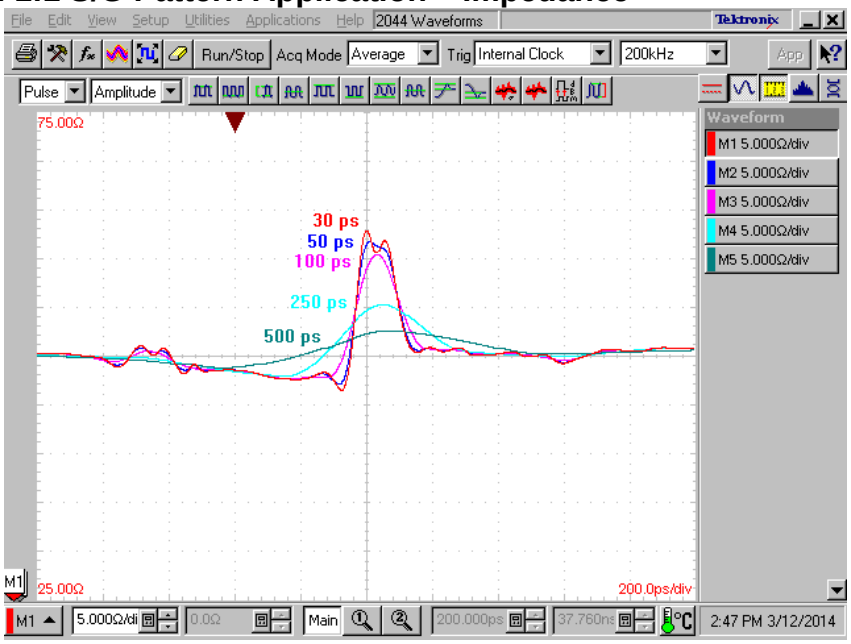
Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse

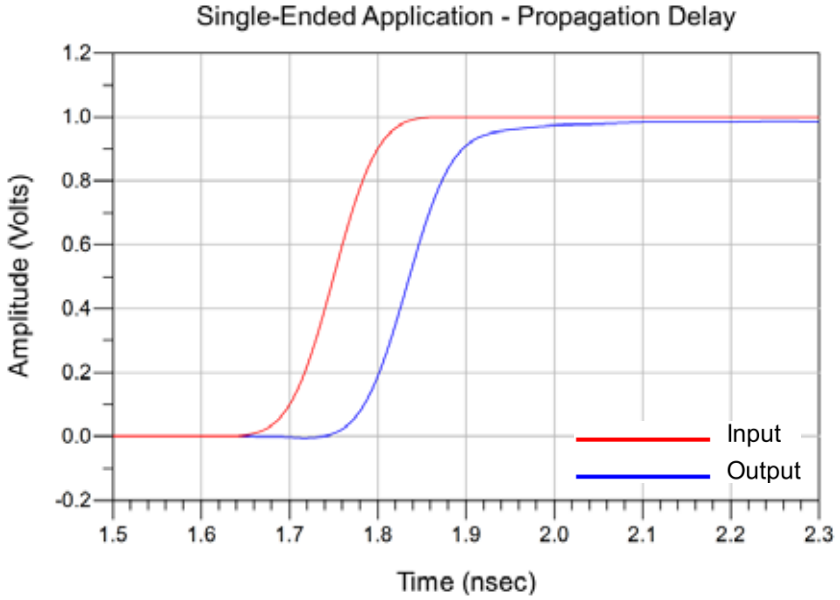


Single-Ended 1:1 S/G Pattern Application – Impedance

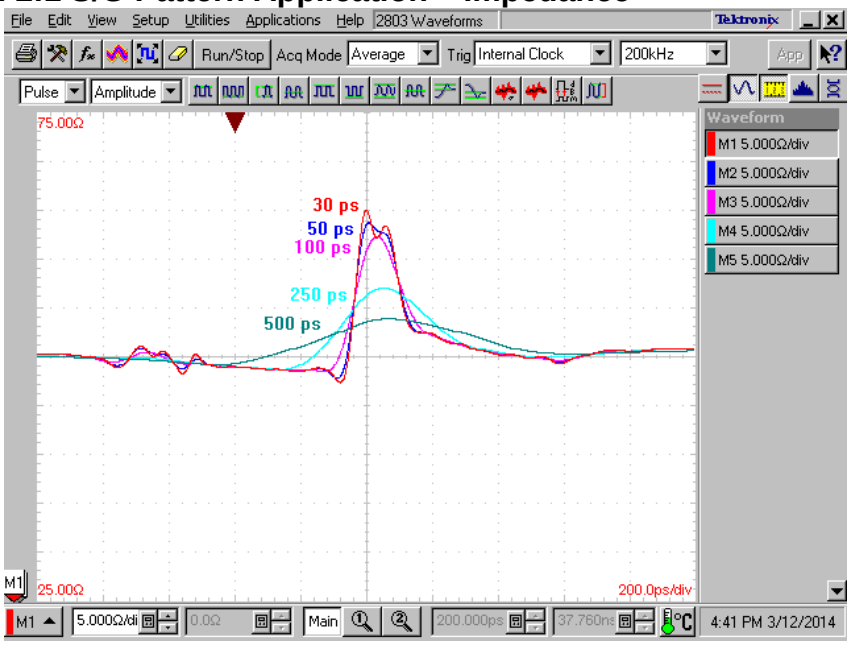


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 1:1 S/G Pattern Application – Propagation Delay

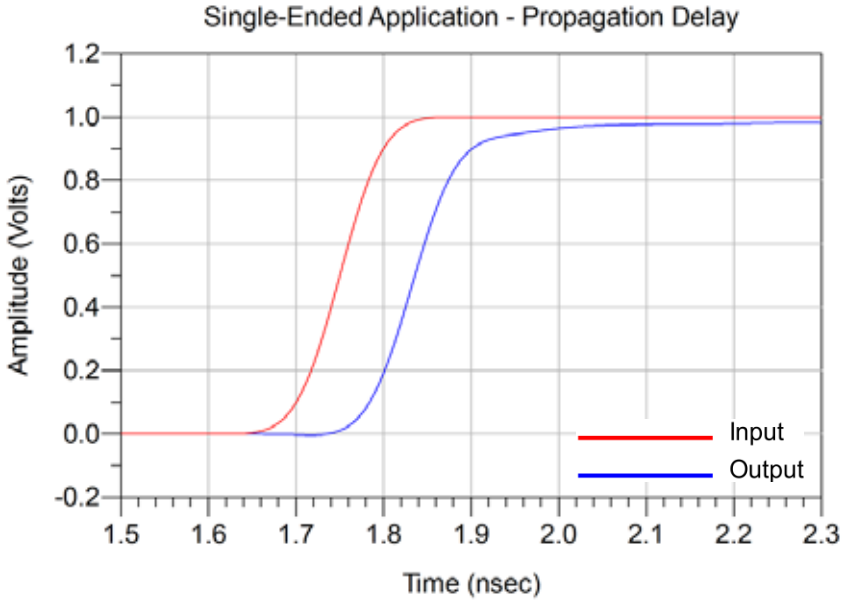


Single-Ended 2:1 S/G Pattern Application – Impedance

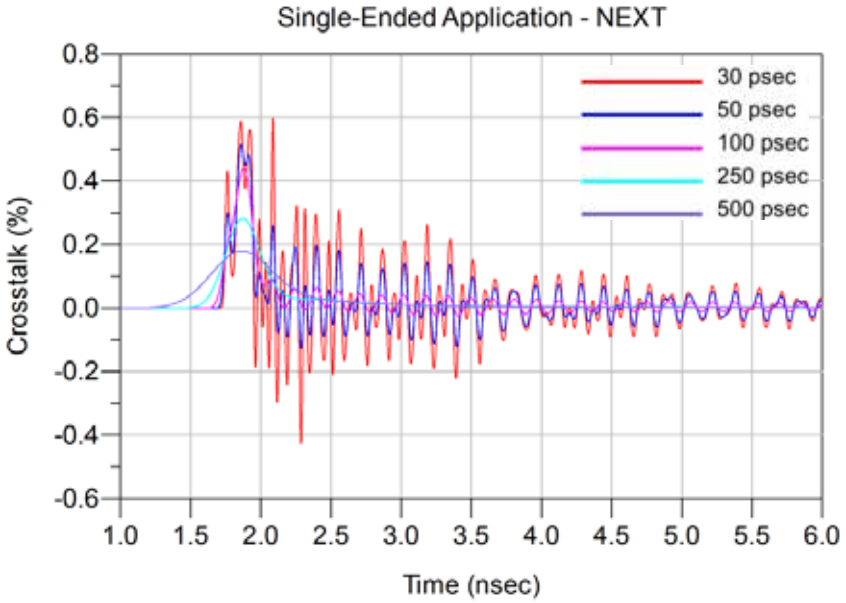


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 2:1 S/G Pattern Application – Propagation Delay

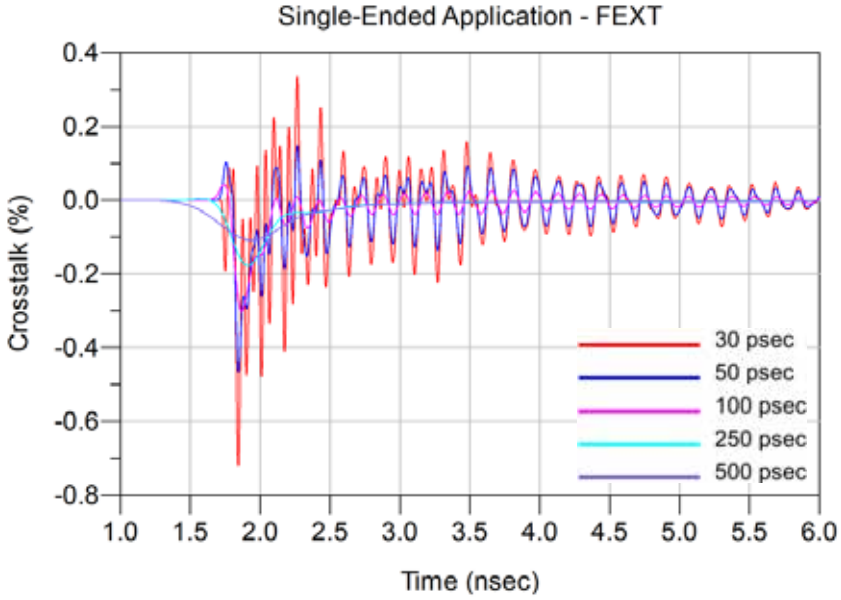


Single-Ended 1:1 S/G Pattern Application – NEXT, SEAM167_SEAM147

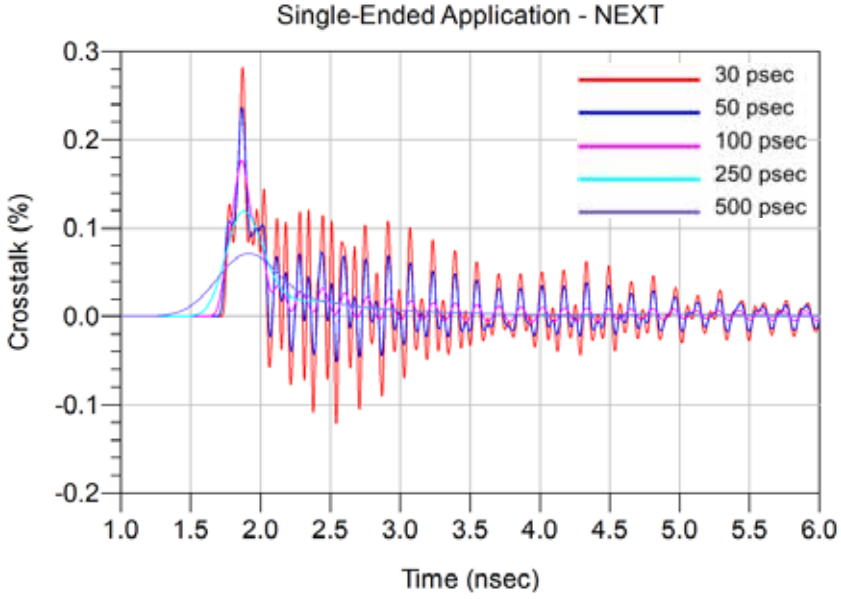


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 1:1 S/G Pattern Application – FEXT, SEAM167_SEAF147

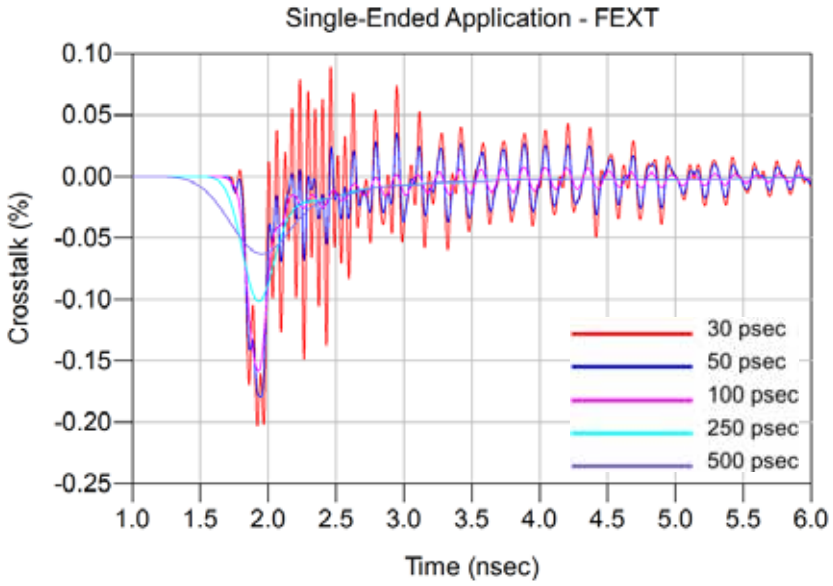


Single-Ended 1:1 S/G Pattern Application – NEXT, SEAM167_SEAM165

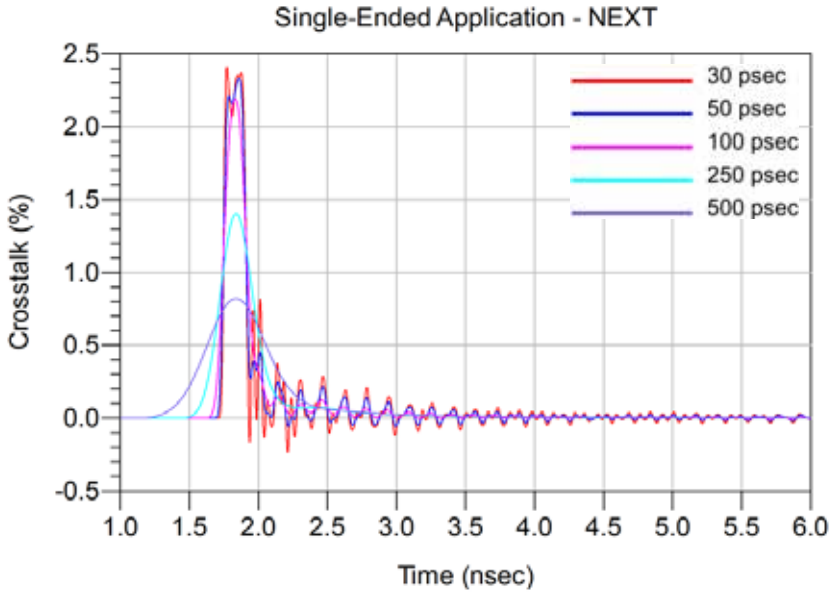


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 1:1 S/G Pattern Application – FEXT, SEAM167_SEAF165

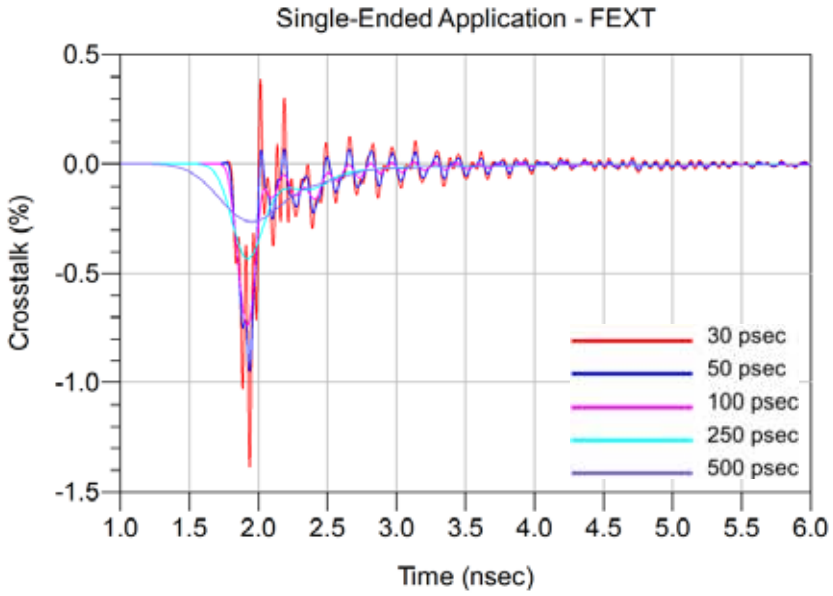


Single-Ended 1:1 S/G Pattern Application – NEXT, SEAM167_SEAM176

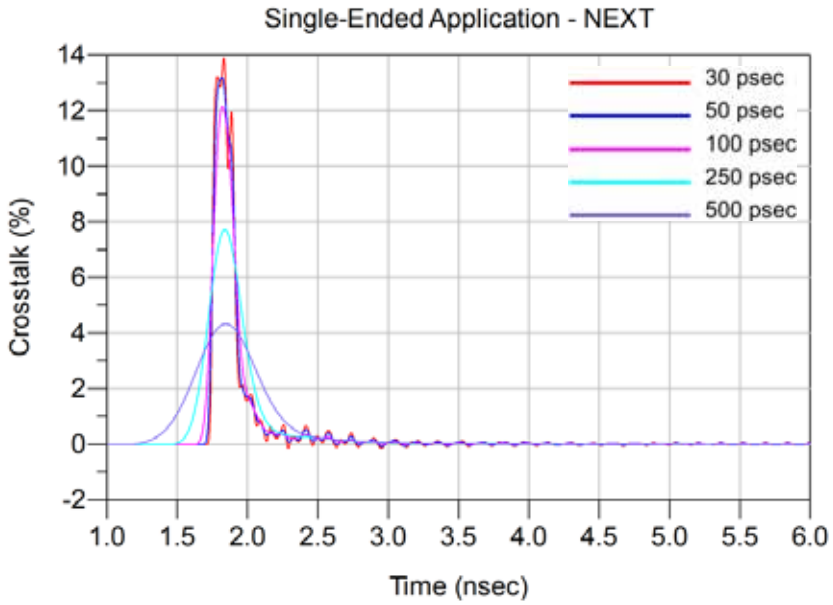


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 1:1 S/G Pattern Application – FEXT, SEAM167_SEAF176

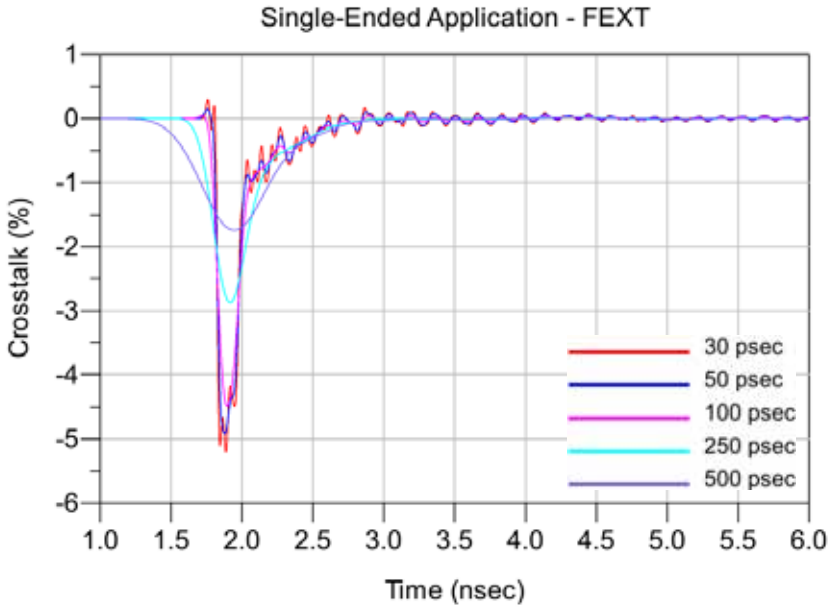


Single-Ended 2:1 S/G Pattern Application – NEXT, SEAM156_SEAM146

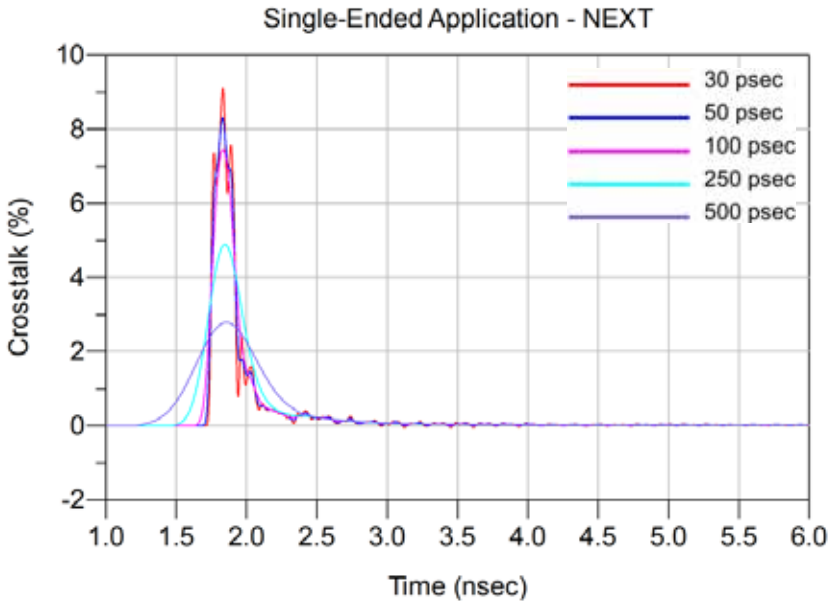


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 2:1 S/G Pattern Application – FEXT, SEAM156_SEAF146

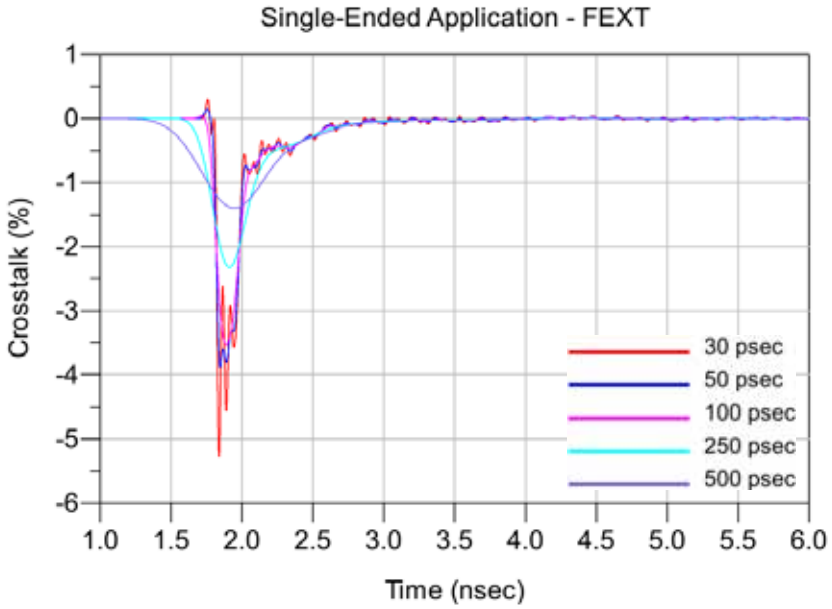


Single-Ended 2:1 S/G Pattern Application – NEXT, SEAM156_SEAM155

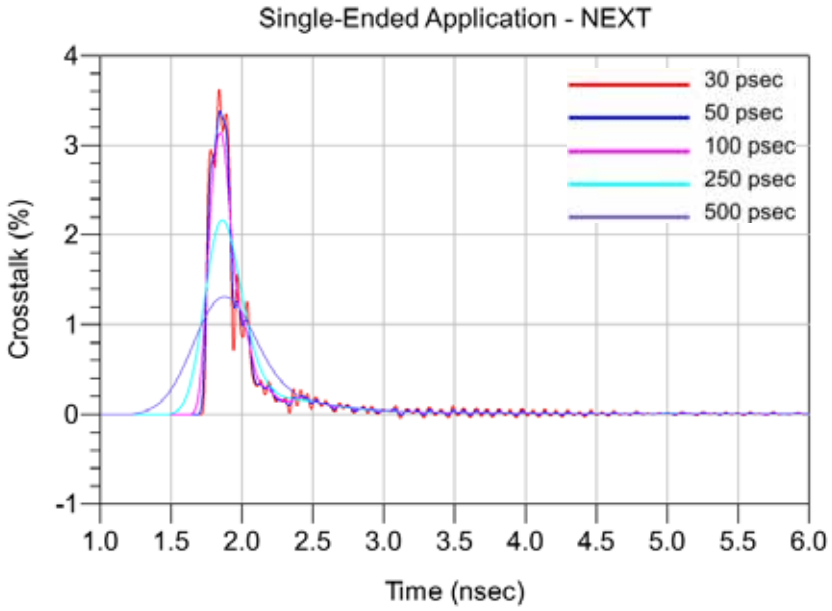


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 2:1 S/G Pattern Application – FEXT, SEAM156_SEAF155

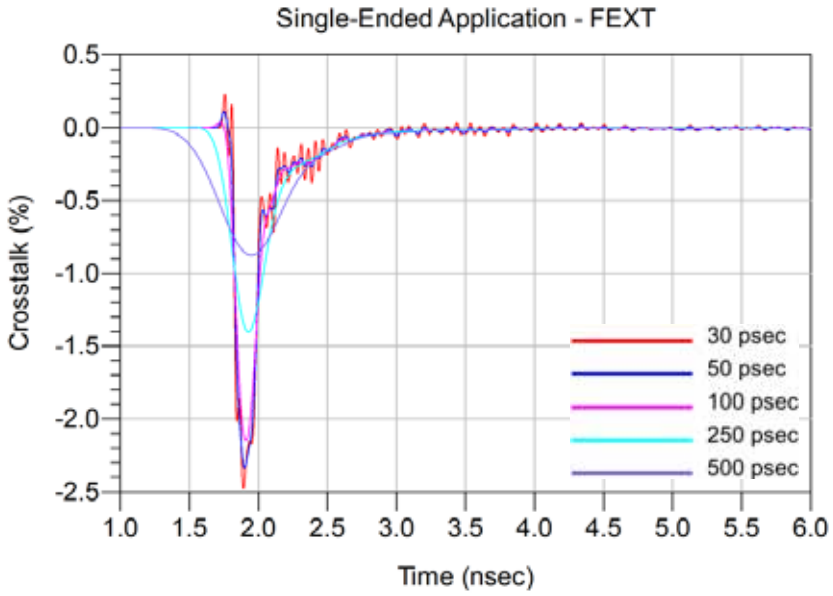


Single-Ended 2:1 S/G Pattern Application – NEXT, SEAM156_SEAM165

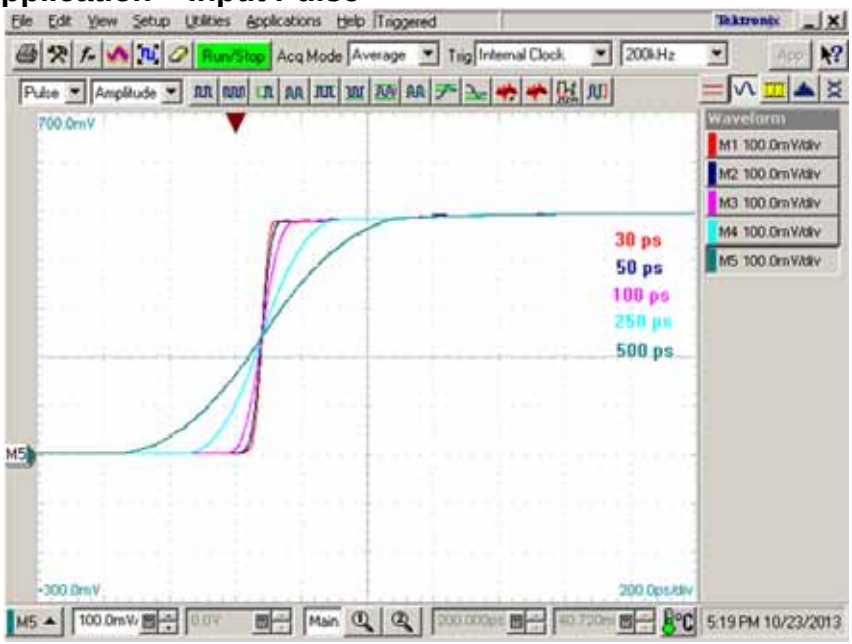


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Single-Ended 2:1 S/G Pattern Application – FEXT, SEAM156_SEAF165

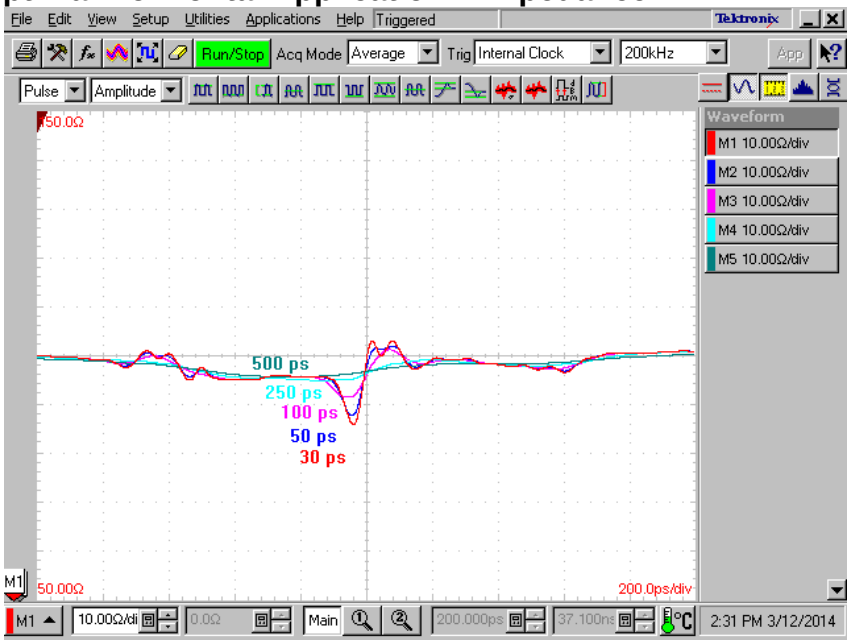


Differential Application – Input Pulse

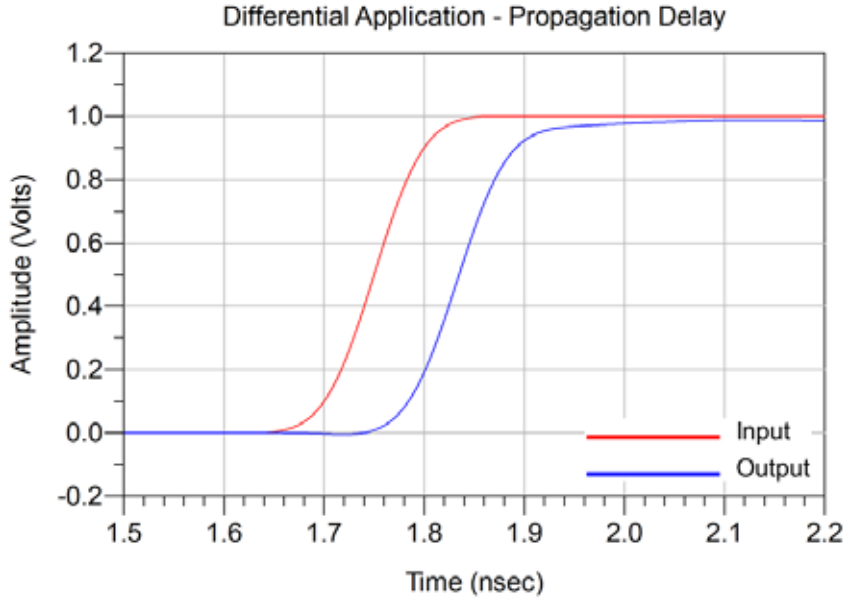


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Optimal Horizontal Application – Impedance

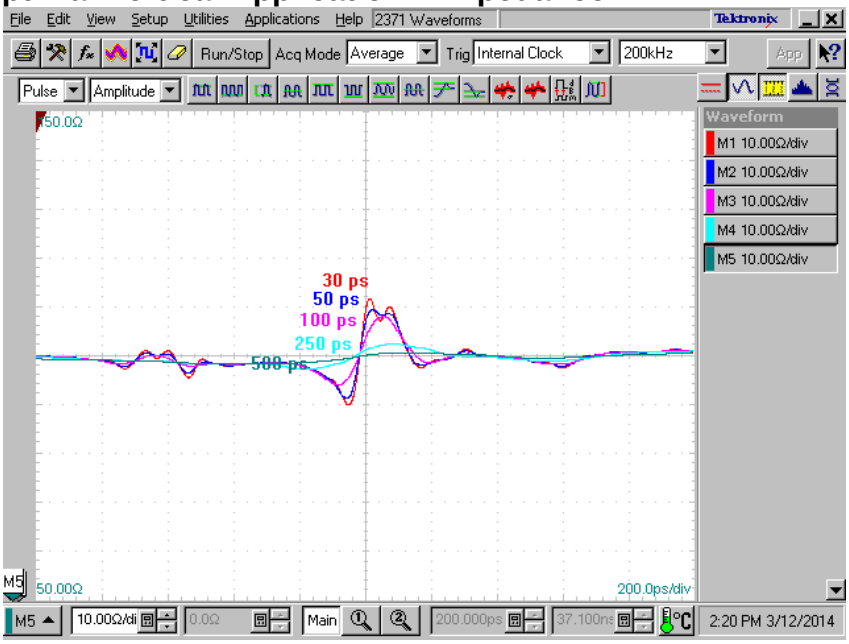


Differential Optimal Horizontal Application – Propagation Delay

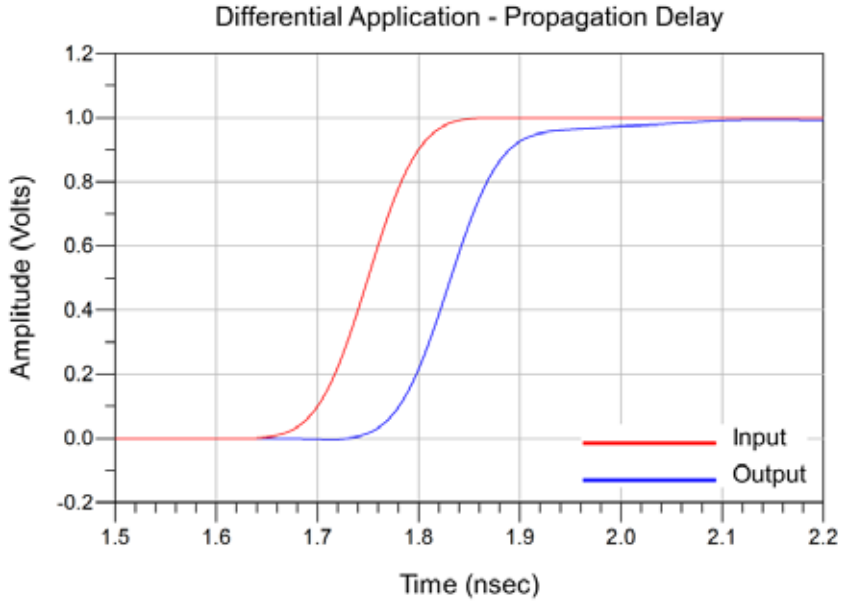


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential Optimal Vertical Application – Impedance

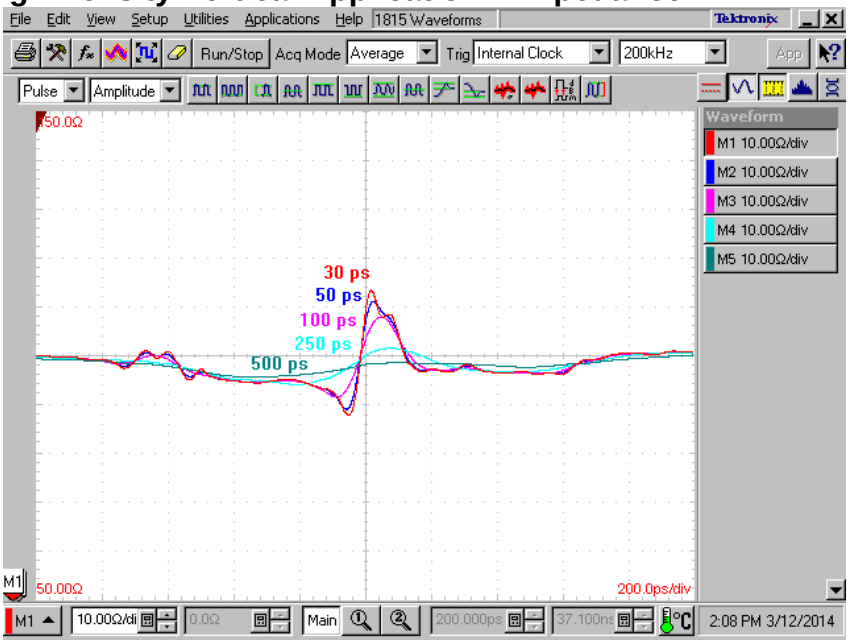


Differential Optimal Vertical Application – Propagation Delay

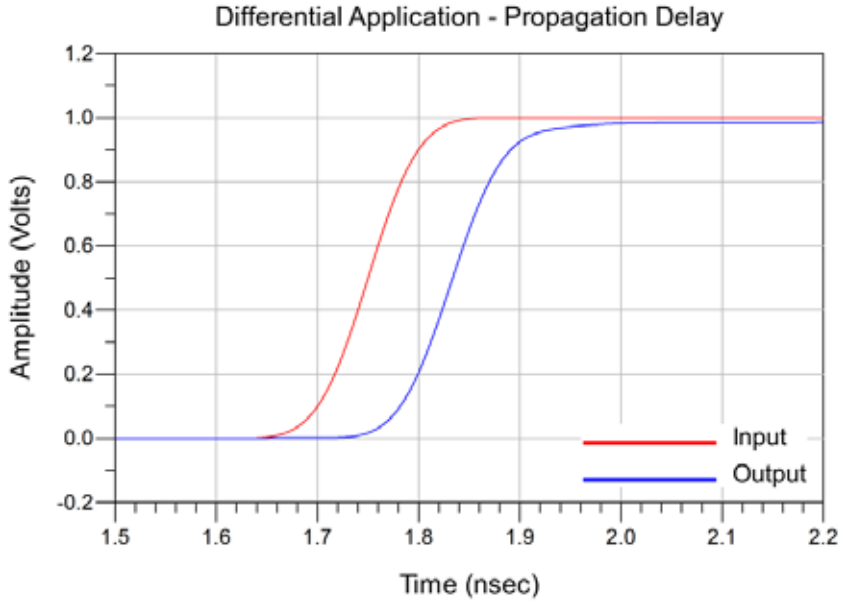


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Differential High Density Vertical Application – Impedance

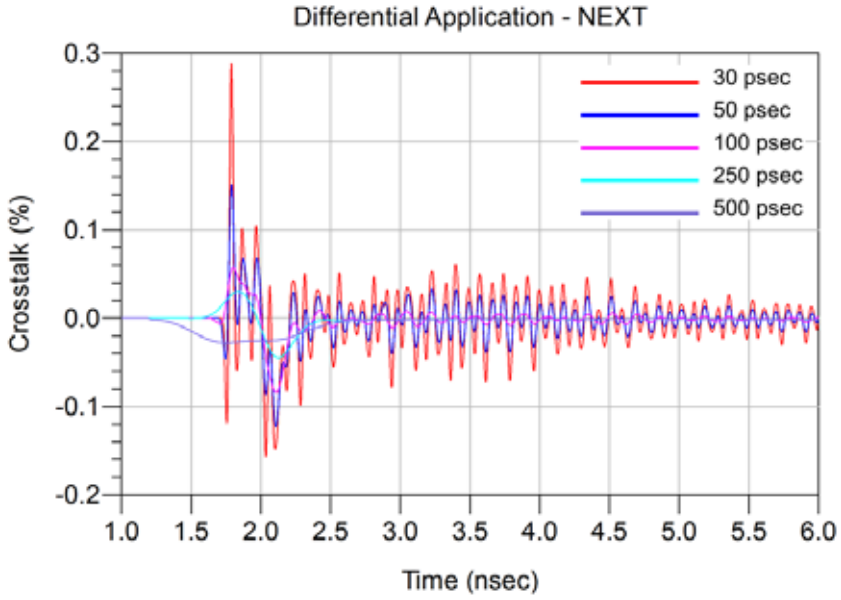


Differential High Density Vertical Application – Propagation Delay

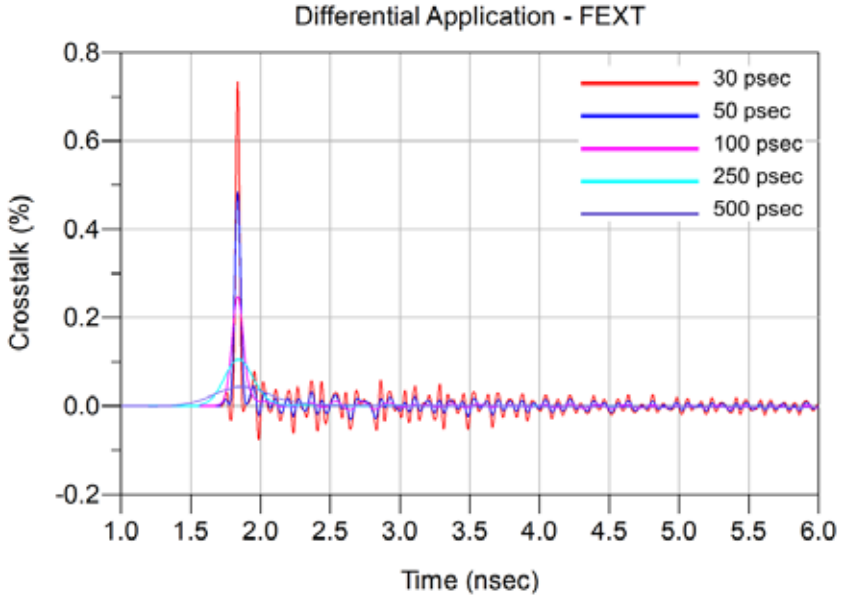


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Horizontal Application – NEXT, SEAM147, 157_SEAM107, 117

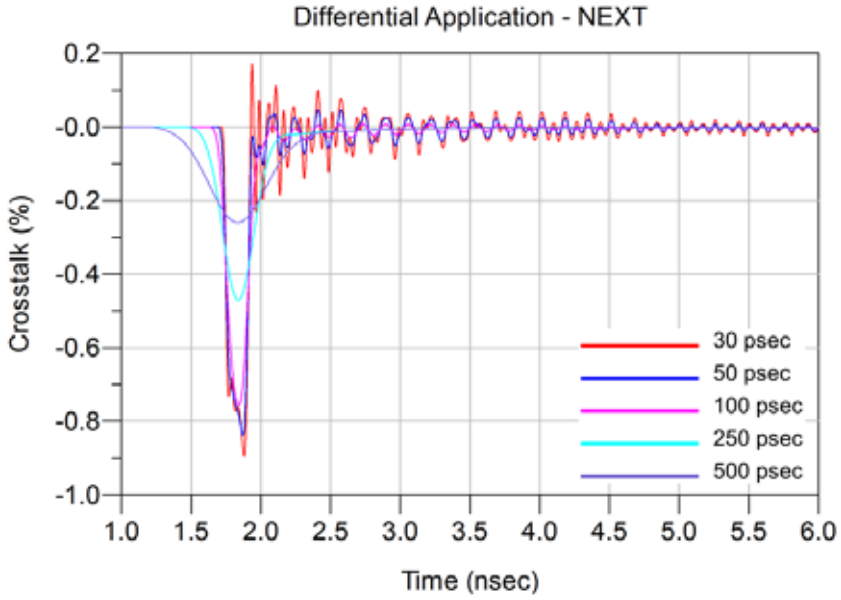


Diff Optimal Horizontal Application – FEXT, SEAM147, 157_SEAF107, 117

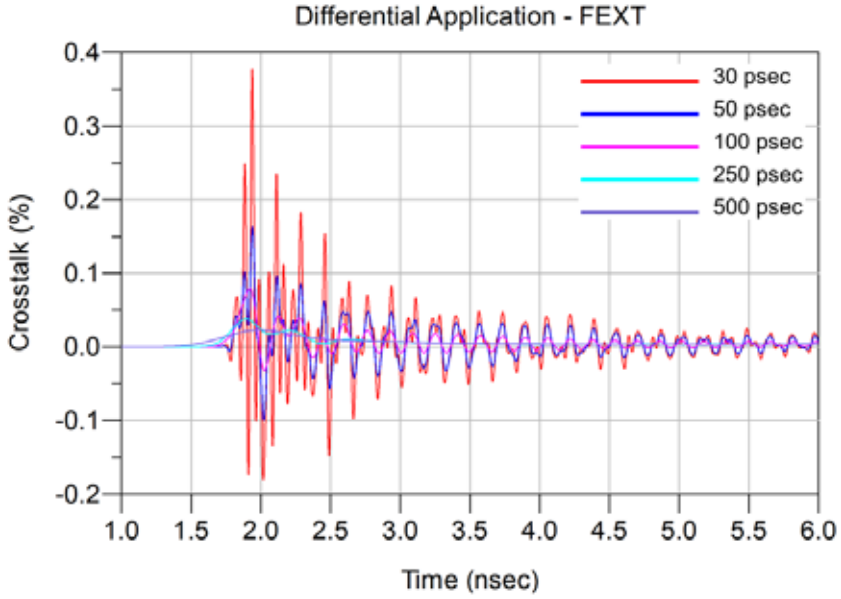


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Horizontal Application – NEXT, SEAM147, 157_SEAM126, 136

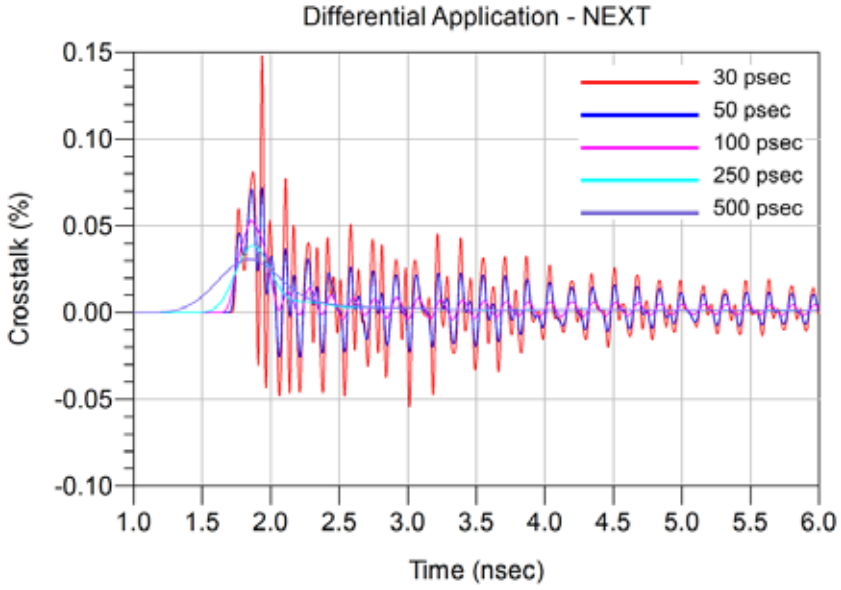


Diff Optimal Horizontal Application – FEXT, SEAM147, 157_SEAF126, 136

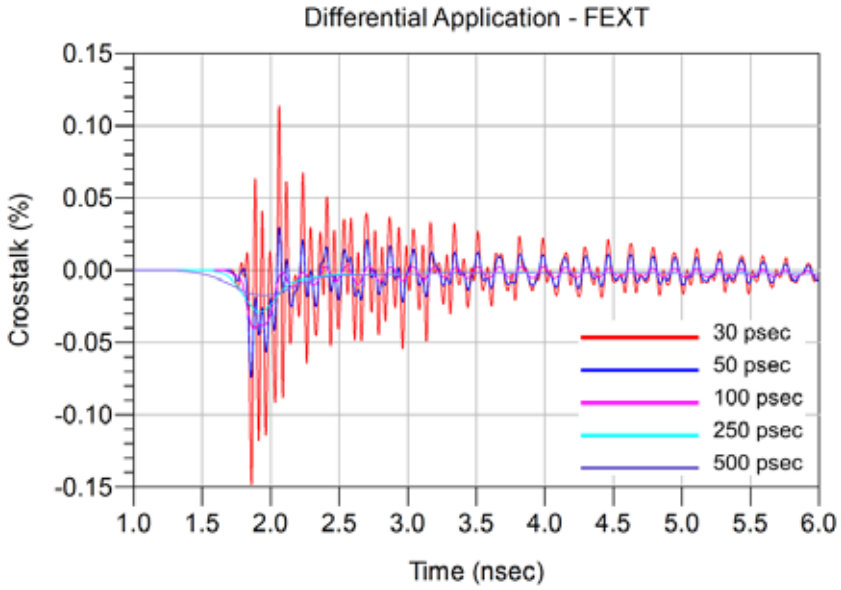


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Horizontal Application – NEXT, SEAM147, 157_SEAM145, 155

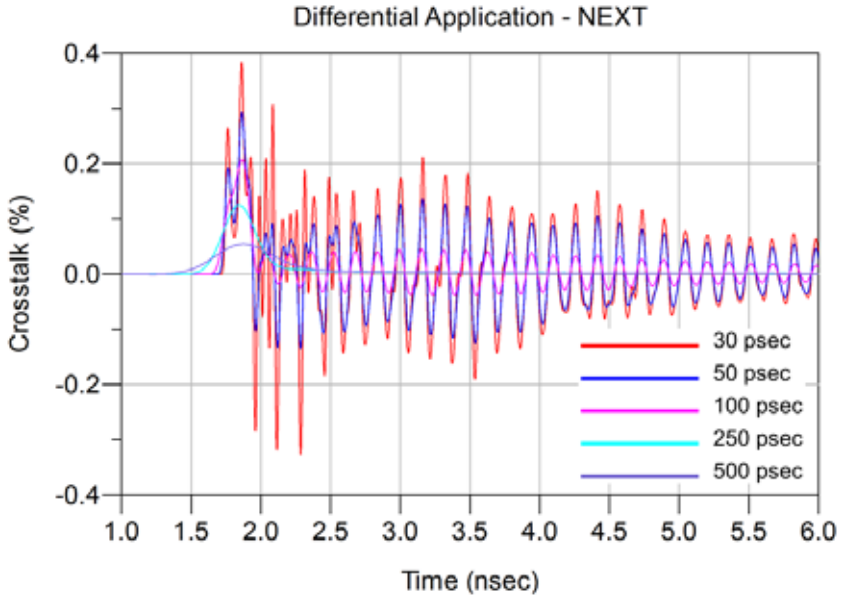


Diff Optimal Horizontal Application – FEXT, SEAM147, 157_SEAF145, 155

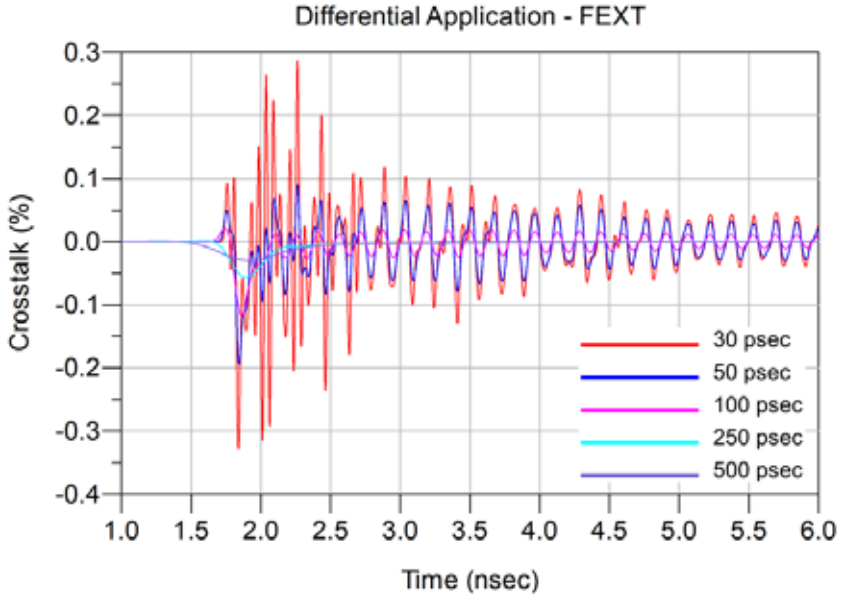


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Vertical Application – NEXT, SEAM157, 158_SEAM137, 138

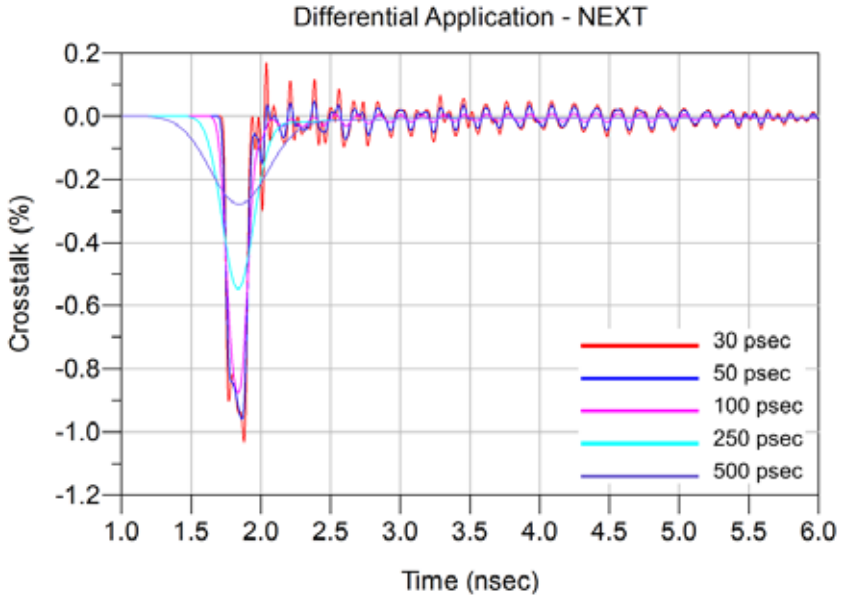


Diff Optimal Vertical Application – FEXT, SEAM157, 158_SEAF137, 138

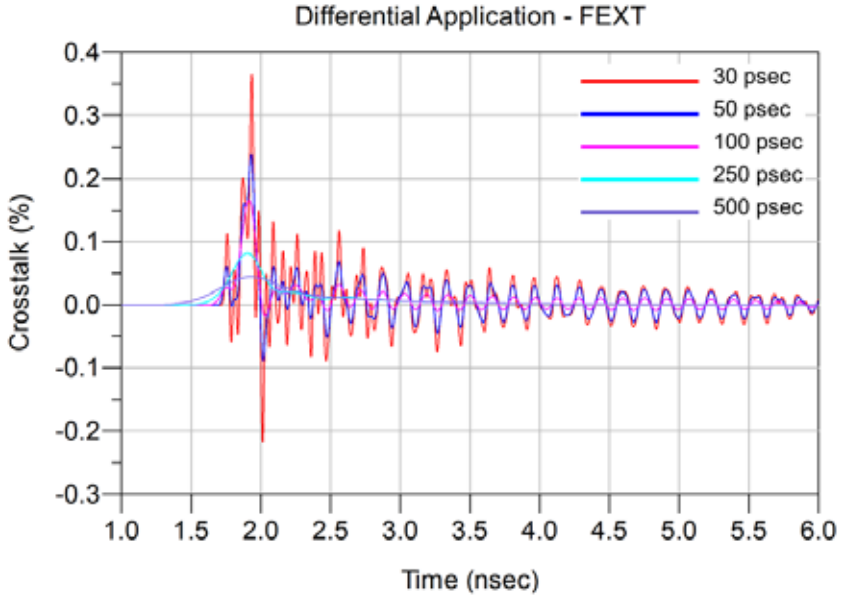


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Vertical Application – NEXT, SEAM157, 158_SEAM145, 146

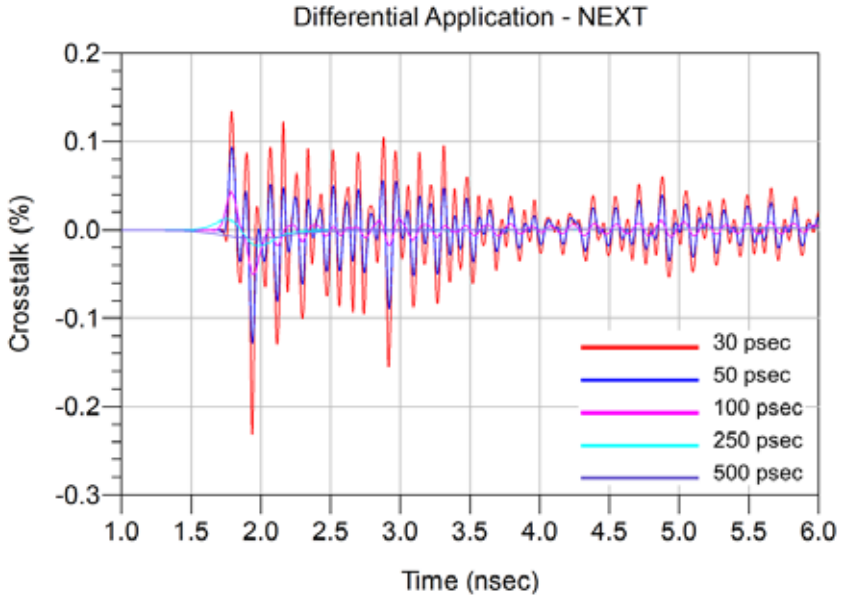


Diff Optimal Vertical Application – FEXT, SEAM157, 158_SEAF145, 146

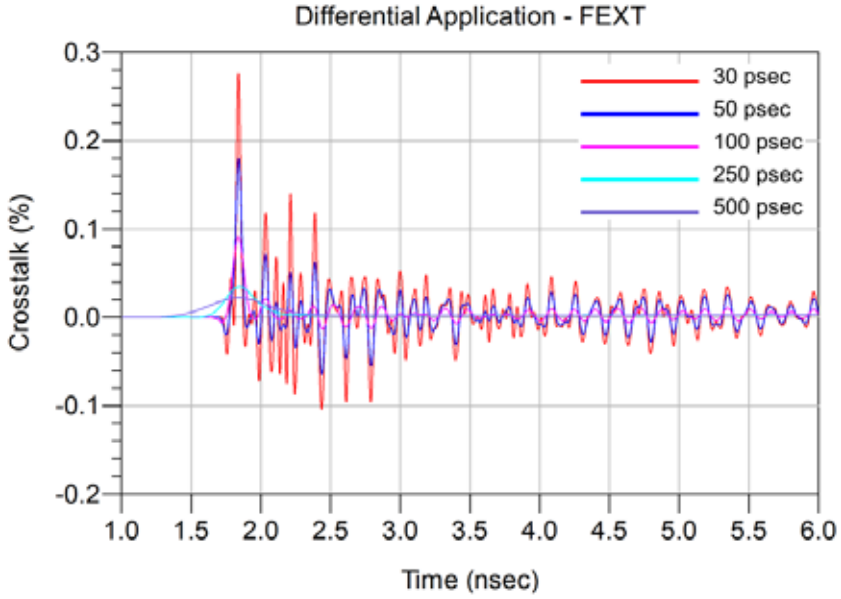


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff Optimal Vertical Application – NEXT, SEAM157, 158_SEAM153, 154

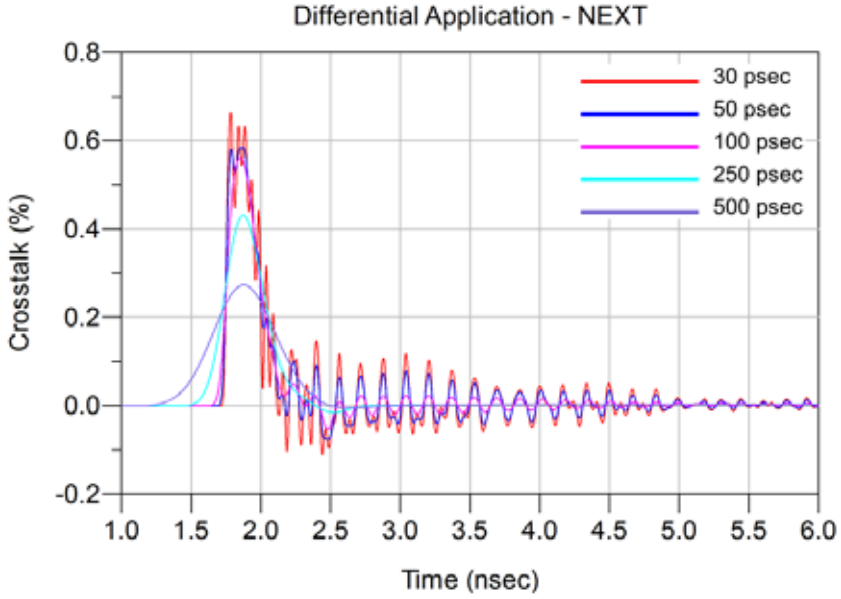


Diff Optimal Vertical Application – FEXT, SEAM157, 158_SEAF153, 154

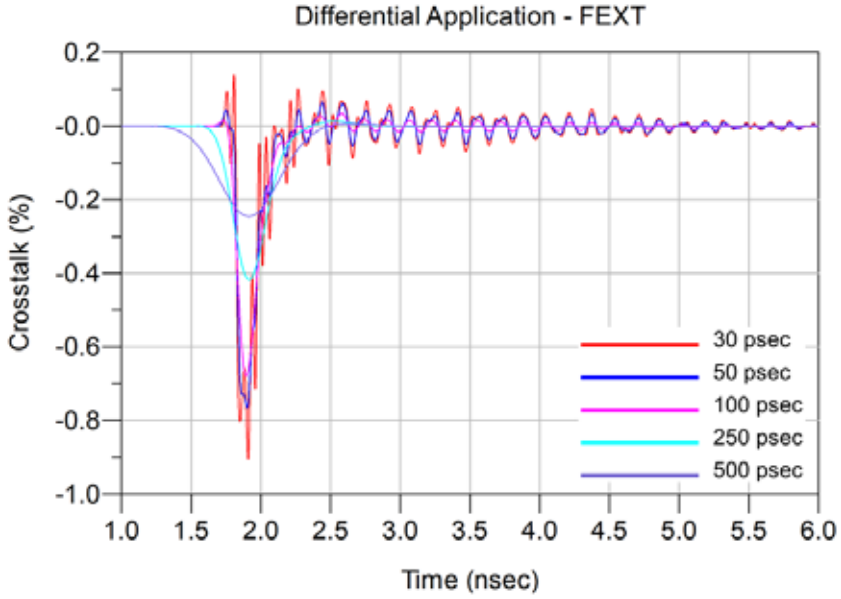


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff High Density Vertical Application – NEXT, SEAM156, 157_SEAM136, 137

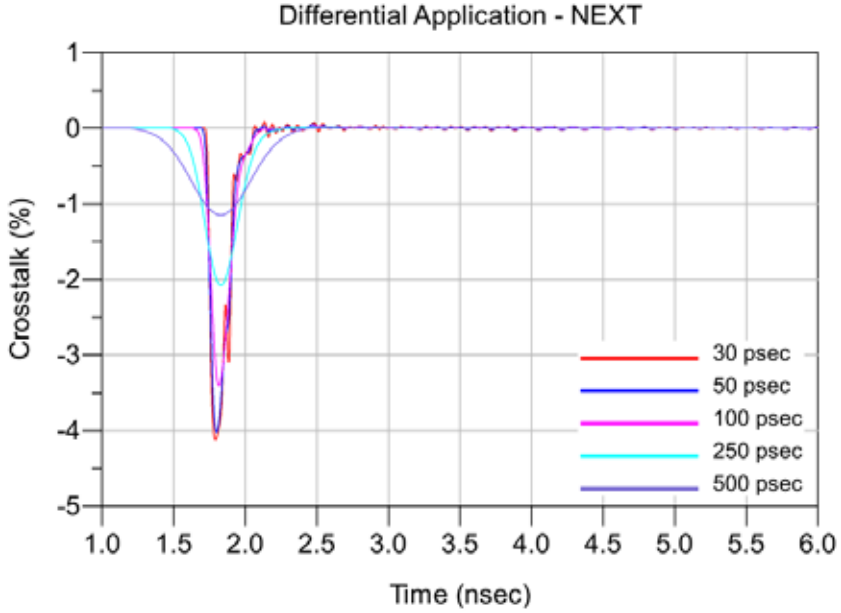


Diff High Density Vertical Application – FEXT, SEAM156, 157_SEAF136, 137

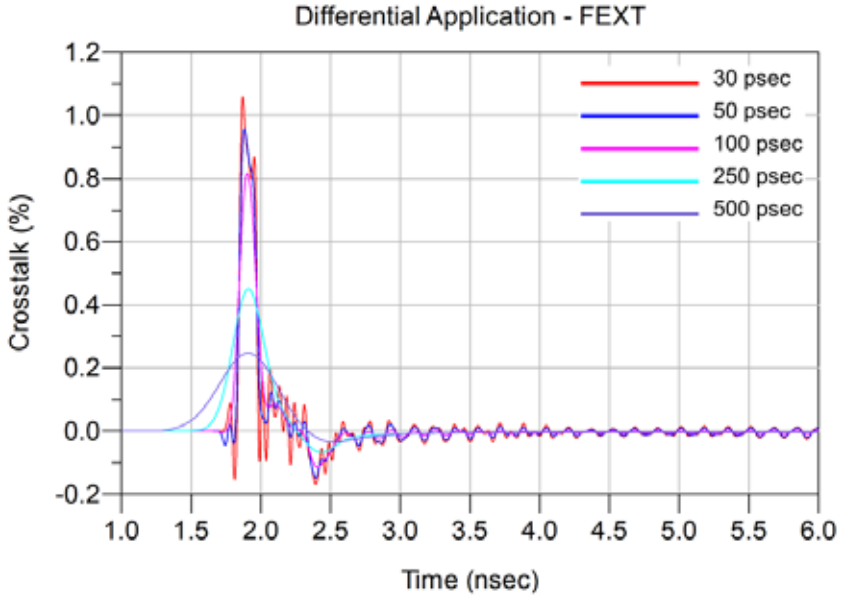


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff High Density Vertical Application – NEXT, SEAM156, 157_SEAM145, 146

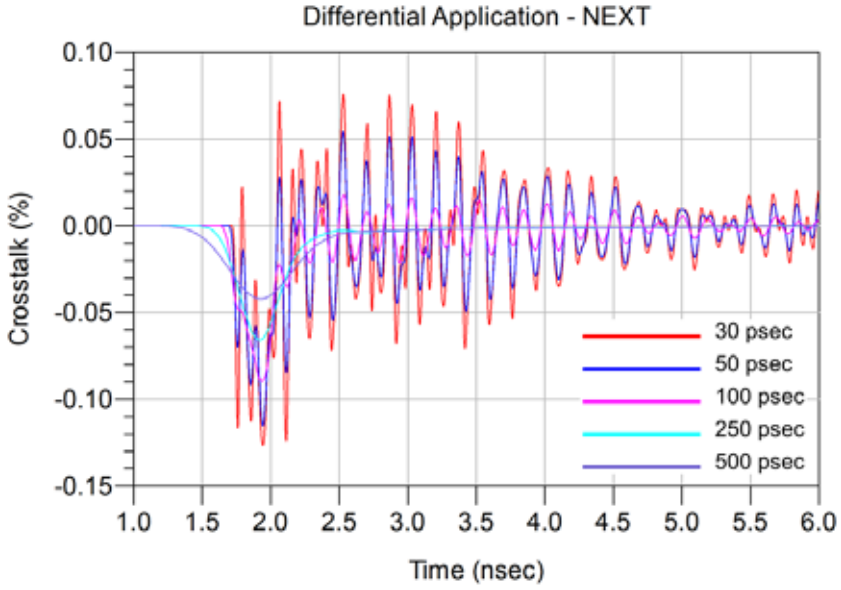


Diff High Density Vertical Application – FEXT, SEAM156, 157_SEAF145, 146

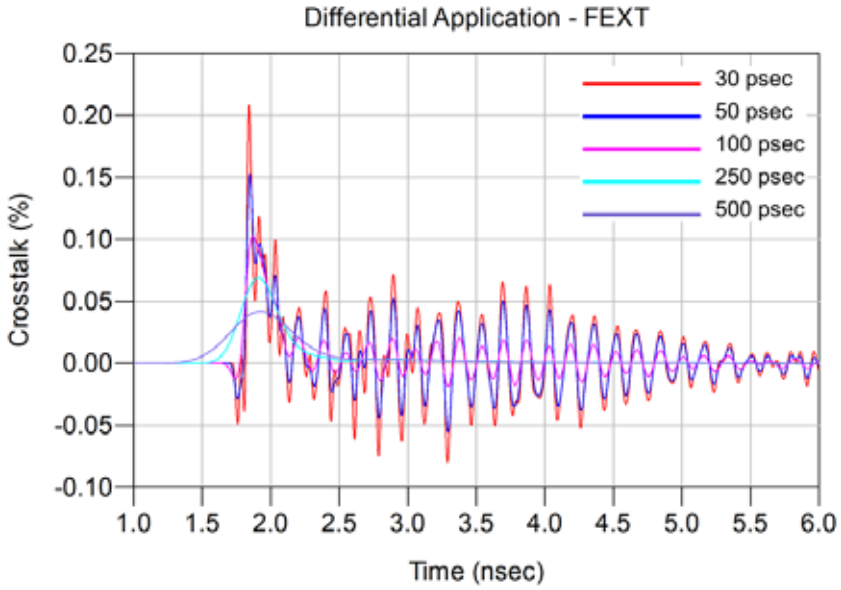


Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Diff High Density Vertical Application – NEXT, SEAM156, 157_SEAM153, 154



Diff High Density Vertical Application – FEXT, SEAM156, 157_SEAF153, 154



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Appendix C – Product and Test System Descriptions

Product Description

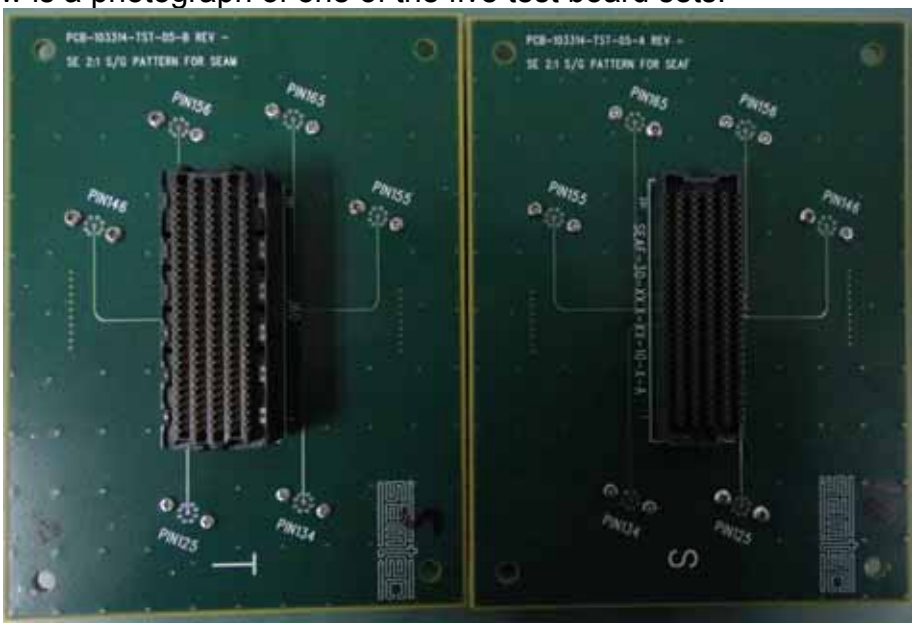
Product test samples are 17.5 mm (0.689") stack height SEAM/SEAF Series connectors. The part numbers are SEAM-30-11.0-S-10-2-A-K-TR and SEAF-30-06.5-S-10-2-A-K-TR. The SEAM/SEAF Series is an open pin field connector designed for single-ended signals with various options for differential signaling configurations. The open pin field array is 10 row providing 30 signal pins per row. A photo of the test articles mounted to SI test boards is shown below.

Test System Description

The test fixtures are composed of four-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec high speed connector products. A PCB mount SMA connector is used to interface the VNA test cables to the test fixtures. Optimization of the SMA launch was performed using full wave simulation tools to minimize reflections. Ten test fixtures are specific to the SEAM/SEAF Series connector set and identified by part numbers PCB-103314-TST-01-A and B to PCB-103314-TST-05 A and B. Calibration standards specific to the SEAM/SEAF Series are located on the calibration boards PCB-103314-TST-06 and PCB-103314-TST-07. To keep trace lengths short, five different test board sets were required to access the necessary signal pins.

PCB-103314-TST-XX Test Fixtures

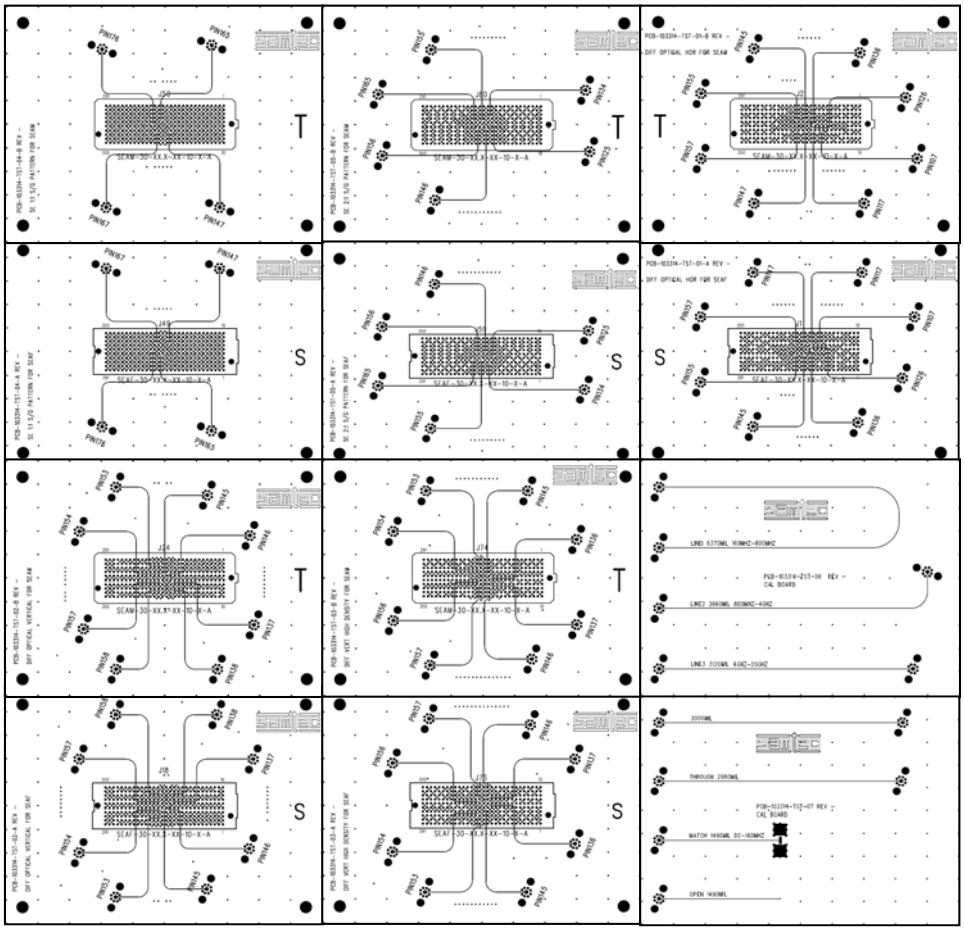
Shown below is a photograph of one of the five test board sets.



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

PCB-103314-TST-XX PCB Layout Panel

Artwork of the PCB design is shown below.



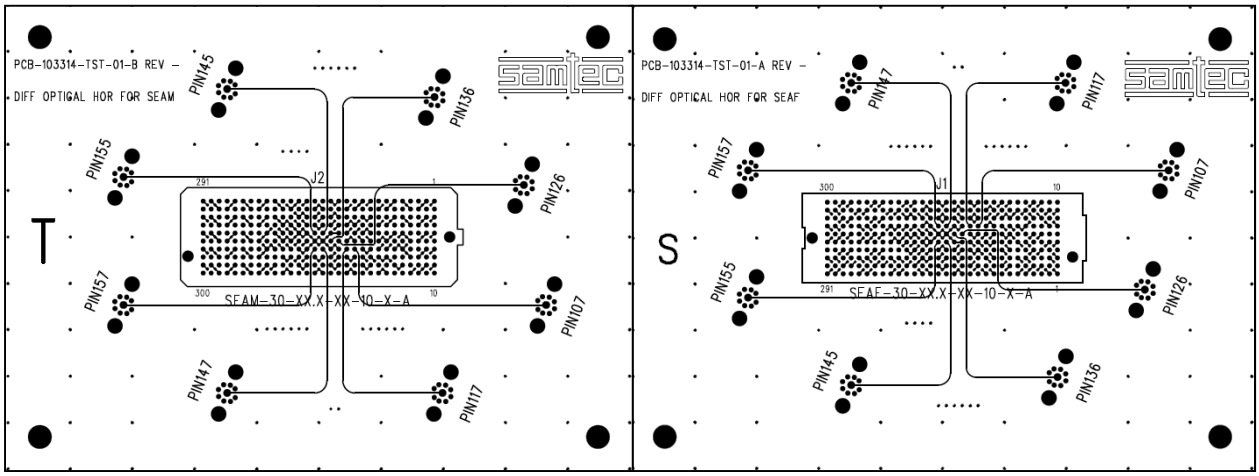
Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

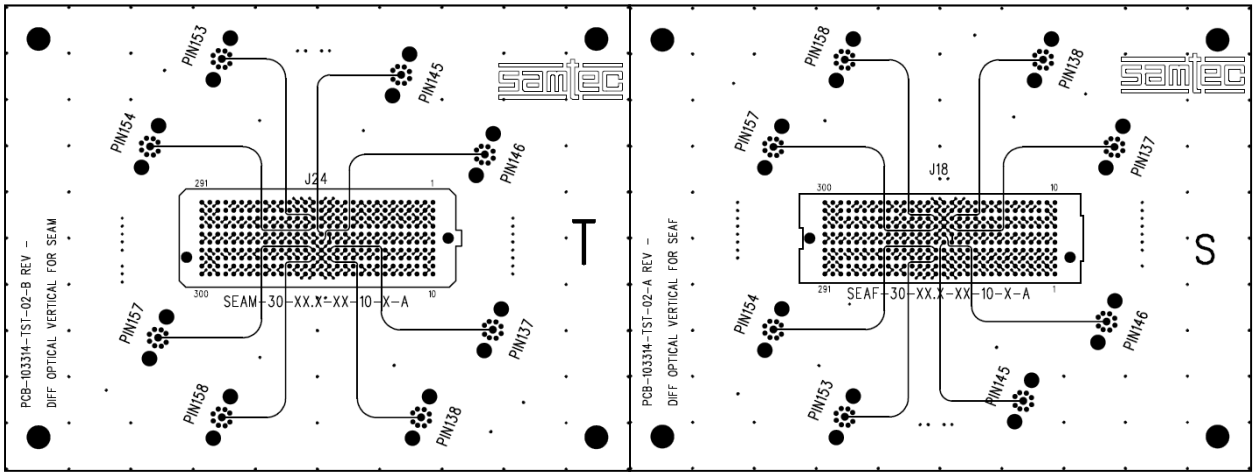
PCB Fixtures

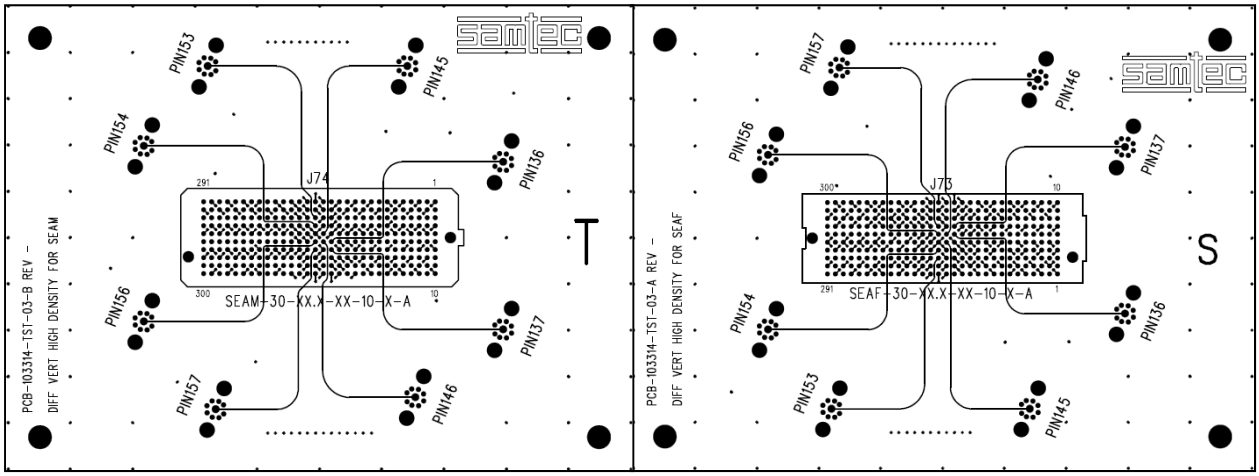
The test fixtures used are as follows:

PCB-103314 -TST-01-A Rev – SEAF Series Test Board for Differential Optimal Horizontal
PCB-103314 -TST-01-B Rev – SEAM Series Test Board for Differential Optimal Horizontal
PCB-103314 -TST-02-A Rev – SEAF Series Test Board for Differential Optimal Vertical
PCB-103314 -TST-02-B Rev – SEAM Series Test Board for Differential Optimal Vertical
PCB-103314 -TST-03-A Rev – SEAF Series Test Board for Differential High Density Vertical
PCB-103314 -TST-03-B Rev – SEAM Series Test Board for Differential High Density Vertical
PCB-103314 -TST-04-A Rev – SEAF Series Test Board for SE 1:1 S/G Pattern
PCB-103314 -TST-04-B Rev – SEAM Series Test Board for SE 1:1 S/G Pattern
PCB-103314 -TST-05-A Rev – SEAF Series Test Board for SE 2:1 S/G Pattern
PCB-103314 -TST-05-B Rev – SEAM Series Test Board for SE 2:1 S/G Pattern

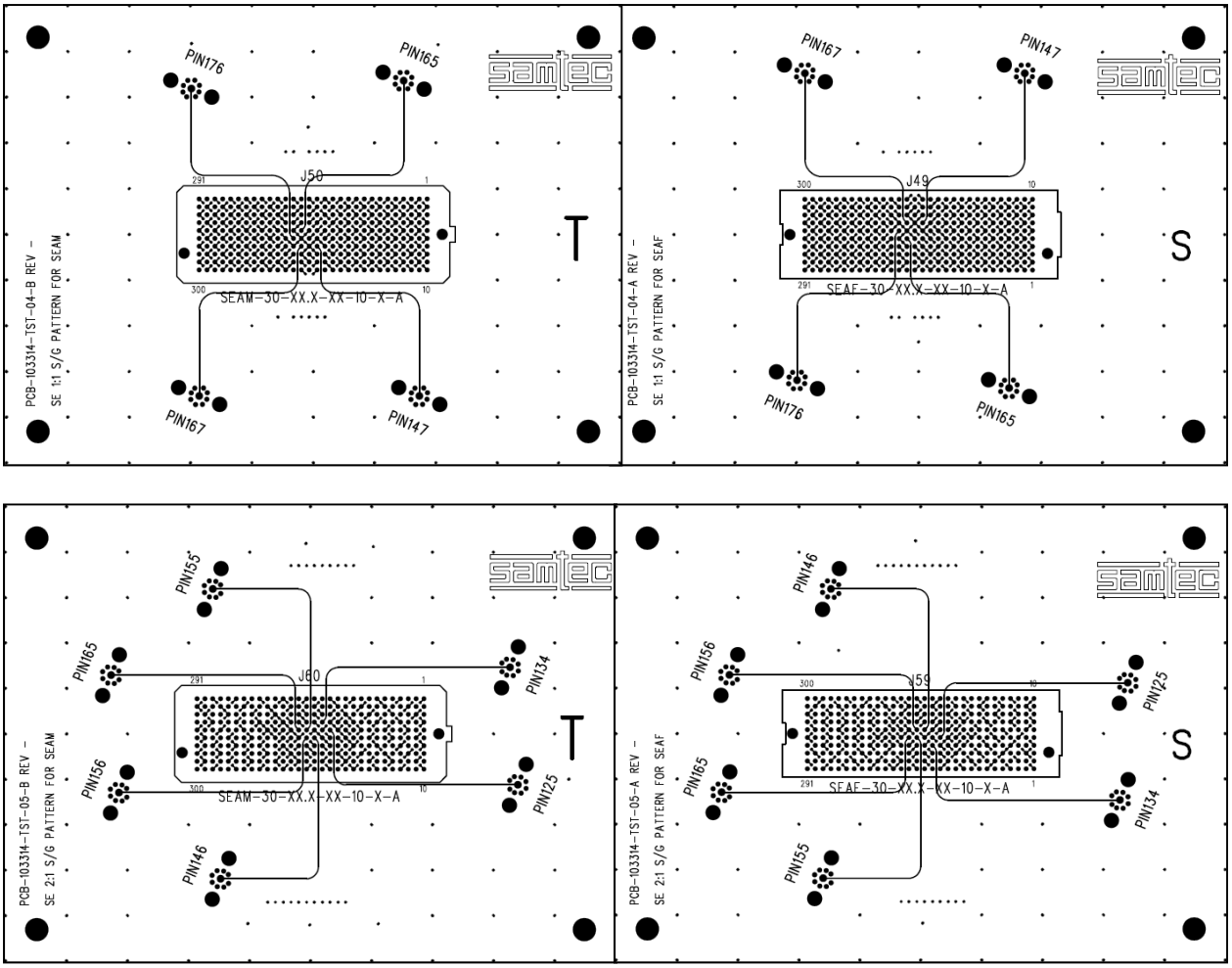
Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height







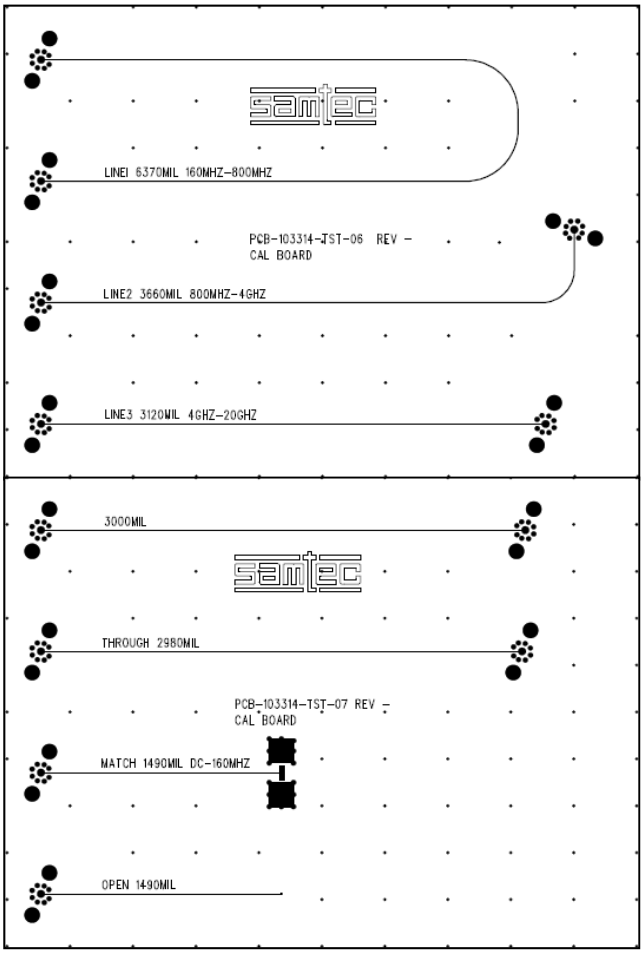
Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Calibration Board

Test fixture losses and test point reflections were removed from the data by use of TRL calibration. The calibration board is shown below. Prior to making any measurements, the calibration board is characterized to obtain parameters required to define the calibration kit. Once a cal kit is defined, calibration using the standards on the calibration board can be performed. Finally, the device can be measured and the test board effects are automatically removed.



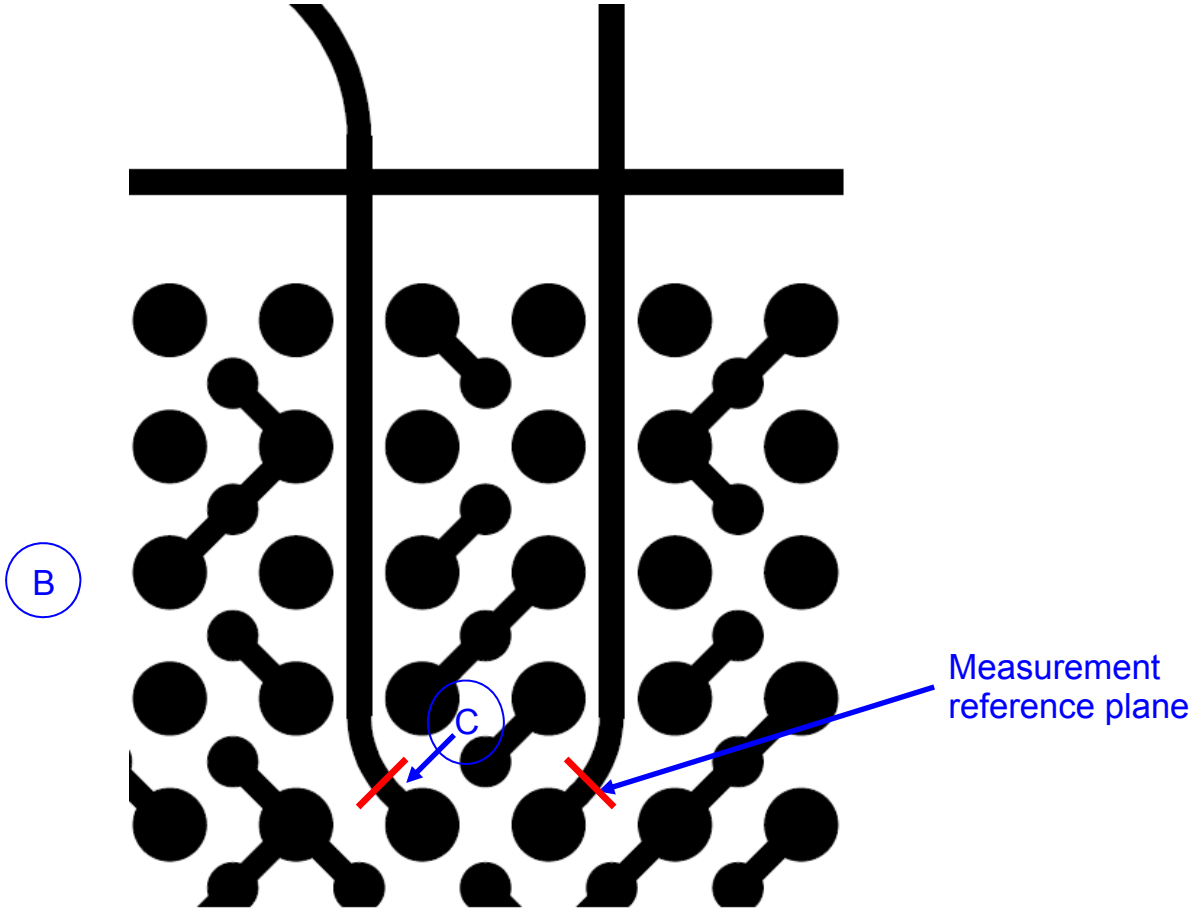
Thru line – 2980 mils
Open Reflect – 1490 mils
Line 1 – 6370 mils
Line 2 – 3660 mils
Line 3 – 3120 mils
Match – 1490 mils

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

All traces on the test boards are length matched to 1.5" measured from the edge of the pad to the SMA. The TRL calibration effectively removes 1.490" of test board trace effects. This means that 10 mils of test board trace length effects are included in the measurement. The S-Parameter measurement includes:

A- The SEAM/SEAF Series connector set
B- Test board vias and pads (footprint effects)
C- 10 mils of 9.5 mil wide microstrip trace

The figure below shows the location of the measurement reference plane.



Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

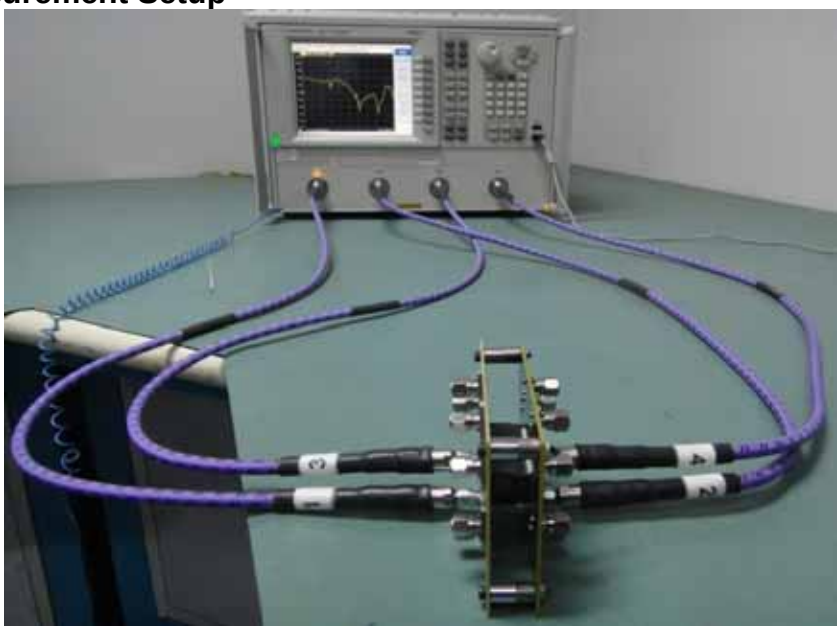
Appendix D – Test and Measurement Setup

For frequency domain measurements, the test instrument is the Agilent N5230C PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz
Stop Frequency – 20 GHz
Number of points -1601
IFBW – 1 KHz

With these settings, the measurement time is approximately 20 seconds.

N5230C Measurement Setup



Test Instruments

QTY	Description
1	Agilent N5230C PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	Gore OWD01D02039-4 (DC-50 GHz)

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

For impedance measurements, the test instrument is the Tektronix DSA8200 Digital Serial Analyzer mainframe and 80E04 sampling module. The impedance data and profiles are obtained directly from the instrument. The Digital Analyzer is configured as follows:

	Single-Ended Signal	Differential Signal
Vertical Scale:	5 ohm / Div:	10 ohm / Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	200ps/ Div	200ps/ Div
Record Length:	4000	4000
Averages:	≥ 16	≥ 16

DSA8200 Measurement Setup

Test Instruments

QTY	Description
1	Tektronix DSA8200 Digital Serial Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module

Test Cables & Adapters

QTY	Description
2	Samtec RF405-01SP1-01SP1-0305 (DC-20 GHz)

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards, and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4433A ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect and 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the SEAM/SEAF Series test boards, this is greater than 20 GHz.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Agilent N5230C. This calibration is saved and can be recalled at any time. Calibration takes roughly 30 minutes to perform.

Time Domain Procedures

Mathematically, Frequency Domain data can be transformed to obtain a Time Domain response. Perfect transformation requires Frequency Domain data from DC to infinity Hz. Fortunately, a very accurate Time Domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The Time Domain responses were generated using Agilent ADS 2009 update 1. This tool has a transient convolution simulator, which can generate a Time Domain response directly from measured S-Parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation.
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Propagation Delay (TDT)
The Propagation Delay is a measure of the Time Domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss, and the Time Domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)
A step pulse is applied to the touchstone model of the connector and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.

Impedance (TDR)

Measurements involving digital pulses are performed using either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. The TDR method is used for the impedance measurements in this report.

The signal line(s) of the SUT's is energized with a TDR pulse and the far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. The "best case" signal mapping was tested and is presented in this report.

Series: SEAM/SEAF Array Series
Description: 1.27mm x 1.27mm grid interconnect system, 17.5mm Stack Height

Appendix F – Glossary of Terms

ADS – Advanced Design Systems
BC – Best Case crosstalk configuration
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
FD – Frequency domain
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
HDV – High Density Vertical
NEXT – Near-End Crosstalk
OV – Optimal Vertical
OH – Optimal Horizontal
PCB – Printed Circuit Board
PPO – Pin Population Option
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
S – Static (independent of PCB ground)
SOLT – acronym used to define Short, Open, Load & Thru Calibration Standards
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
Z – Impedance (expressed in ohms)