Concept Design

GT Readout Platform

Pietro King, Hampus Sandberg and Dionisio Doering

15th November 2023

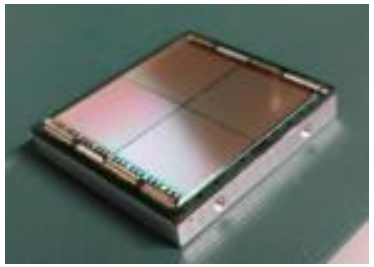
SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Project Goal

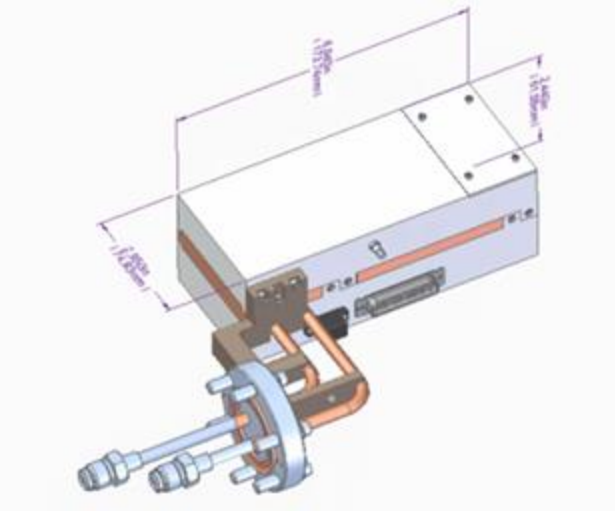
- The aim of *GT Readout Platform* is the development of a high-rate camera for scattering/imaging experiments at LCLS-II-HE

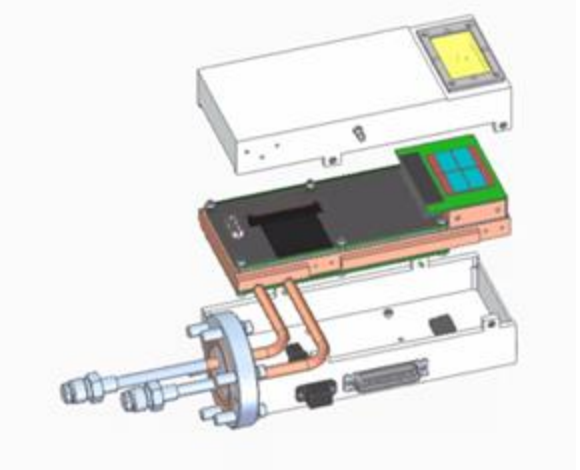
- The target detectors are:
  - 2x2 tile of **ePixUHR** ASICs
  - 2x2 tile of **SparkPix-S** ASICs
  - 2x2 tile of SparkPix-ED ASICs
  - Possibly other variants



Platform specification

	Small Camera **ePixUHR – 140k 2x2 ASIC**	Small Camera **SparkPix S – 500k 2x2 ASIC**
Pixel Pitch (um)	100	50
Pixels	129,024 px (168*192*4 ASICs)	540,672 px (352*384*4 ASICs)
Frame Rate	35kHz / 100kHz	1MHz
Focal Plane Area	4cm x 4cm	4cm x 4cm
Front side footprint (window)	5cm x 5cm	5cm x 5cm
Number of GT IOs required	48	48
Expected GT IOs speed (per framerate)	1.75 Gbps/ 5.25 Gbps	5.25 Gbps
Maximum Power Dissipation	90W	110W
Weight	1.5kg	1.5kg
Data volume (per framerate)	56 Gbps/ 160 Gbps	160 Gbps





Design conforming with *LCLS-II-HE Detectors Interface Control Document* (#LCLSII-HE-1.4-IC-0688-R0)

Detector Overview

	2x2 ePixUHR/SparkPix-S	
Parameter	Small Camera **ePixUHR – 140k 2x2 ASIC**	Small Camera **SparkPix S – 500k 2x2 ASIC**
Pixels	129,024 px (168 *192*4)	540,672 px (352*384*4)
Rate	35kHz / 100kHz	1MHz
Focal Plane Area	4cm x 4cm	4cm x 4cm
Front side footprint (window)	5cm x 5cm	5cm x 5cm
Weight	1.5kg	1.5kg
Data volume	56 Gbps/ 160 Gbps	160 Gbps

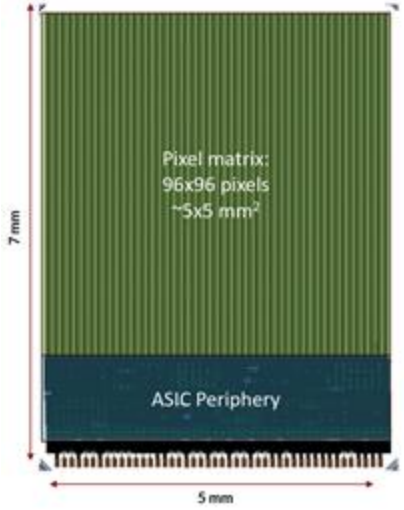
ePixUHR

- Full frame readout
- 100 um pixel pitch
- Full Scale: 168 x 192 px
- Framerate: 35kHz prototype followed by a 100kHz version

ePixUHR-35kHz Prototype Charge Injection pattern

SparkPix-S

- Sparse Readout Strategy
- 50 um pixel pitch
- Full Scale: 352 x 384 px
- 1% Occupancy @ 1MHz framerate



SparkPix-S Prototype (96x96 Pixels)

ASIC Power Requirements

ASIC Power	Analog Section		Digital Section		I/O Section		0.6V Sink		Analog TPS	
Requirement	ePixUHR 140k 2x2 Detector	SparkPix-S 500k 2x2 Detector	ePixUHR 140k 2x2 Detector	SparkPix-S 500k 2x2 Detector	ePixUHR 140k 2x2 Detector	SparkPix-S 500k 2x2 Detector	ePixUHR 140k 2x2 Detector	SparkPix-S 500k 2x2 Detector	ePixUHR 140k 2x2 Detector	SparkPix-S 500k 2x2 Detector
Voltage	**1.3 V**	**1.3V**	**1.3V**	**1.3V**	**1.3V**	**1.3V**	**N/A**	**0.6 V**	**2.5 V**	**2.5V**
Required current	10A (= 2.5 A* 4 ASIC)	**13.4 A** (= 3.35A * 4 ASIC)	1.2 A (= 0.3 A * 4 ASIC)	**2.0 A** (= 0.5 A * 4 ASIC)	**1.6 A** (= 0.4 * 4 ASIC)		N/A	**-8 A** (= -2A * 4 ASIC)	**0.4 A** (=0.1 * 4 ASIC)	
System Requirement	**+1.3 V @ +17.5 A** (Adding +30% current for PVT variation)		**+1.3 V @ +3 A** (Adding +30% current for PVT variation)		**+1.3 V @ +2.5 A** (Adding +30% current for PVT variation)		**+0.6 V @ -11 A** **!this current is not provided by the LDO. But it passes through it.** (Adding +30% current for PVT variation)		**+2.5 V @ +0.5 A** (Adding +30% current for PVT variation)	

ePixUHR : 10A* 1.3V + 1.2A * 1.3V + 1.6A * 1.3V + 0.4A * 2.5V = 17.6 W +30% = 23W
SparkPix-S: 13.4* 1.3V + 2.0A * 1.3V + 1.6 * 1.3V + 0.4A * 2.5V = 23.1W +30% = 30W

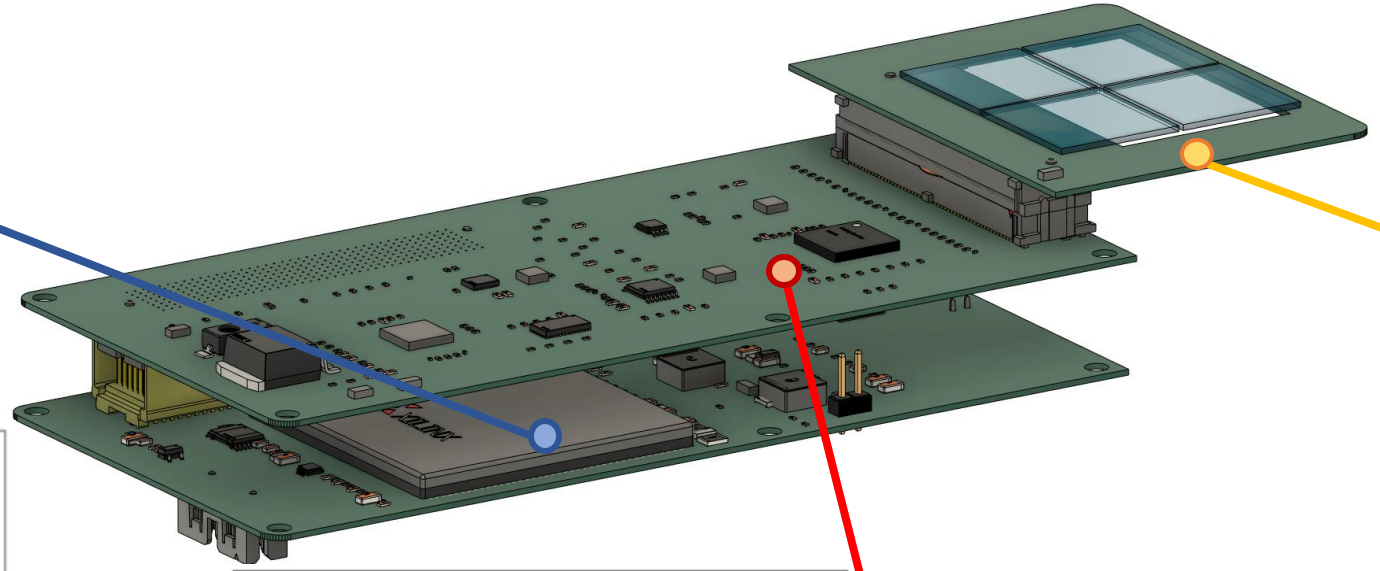
ASIC High Speed GTs requirements

ePixUHR and SparkPix-S will use 5Gb/s Fast Transceivers.
In order to read them, the readout system will need to use fast receivers as well.
The choice fell on Xilinx GTH/GTY transceivers.
Consequently, the readout FPGA will need an adequate number of transceivers for the readout of 4 ASICs

	2x2 ePixUHR/SparkPix-S	
	Small Camera **ePixUHR – 140k** **2x2 ASIC**	Small Camera **SparkPix S – 500k** **2x2 ASIC**
High Speed GTs (GTH/GTY)	- ASIC data: 32 = 8 lanes * 4 ASIC - Spare outputs : 4 - FPGA-PC communication: 12 = 12* 160 Gbps/ 275Gbps Total: **48 High Speed GTs**	- ASIC data: 32 = 8 lanes * 4 ASIC - Spare outputs : 4 - FPGA-PC communication: 12 = 12* 160 Gbps/ 275Gbps Total: **48 High Speed GTs**

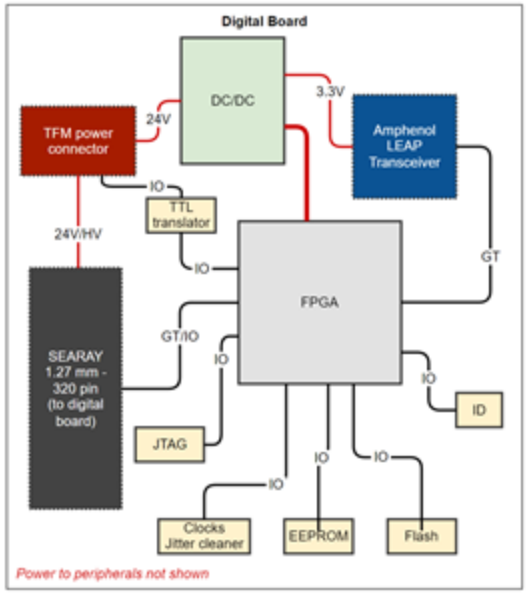
		UHR 2x2	SparkPix S 2x2
	Requirements	48 GTs	48 GTs
	Characteristics		
KU15P (-A1156) Kintex U+	28 GTs / 35^2 mm^2 / 10k$	✗	✗
KU15P (-E1517) Kintex U+	56 GTs / 40^2 mm^2 / 10k$	✓	✓
KU15P (-A1760) Kintex U+	76 GTs / 42.5^2 mm^2 / 10k$	✓	✓
XCVU160 (-C2104) Virtex U	104 GTs / 47.5^2 mm^2 / 40k$	✓	✓
XCVU190 (-A2577) Virtex U	120 GTs / 47.5^2 mm^2 / 70k$	✓	✓
VU13P (-A2577) Virtex U+	128 GTs / 52.5^2 mm^2 / 110k$	✓	✓

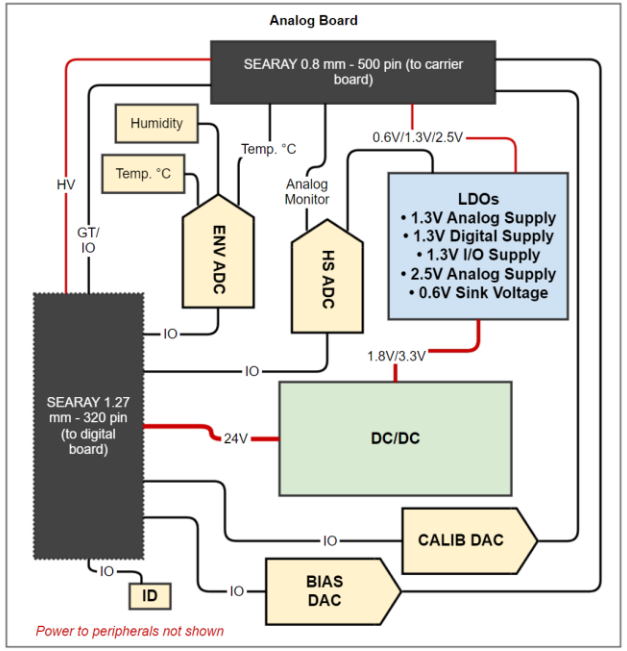
GT Readout Camera Block Diagram



Digital Board

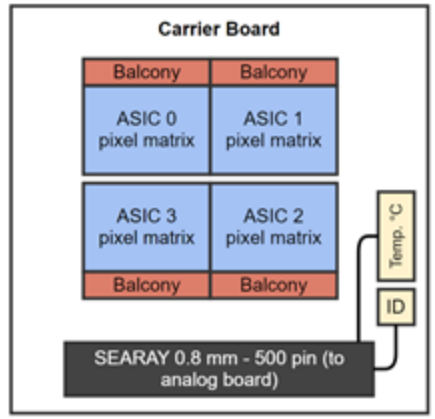
- **Kintex Ultrascale+ FPGA (KU15P-A1760)**
- 300Gbps Amphenol Leap OBT optical transceiver
- Clean fast clocks generation





Carrier Board

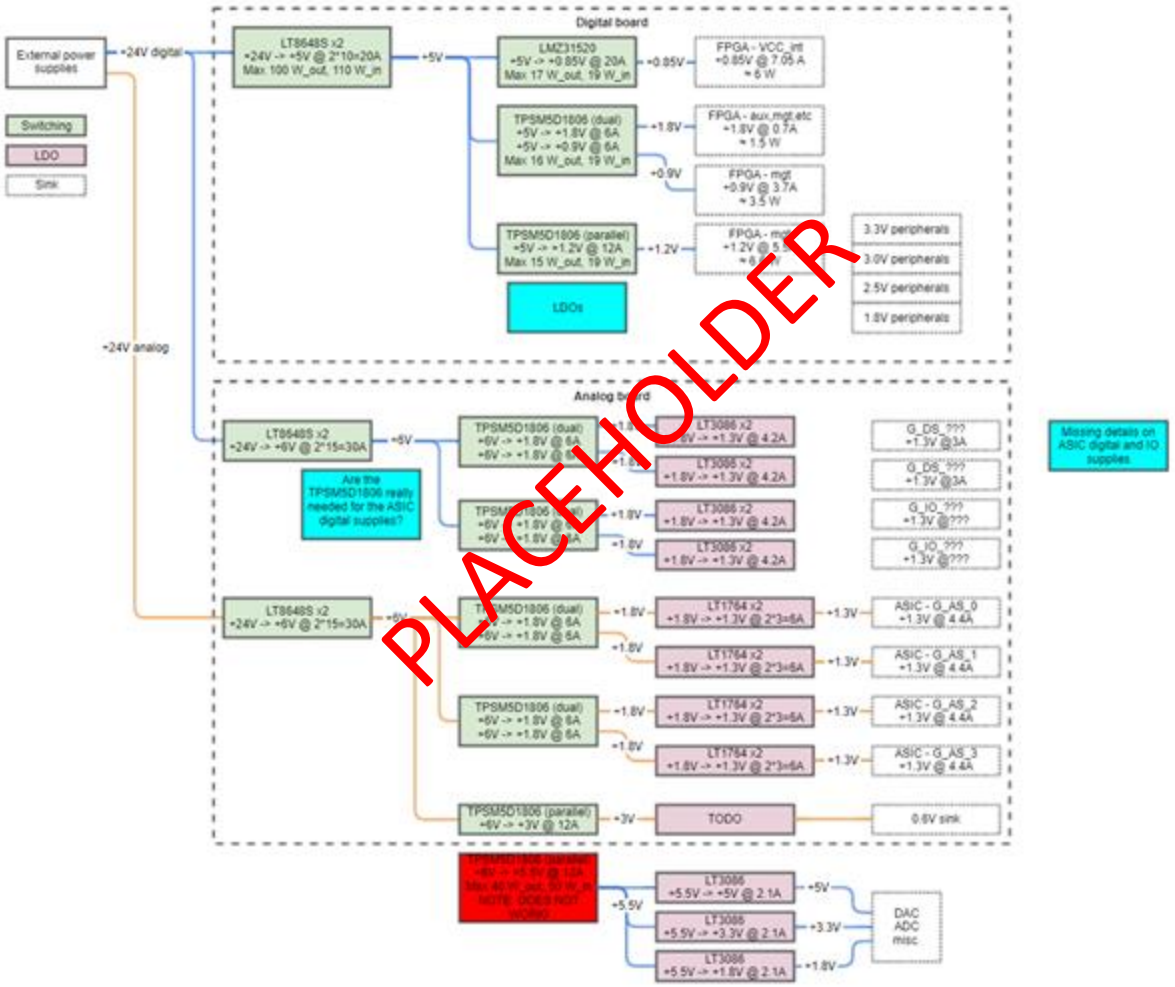
- It will host a tile of 2x2 ASIC/Sensor
- Large cutout for cooling
- 500-pin Samtec SEAM8 Connector



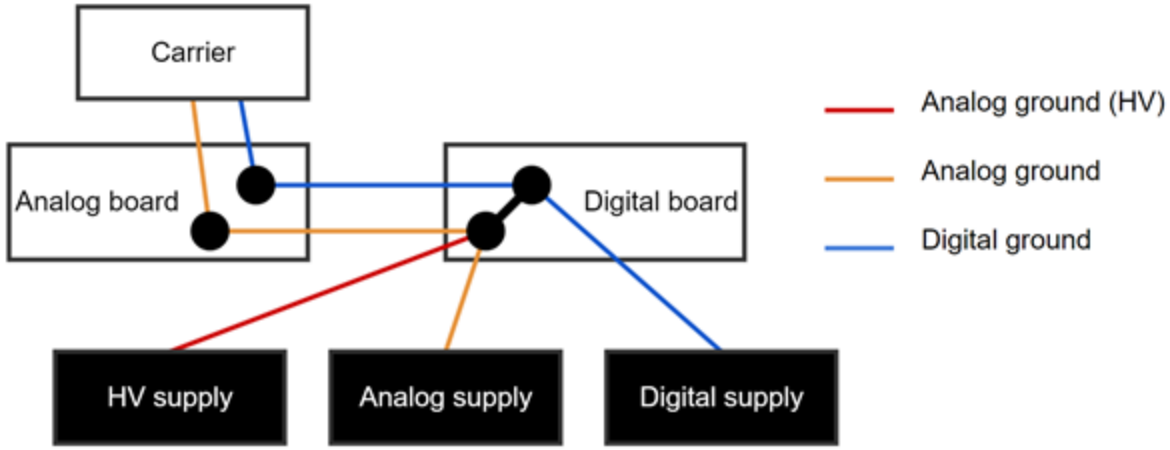
Analog Board

- Monitoring ADCs
  - High Speed for oscilloscope-like power monitoring
  - Environmental (Temperature, Humidity and general voltages)
- DACs
  - ASIC Calibration and Charge injection
  - Sensor Guard Ring

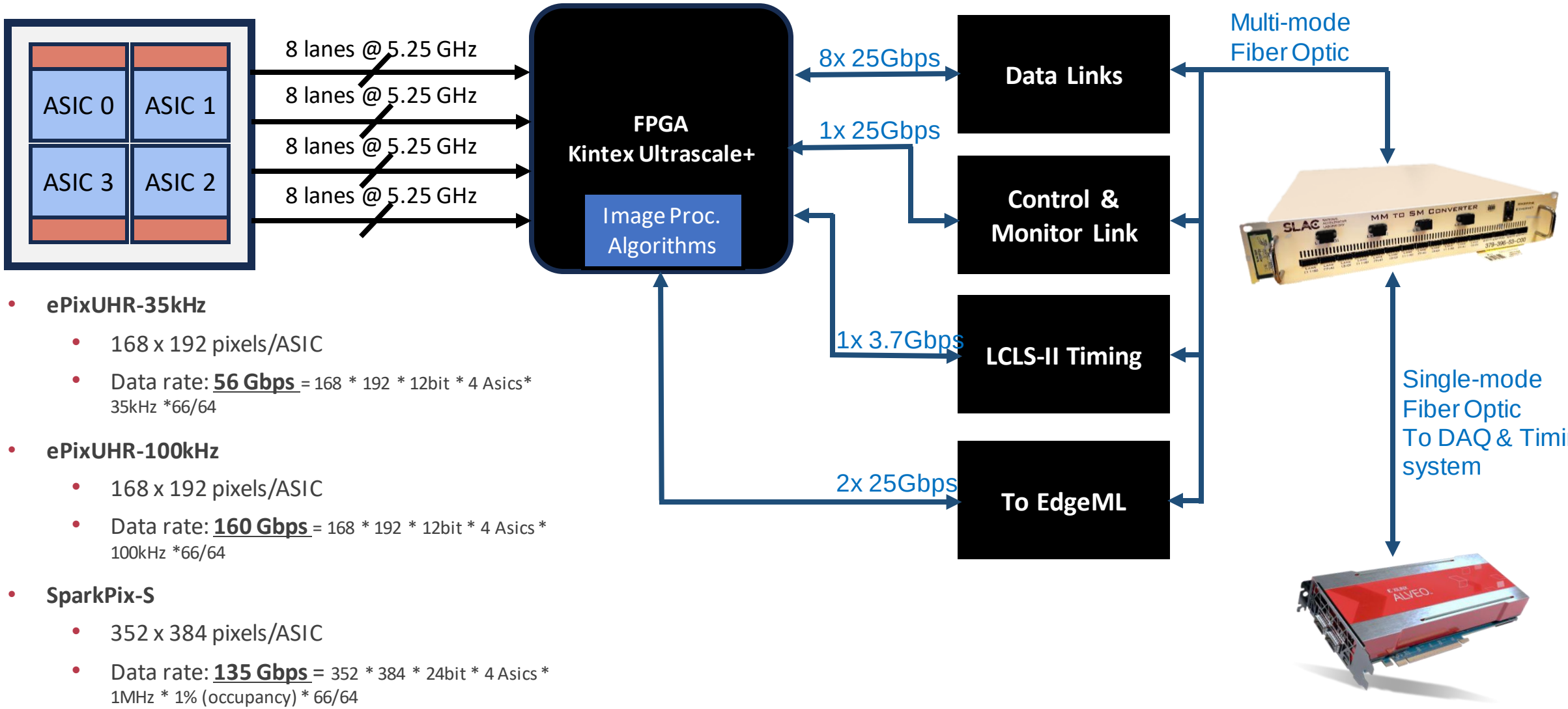
Camera Power Distribution



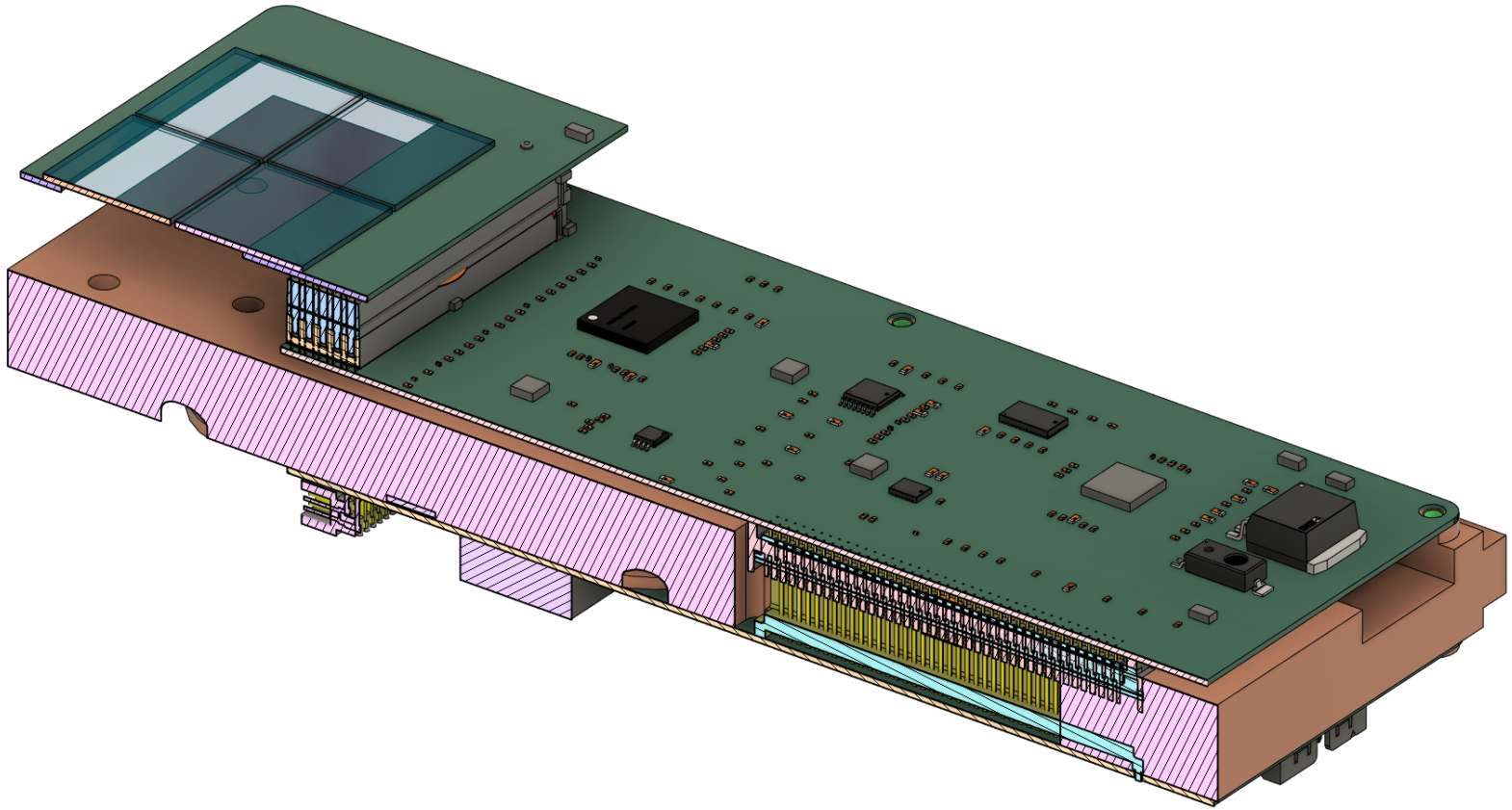
Grounding Scheme

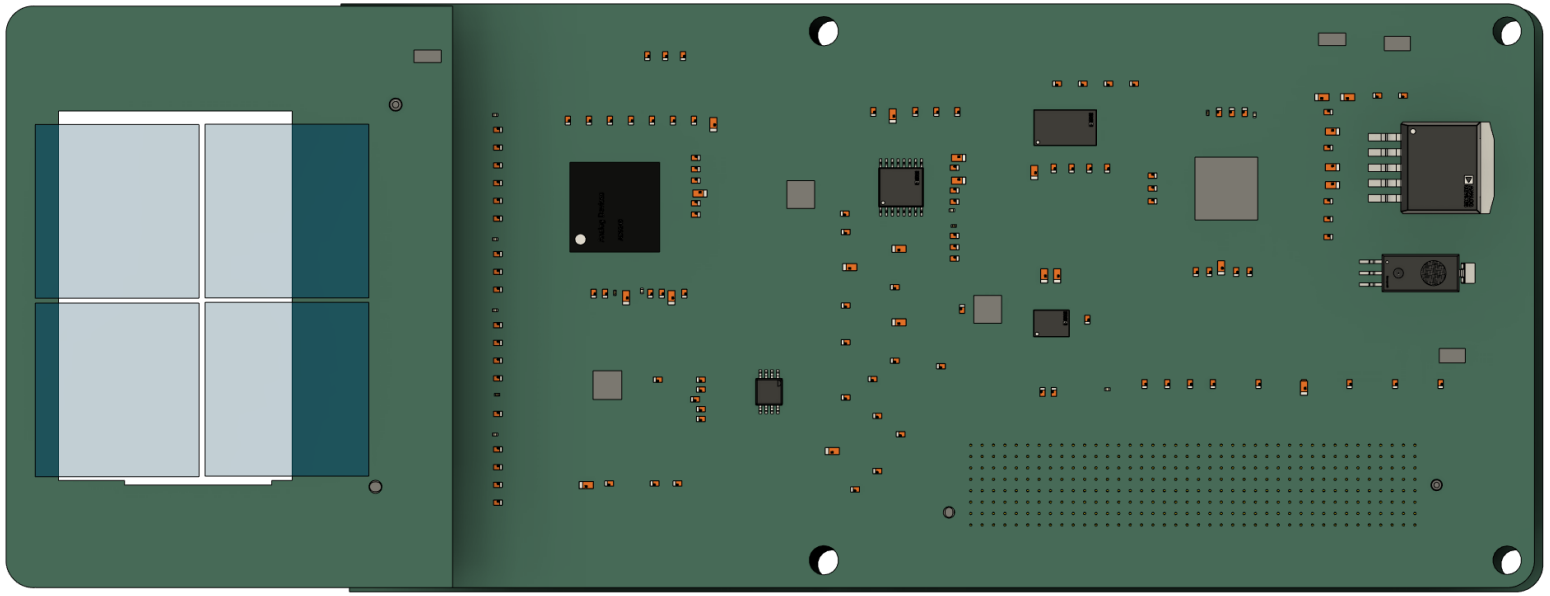


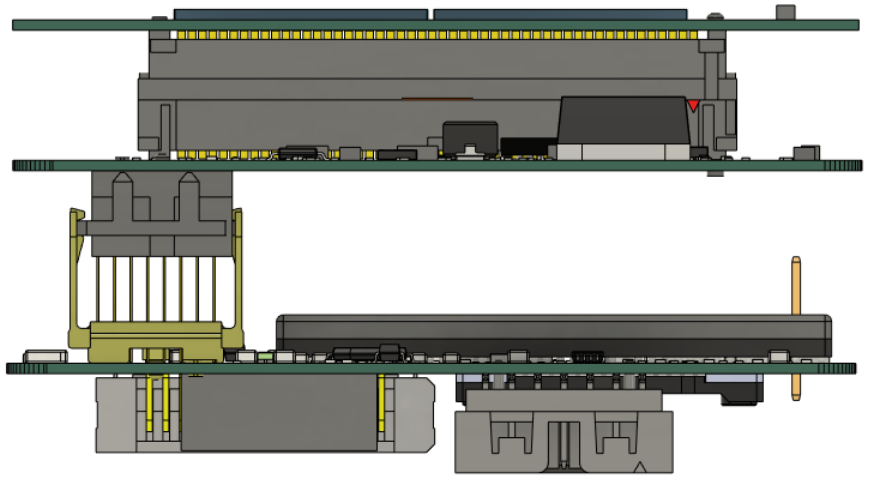
GT Readout Data flow

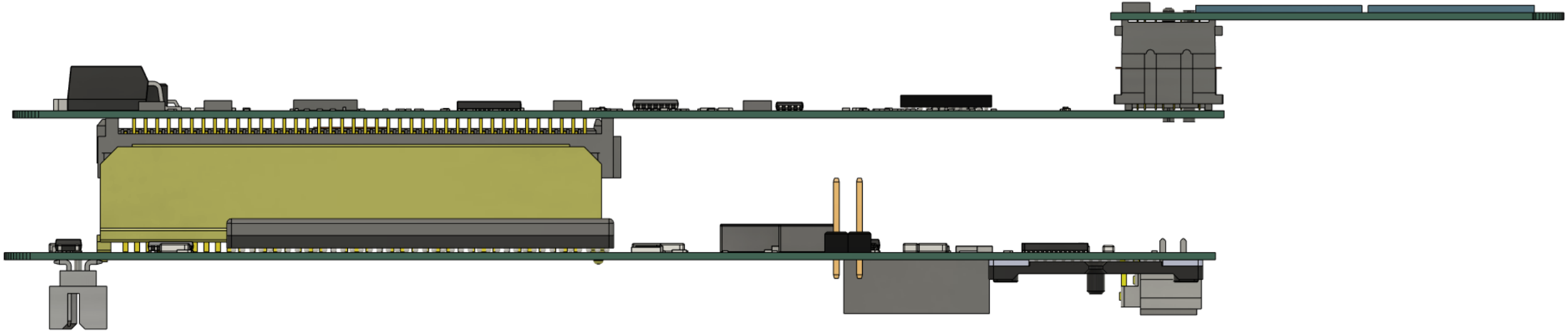


- **ePixUHR-35kHz**
  - 168 x 192 pixels/ASIC
  - Data rate: **56 Gbps** = 168 * 192 * 12bit * 4 Asics* 35kHz *66/64
- **ePixUHR-100kHz**
  - 168 x 192 pixels/ASIC
  - Data rate: **160 Gbps** = 168 * 192 * 12bit * 4 Asics * 100kHz *66/64
- **SparkPix-S**
  - 352 x 384 pixels/ASIC
  - Data rate: **135 Gbps** = 352 * 384 * 24bit * 4 Asics * 1MHz * 1% (occupancy) * 66/64

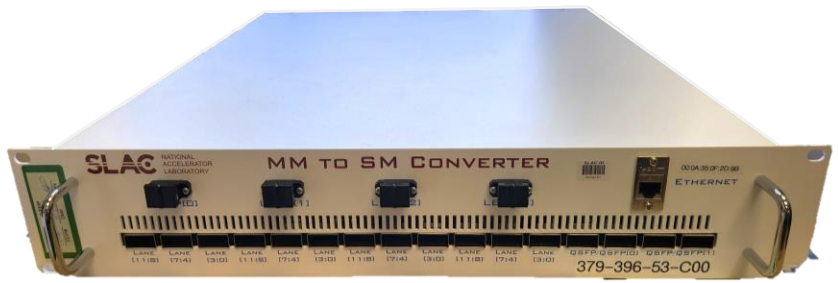









SLAC
NATIONAL ACCELERATOR LABORATORY
MM TO SM CONVERTER
ETHERNET
379-396-53-C00


SLAC
NATIONAL ACCELERATOR LABORATORY
MM TO SM CONVERTER
ETHERNET
379-396-53-C00