

# Sinking Current LDO - Update

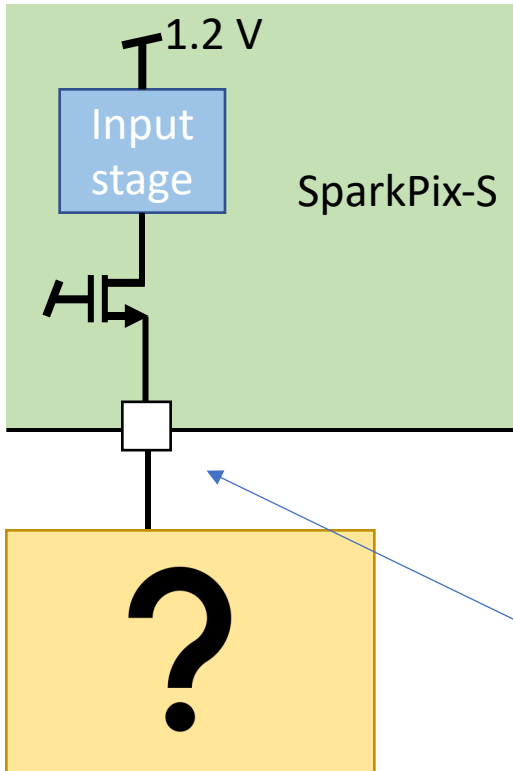
*SparkPix-S*

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30<sup>th</sup> August 2022

# Problem Specifications - Updated

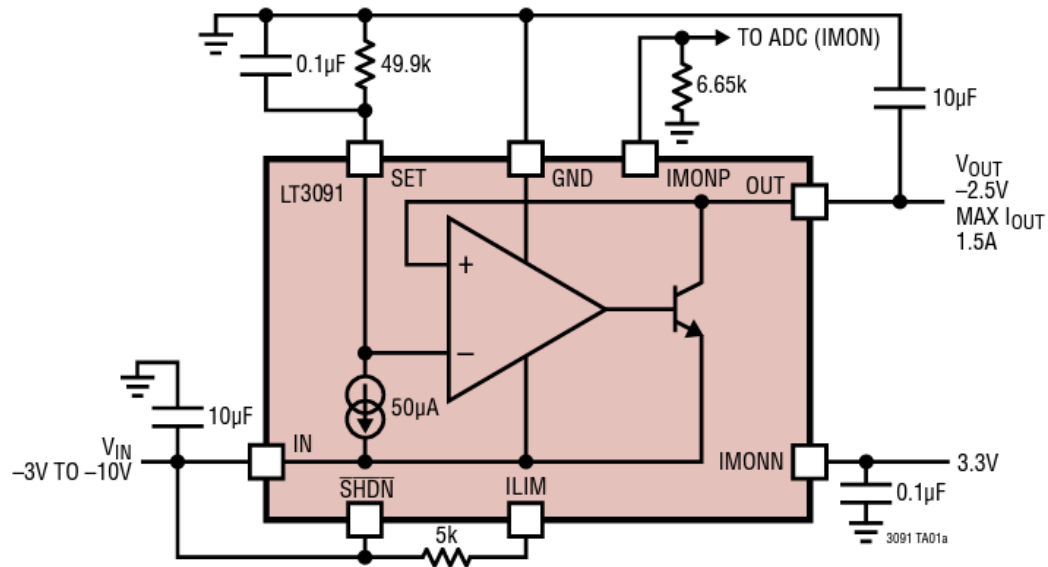


In order to bias the analog input stage of SparkPix-S we need:

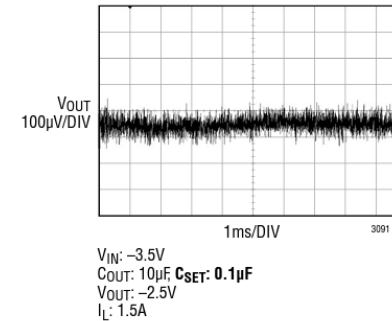
- **a stable, low noise 0.6 V voltage**
- **Sinking about 2.4 A of current**
- Rout seen by the pad:  $\frac{1}{g_m} * \frac{1}{N_{ch}} \approx \frac{1}{150 \mu S} * \frac{1}{160k} \approx 0.04 \Omega$
- Peak current on a single channel: we see a positive 1uA spike for the max FSR signal, and a negative 0.6 uA spike during reset.
- **Peak current on full matrix: +1.6 mA (x1600 pixel hit), -96 mA on reset (160k pixel reset all the time)**

Low impedance node, considere using protection diodes!!

# LT3091 Negative Linear Regulator (1.5 A)



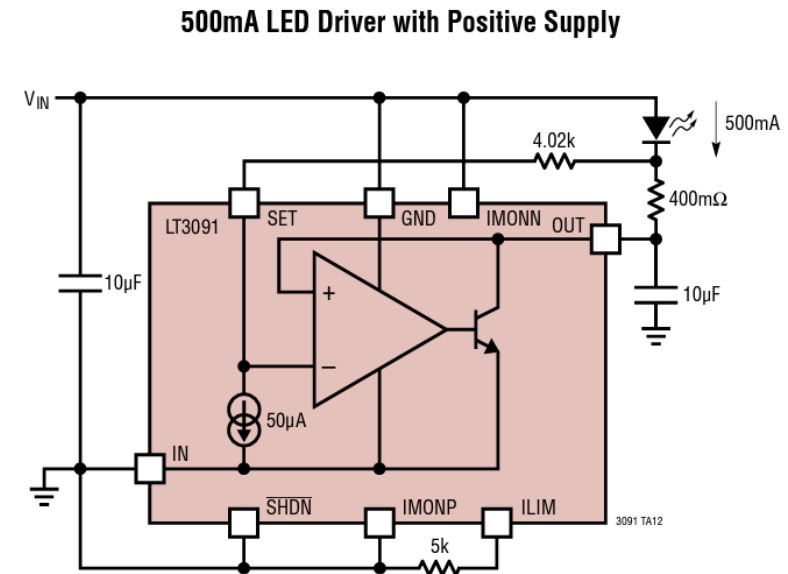
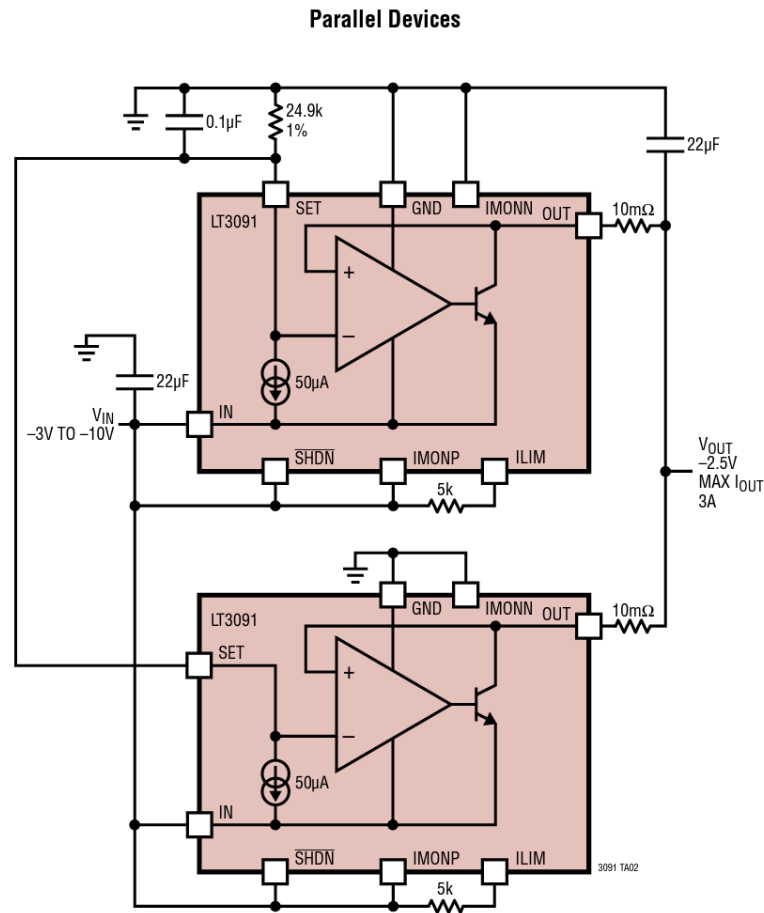
Output Noise: 10Hz to 100kHz



- Output Current: 1.5A
- Single Resistor Sets Output Voltage
- 50µA SET Pin Current: ±1% Initial Accuracy
- Programmable Current Limit
- Positive or Negative Output Current Monitor
- Parallelable for Higher Current and Heat Spreading
- Low Dropout Voltage: 300mV
- **Low Output Noise: 18µV<sub>RMS</sub> (10Hz to 100kHz)**
- Configurable as a 3-Terminal Floating Regulator
- Wide Input Voltage Range: -1.5V to -36V
- Rail-to-Rail Output Voltage Range: 0V to -32V
- Positive/Negative Shutdown Logic or UVLO
- Programmable Cable Drop Compensation
- Load Regulation: 1.2mV (1mA to 1.5A)
- Stable with 10µF Minimum Output Capacitor
- Stable with Ceramic or Tantalum Capacitors
- Thermally Enhanced 14-Lead 4mm × 3mm DFN, 16-Lead TSSOP, 7-Lead TO-220 and DD Packages

# Typical Applications (from datasheet)

From datasheet architectures for typical applications, we see both parallel devices in order to increase the max current, and a positive output voltage with current sinking



# Design notes

## Current Monitoring (IMONN and IMONP)

The LT3091 incorporates a precision positive or negative current monitor. As illustrated in the Block Diagram, the negative current monitor pin (IMONN) sinks current proportional (1:2000) to the output current while the positive current monitor pin (IMONP) sources current proportional (1:4000) to the output current. For proper operation, ensure IMONN is at least 2V above IN and IMONP.

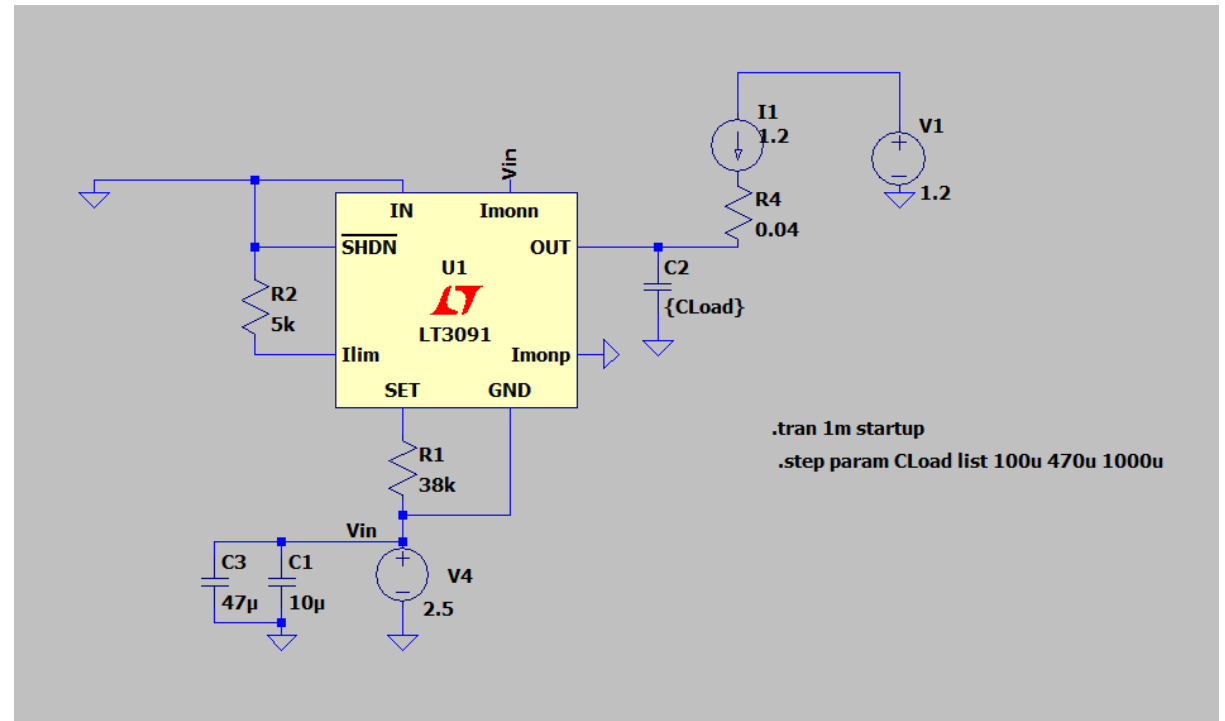
When unused, IMONN and IMONP pins can be left floating; however, this slightly reduces (~5%) the device's internal current limit. Hence, if the current monitor functionality is not used, as shown in Figure 1, it is recommended to tie IMONN to GND and IMONP to IN.

## Externally Programmable Current Limit

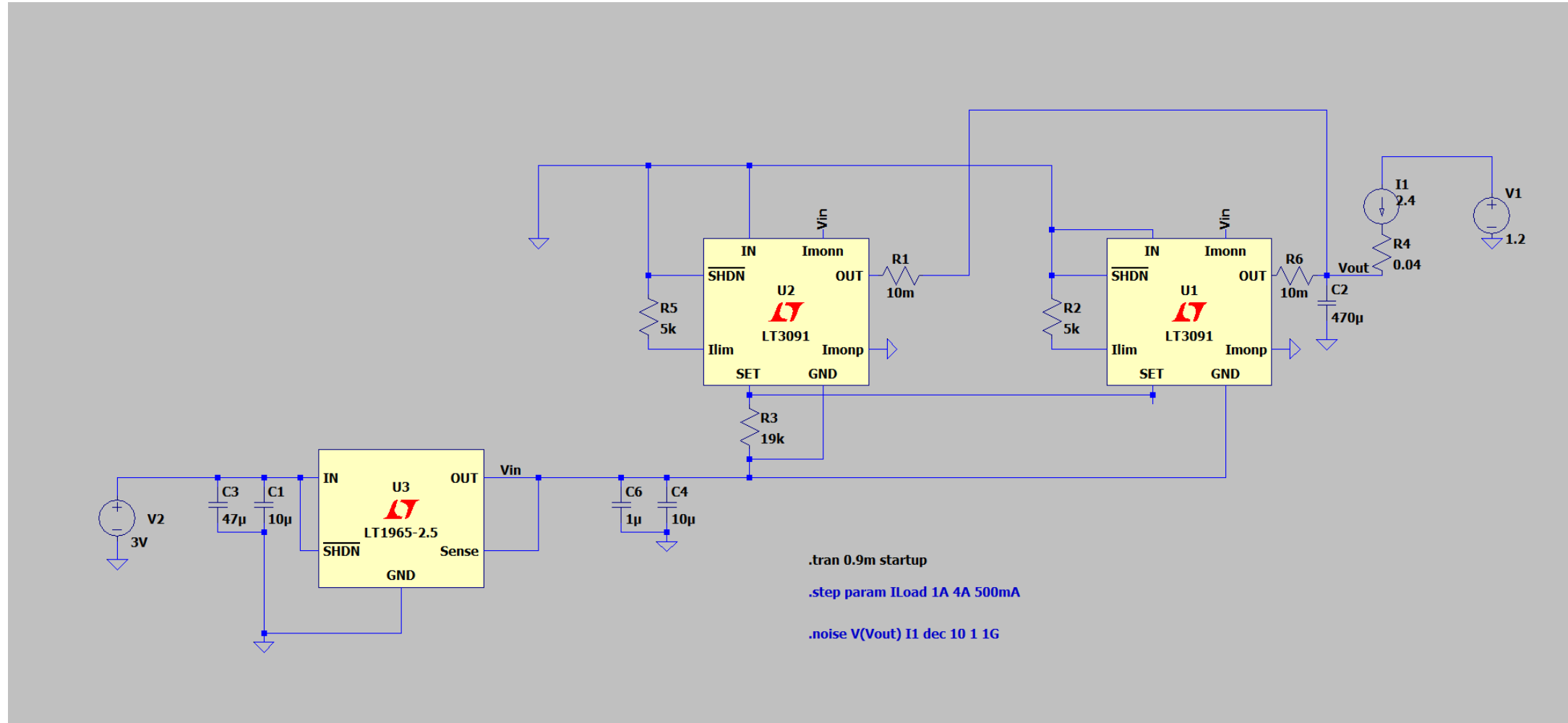
ILIM can be tied to IN if external programmable current limit is not needed. However, because the ILIM pin is internally regulated to 225mV above IN, if ILIM pin is shorted to IN, then this loop current limits, causing the LT3091's quiescent current to increase by about 300µA. Hence, when unused, it is recommended to tie ILIM to IN through a 5k resistor.

## GND Pin Versatility of LT3091

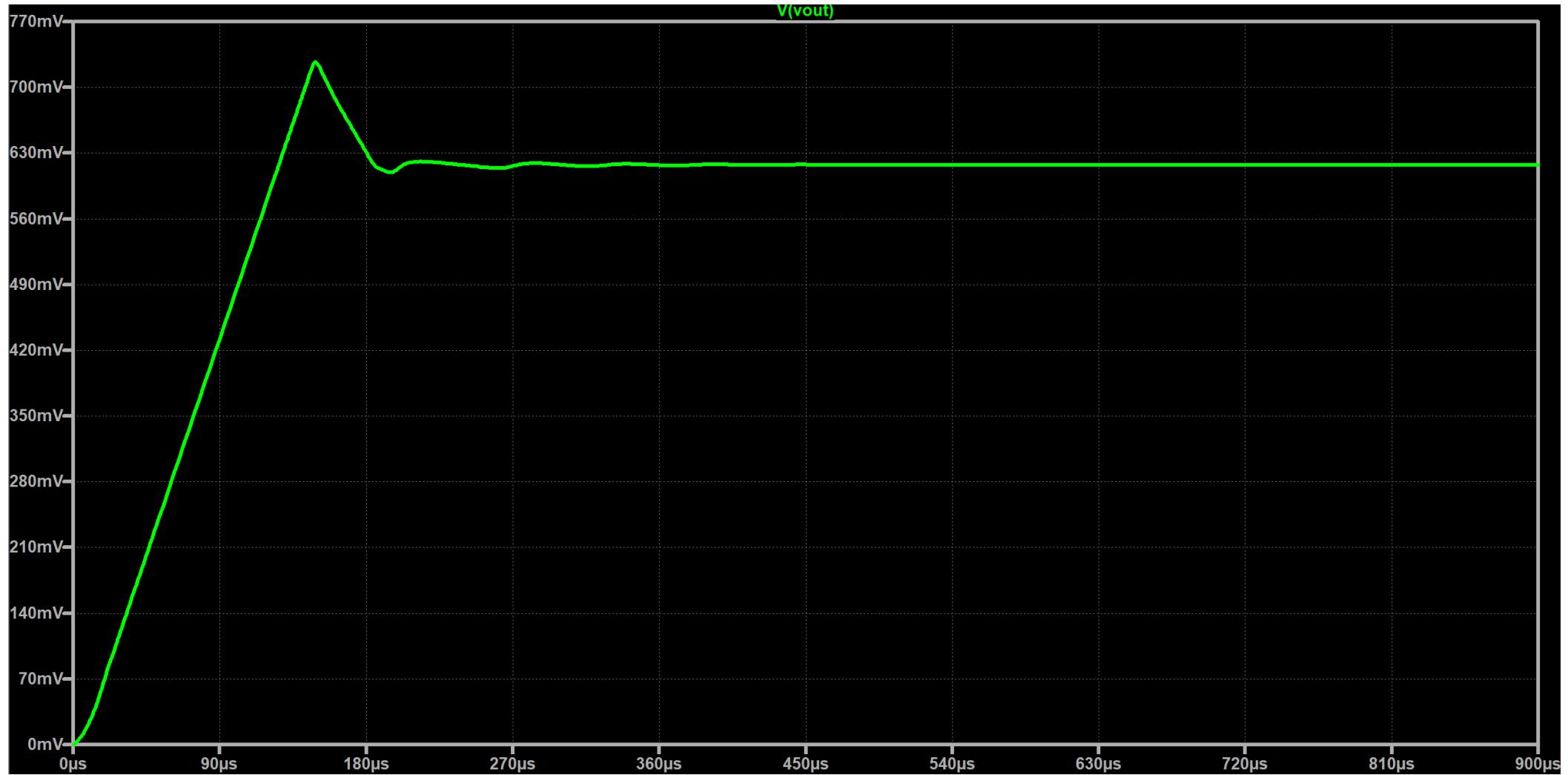
connected. The GND pin does not need to be connected to system ground! It can be connected to a positive voltage as well. If the GND pin of LT3091 is tied to a positive voltage that is at least 1.9V above  $V_{IN}$ , then  $V_{IN}$  can be set below the LT3091's -1.9V minimum input voltage. As long as there is 1.9V between IN and GND pins of LT3091, the minimum operating voltage is satisfied. Now it can



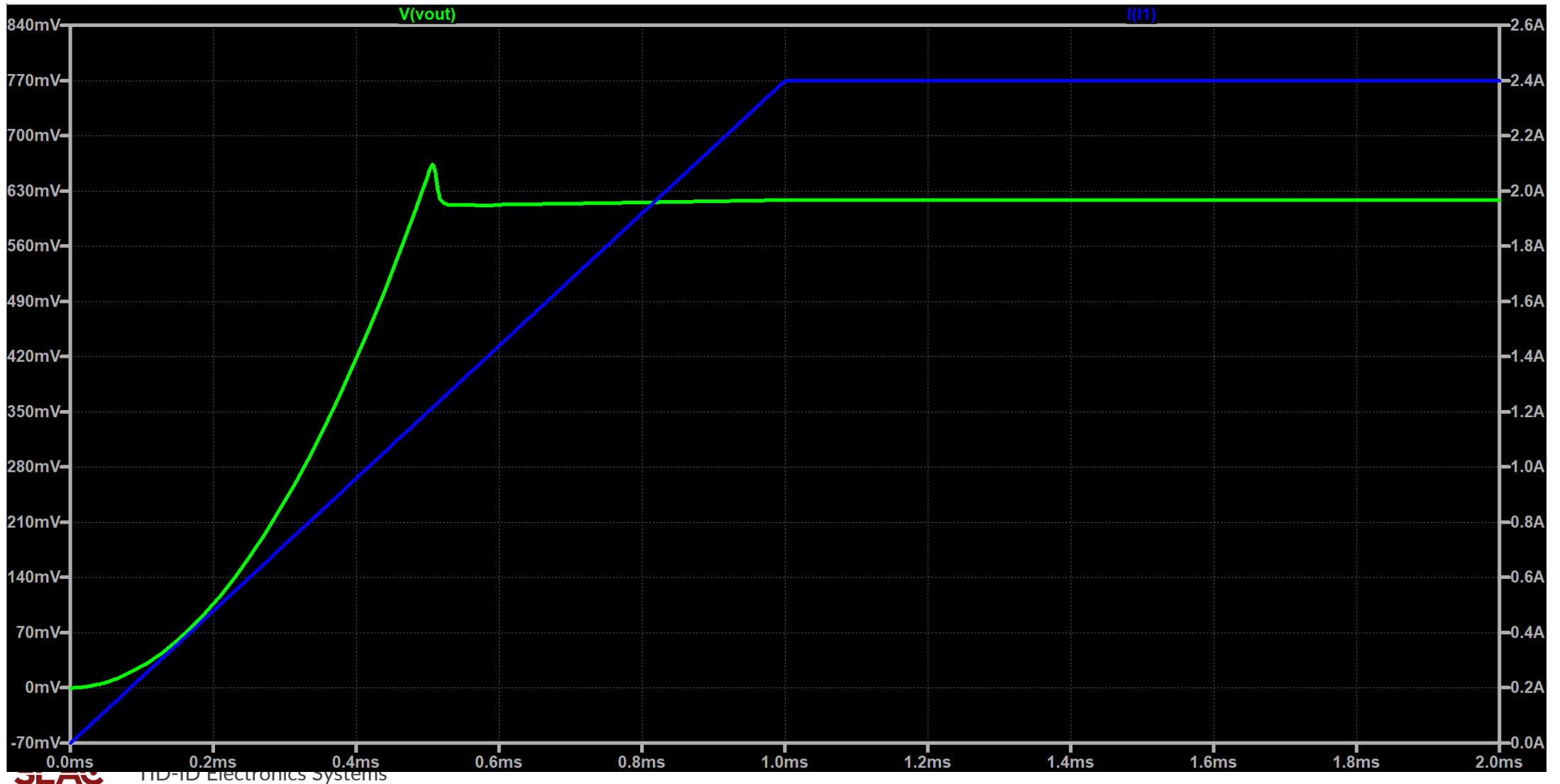
# LT3091 with real 2.5 V reference



# Startup (.tran 0.9m startup)

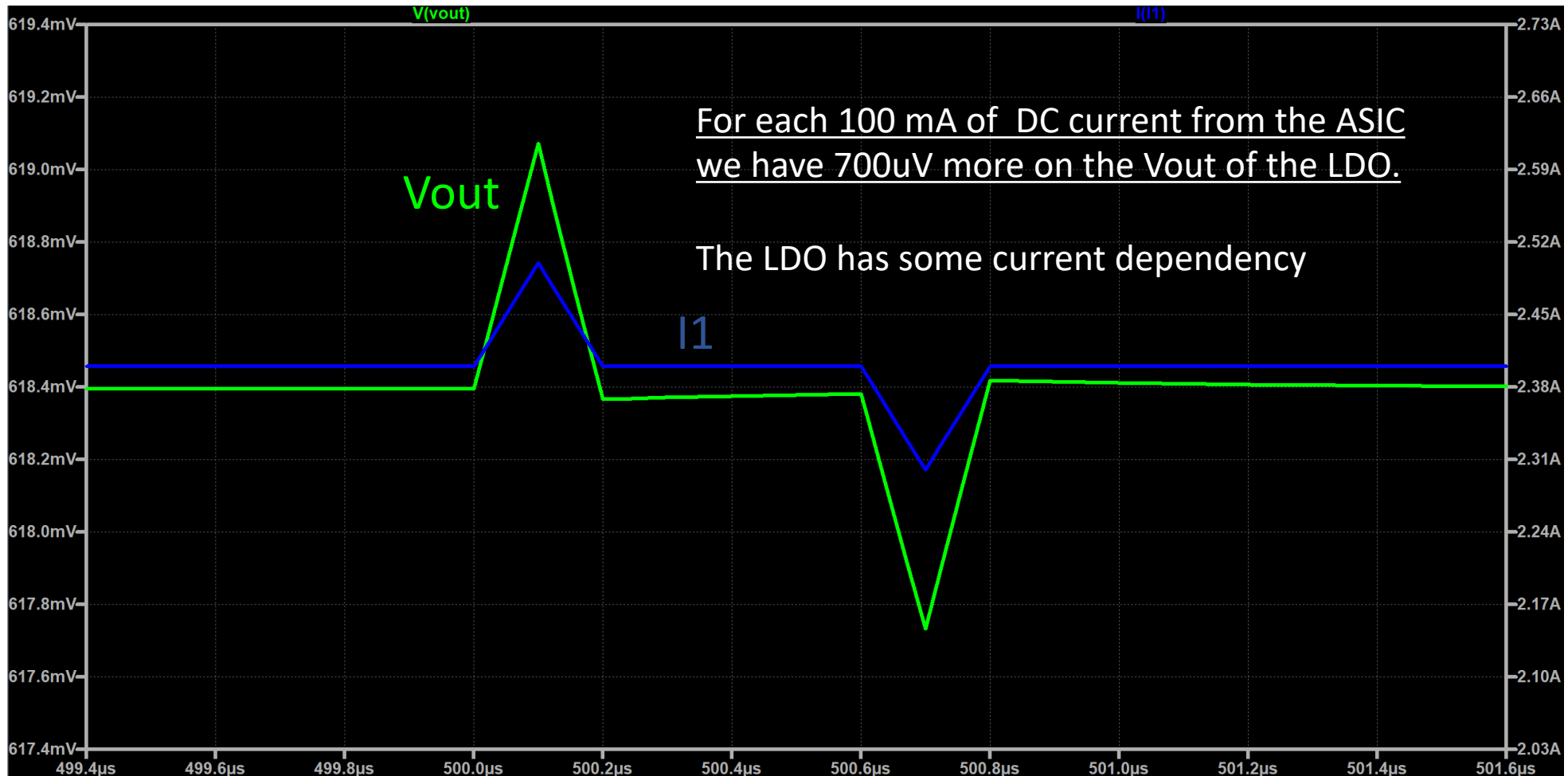


# I1 ramp ()

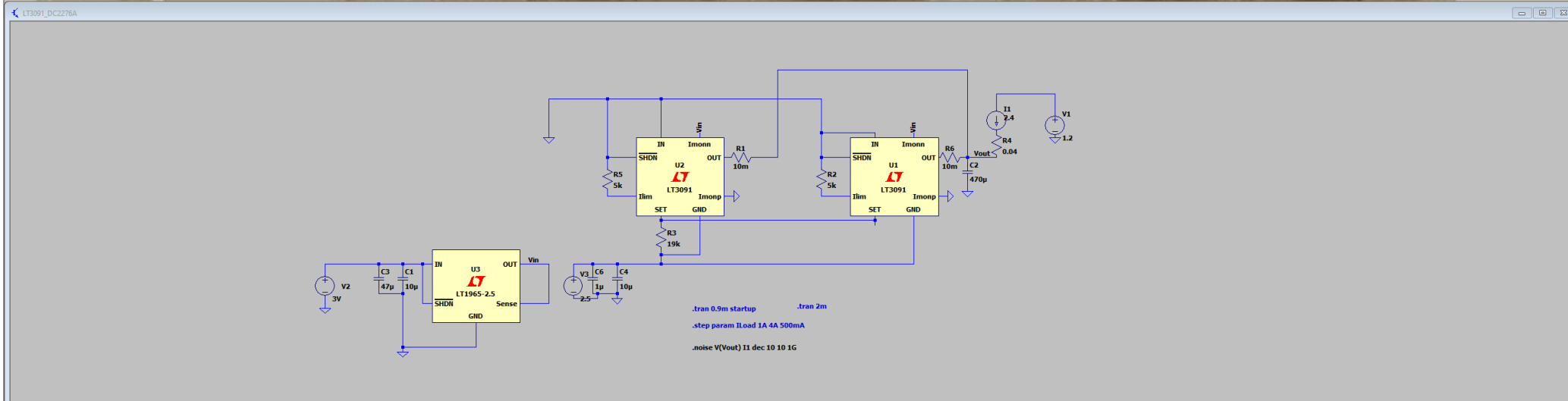
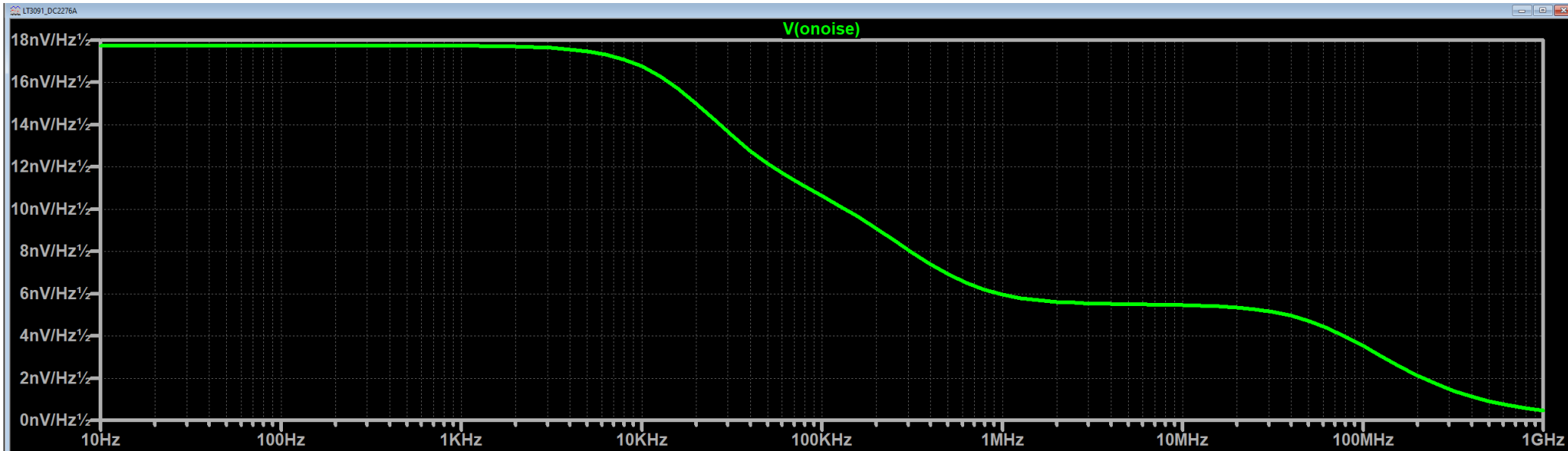




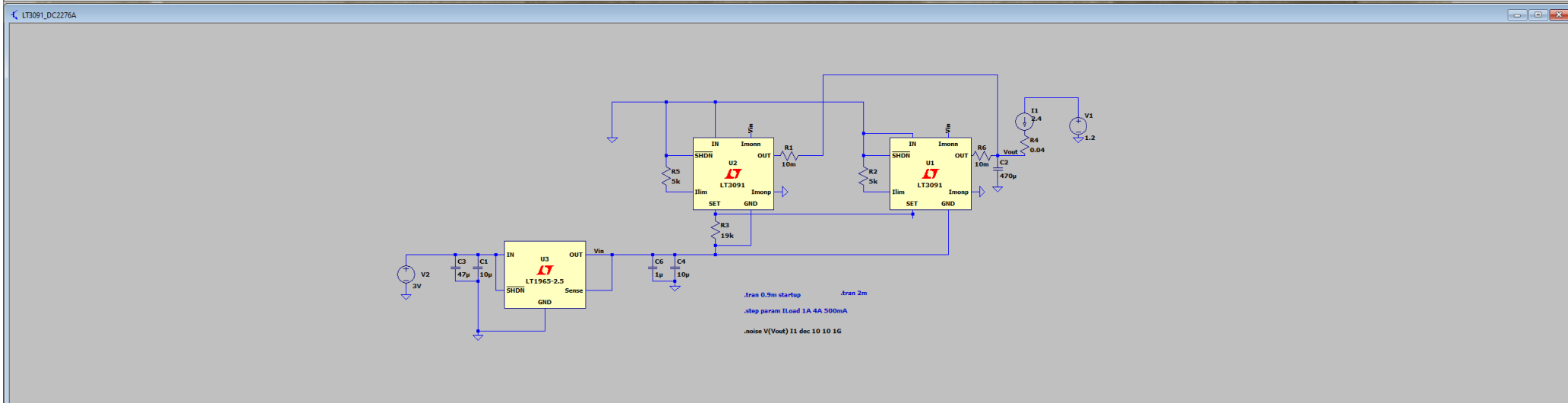
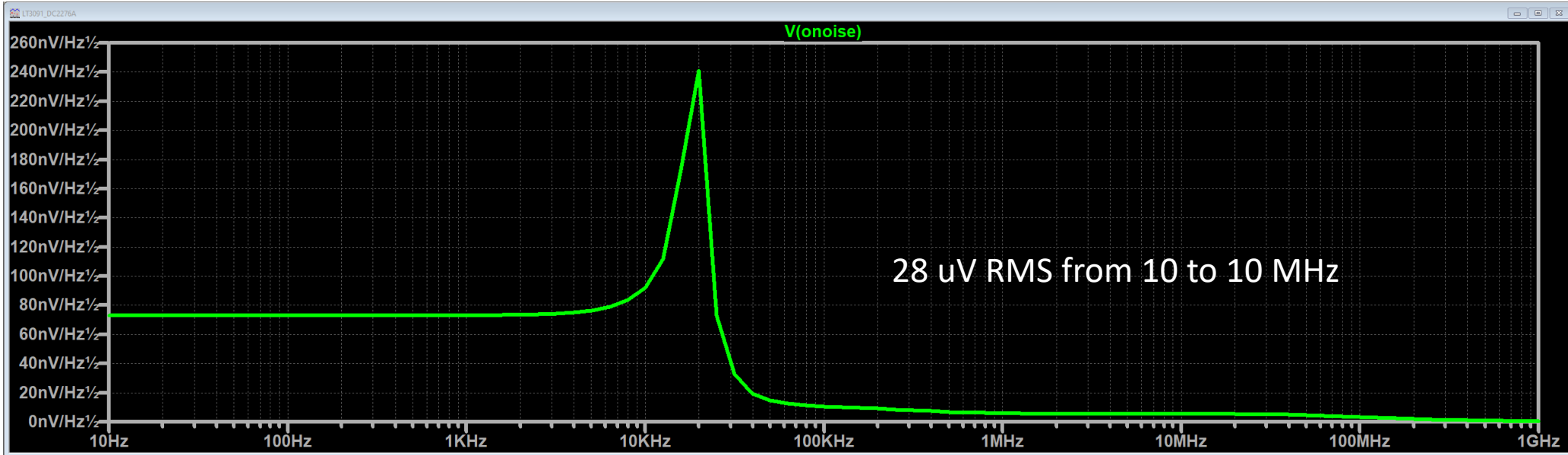
# Current spikes (+-100 mA around 2.4)



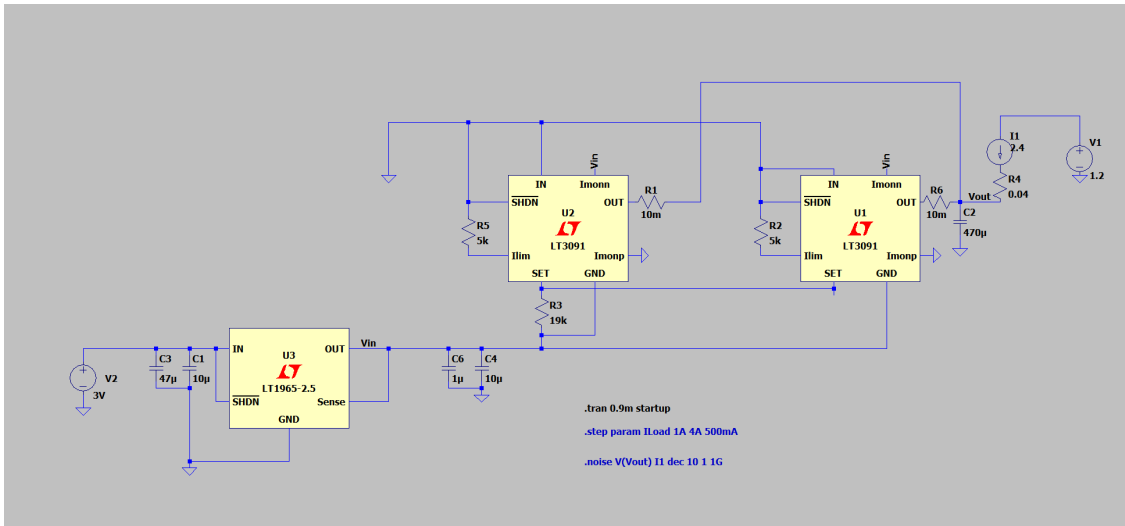
# Noise plot with ideal 2.5V ref



# Noise plot with real 2.5V ref (LT1965-2.5)



# 2.5V LDO power consumption



The 2.5V LDO does not need a lot of current.  
Only a few mA at most are drawn for the loop control

Parameter	Conditions	1.0V	1.5V	2.0V	Unit
SET Pin Current ( $I_{SET}$ )	$V_{IN} = -1.9V$ , $I_{LOAD} = 1mA$ $-36V < V_{IN} < -1.9V$ , $1mA < I_{LOAD} < 1.5A$ (Note 5)	49.5	50	50.5	$\mu A$
GND Pin Current	$I_{LOAD} = 20\mu A$	1.2	2.0		mA
$V_{IN} = V_{OUT(NOMINAL)}$ (Note 8)	$I_{LOAD} = 1mA$	1.2	2.0		mA
	$I_{LOAD} = 100mA$	2.6	5.5		mA
	$I_{LOAD} = 500mA$	9.3	20		mA
	$I_{LOAD} = 1.5A$	40	80		mA

**Note 8.** GND pin current is tested with  $V_{IN} = V_{OUT(NOMINAL)}$  and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages.