XTCAV and STCAV project overview

Kuktae Kim

Technology Innovation Directorate - Controls Data Systems Division

5/5/2023

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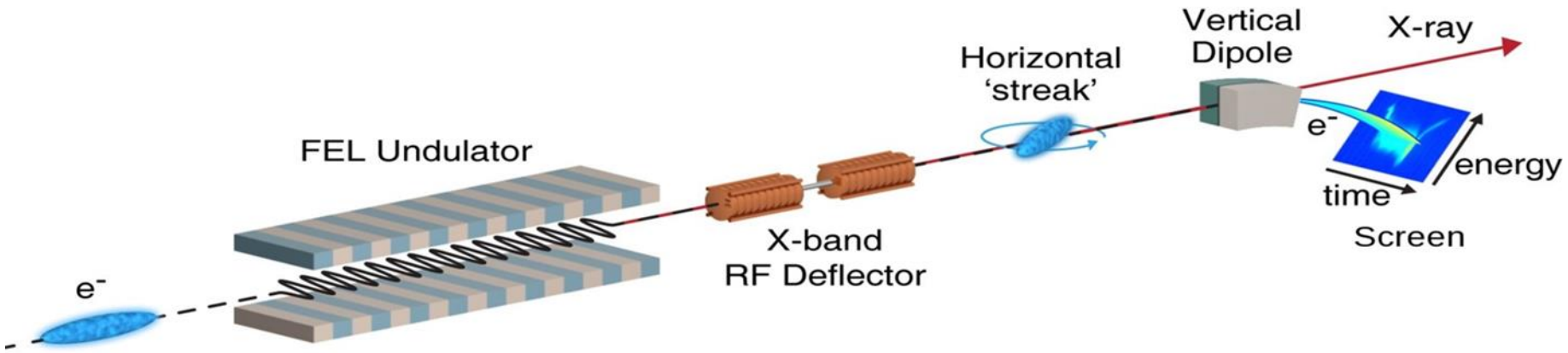
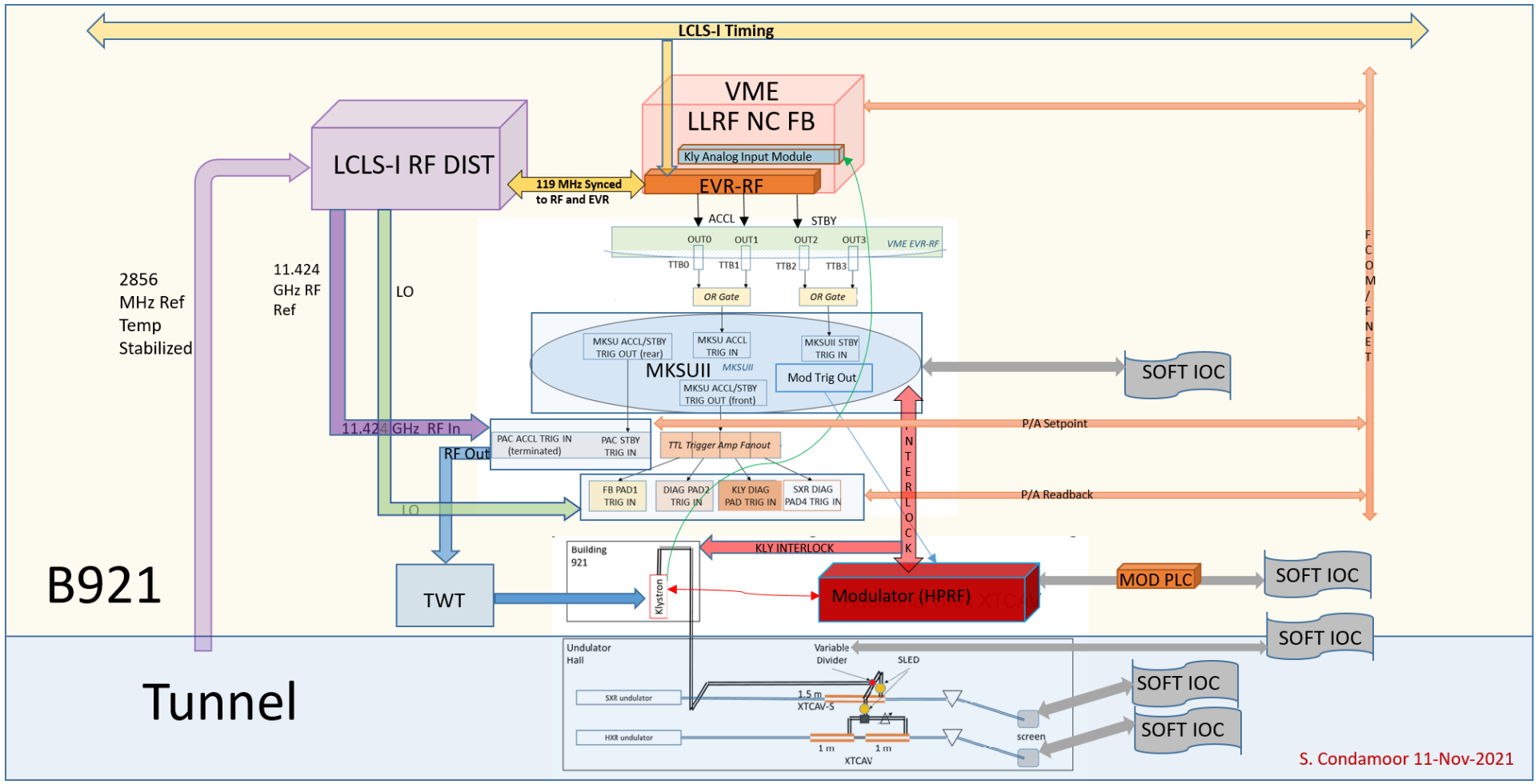
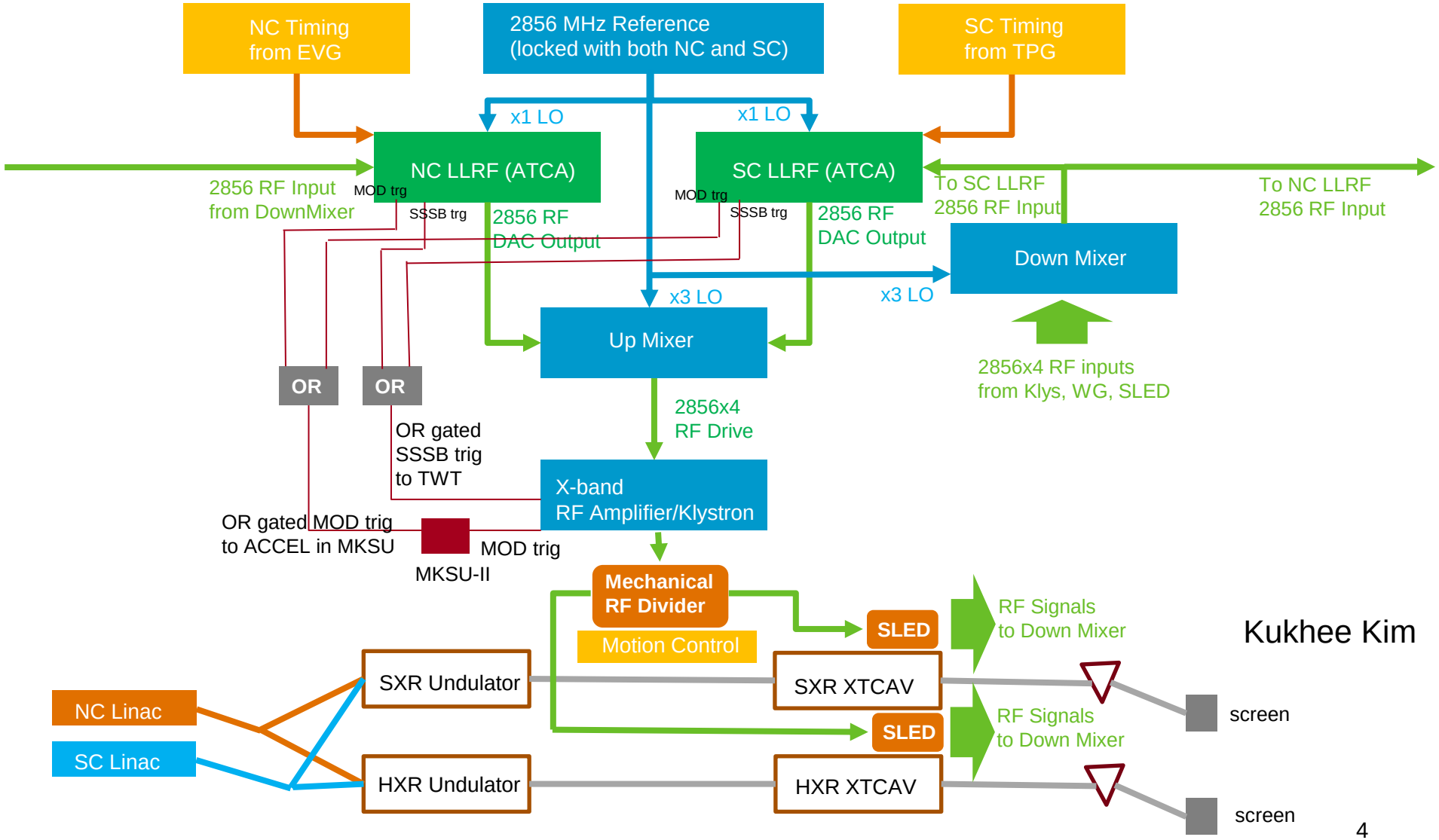
XTCAV


Vertical
Dipole
X-ray
Horizontal
'streak'
e⁻
FEL Undulator
energy
time
X-band
RF Deflector
e⁻
Screen

ATCA LLRF for XTCAV_NC_SC Existing System



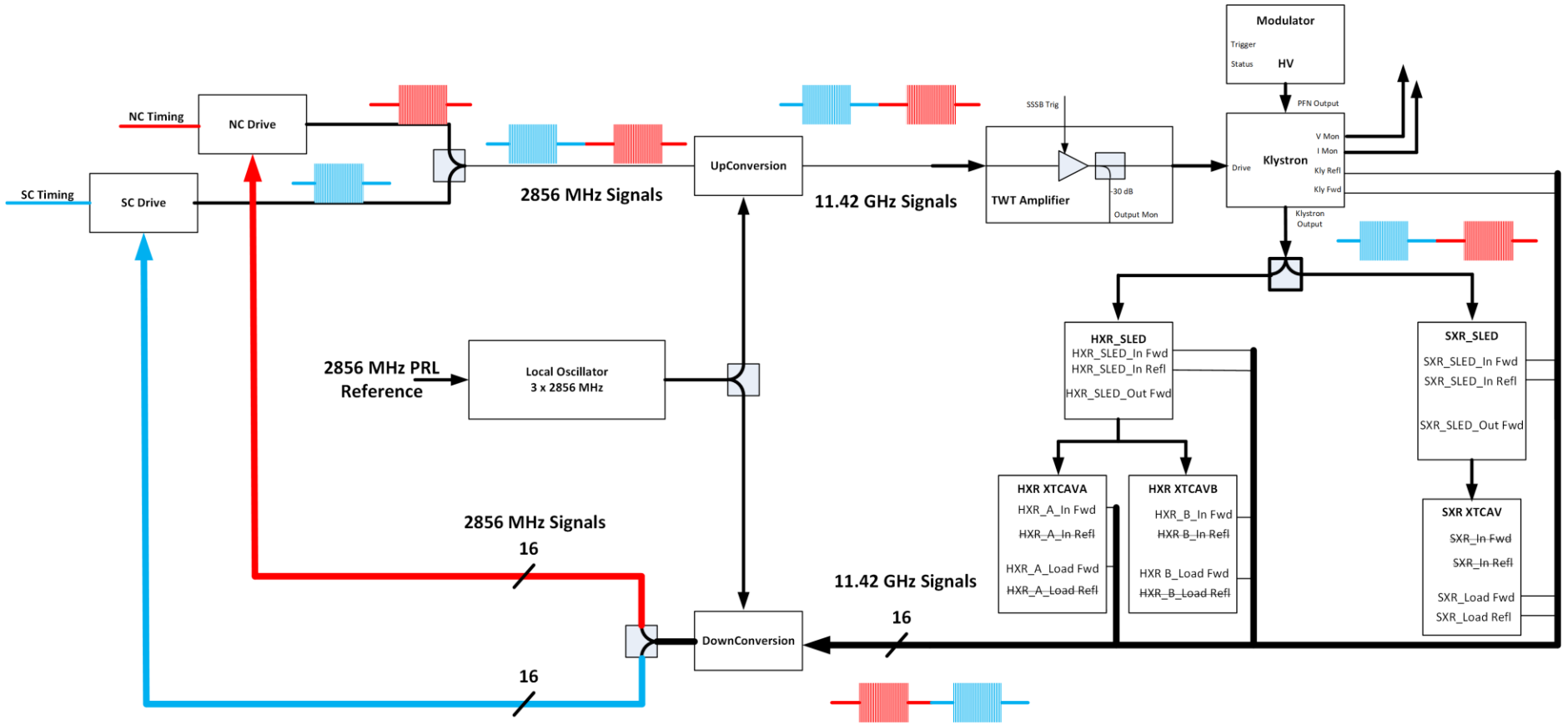
ATCA LLRF for XTCAV_NC_SC Proposed Changes



Kukhee Kim

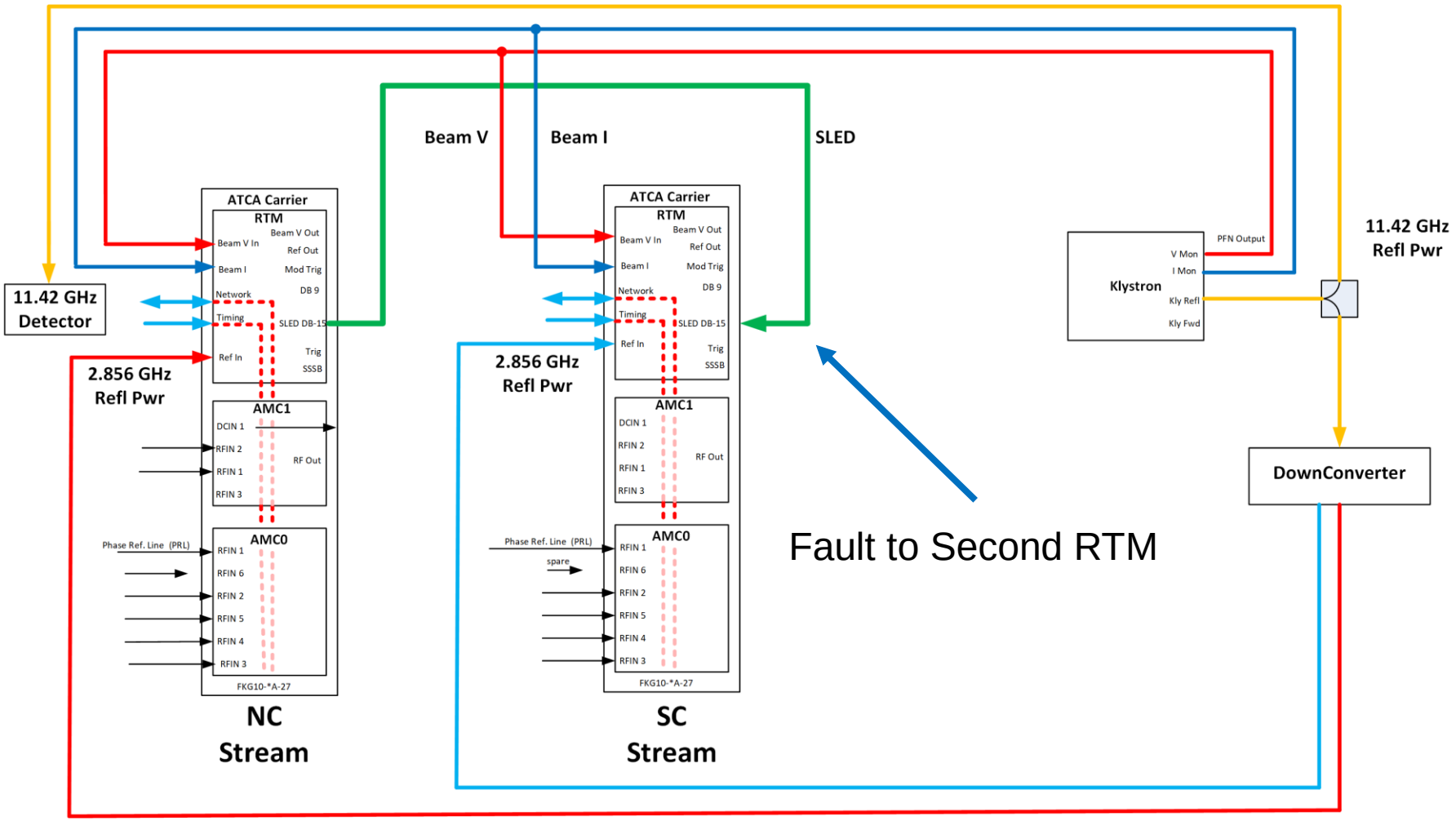
ATCA LLRF for XTCAV_NC_SC

Interleaved RF from Two Timing Streams

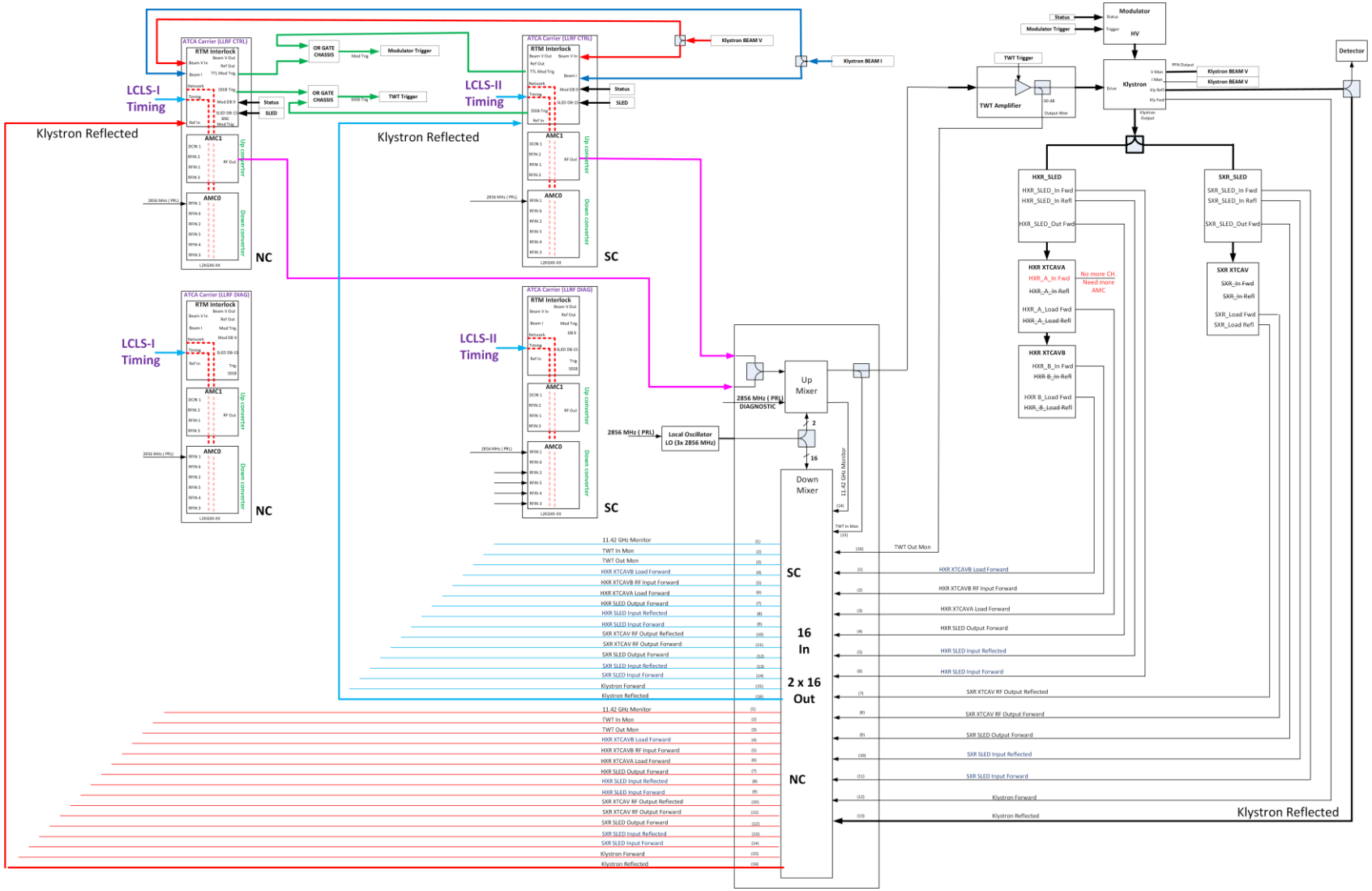


ATCA LLRF RTM Interlocks

RTM Interlocks for Klystron V, I and Reflected Power



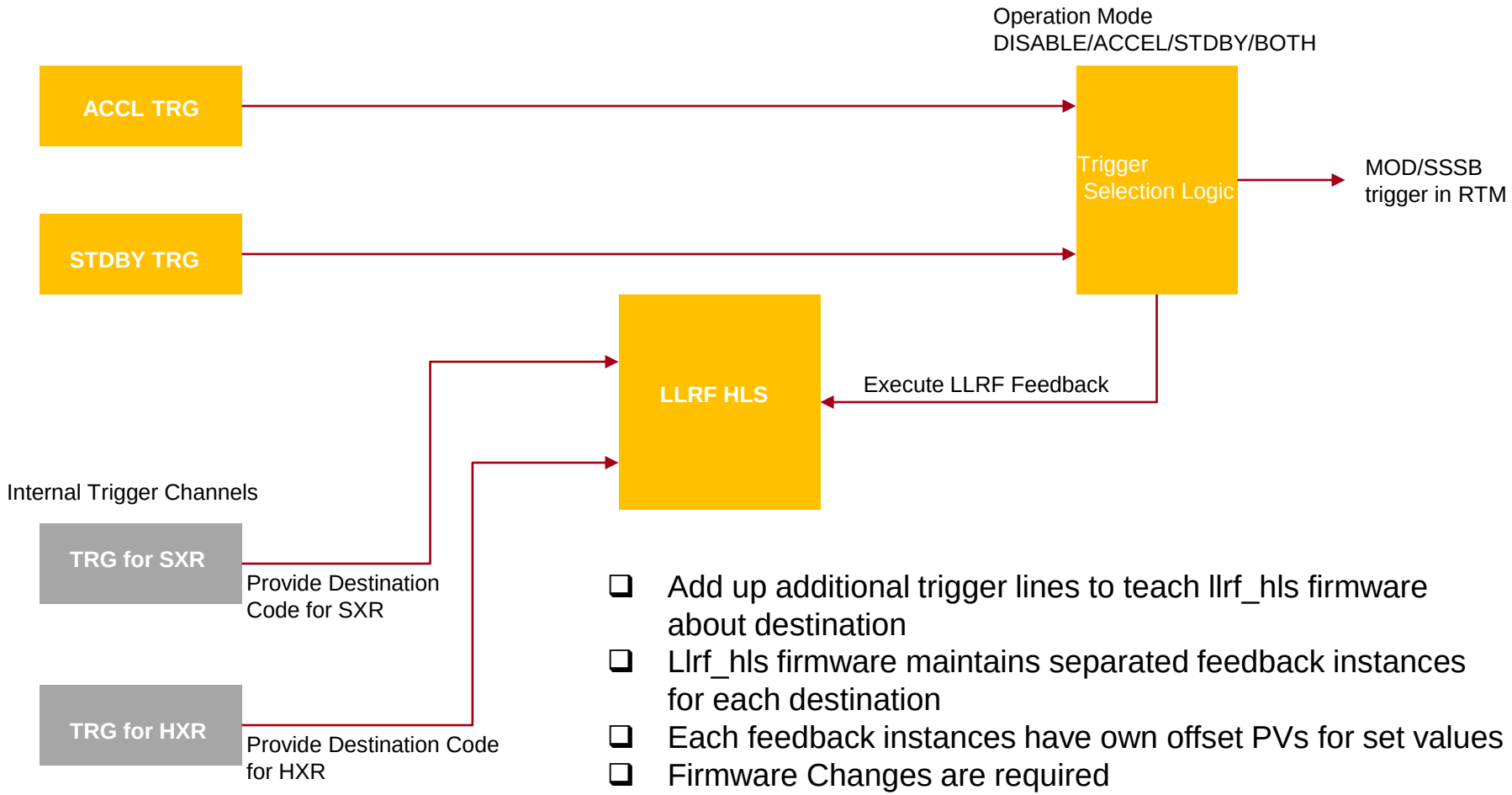
ATCA LLRF for XTCAV_NC_SC System



Interleaving Sources and Destination (PAU)

- Interleaving of source is handled by the trigger and separated LLRF cards
  - NC beam / NC LLRF with NC XTCAV = NC_HXR_XTCAV | NC_SXR_XTCAV
  - SC beam / SC LLRF with SC XTCAV = SC_HXR_XTCAV | SC_SXR_XTCAV
  - Different set values, readback values and feedback are maintained by different systems (NC LLRF and SC LLRF) independently
- Interleaving of destination
  - Need to drive different set values for different destination
  - Allocated internal trigger channels (in the timing-core) for each destination (HXR and SXR)
  - Base firmware provide destination code to HLS firmware when a trigger occurred on the internal trigger channel
  - HLS firmware adds up proper offset on the set values for driving RF depends on the destination code from the internal trigger channel
- Equivalent with the software PAU (pattern aware unit), but minimize the firmware changes

Trigger/PAU Implementation in the ATCA Firmware



- Add up additional trigger lines to teach llrf_hls firmware about destination
- Llrf_hls firmware maintains separated feedback instances for each destination
- Each feedback instances have own offset PVs for set values
- Firmware Changes are required

Extension of Trigger Configuration

- Trigger Channel Assignment for UED

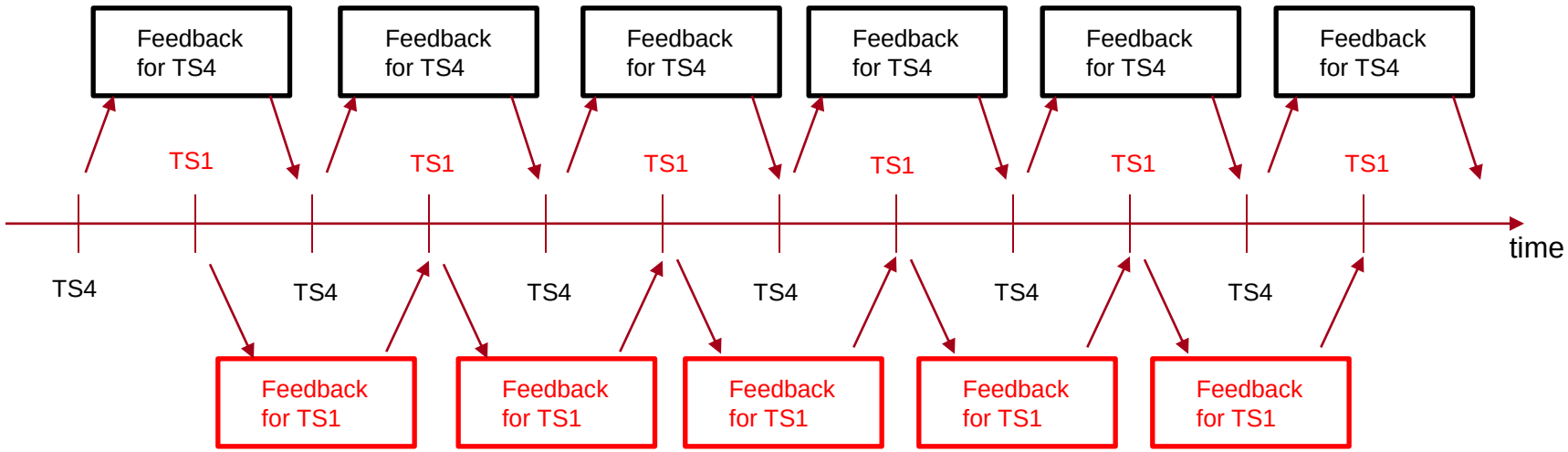
Trigger Channel Number	Name	Purpose / Remarks
0	LLRF Accel	Drive llrfHls firmware
1	LLRF StdBy	
2	MOD Accel	Modulator Trigger Output
3	MOD StdBy	
4	RTM Accel	Drive RTM firmware
5	RTM StdBy	
6	SSSB Accel	SSSB Trigger Output
7	SSSB Stdby	
8	DaqMux Accel	Driv DaqMux
9	DaqMux Stdby	
10	Check Timeslot	Getting Timeslot Information
11	Destination HXR	Getting Destination
12	Destination SXR	Getting Destination

Making destination-aware timeslot with 3 triggers for PAU function

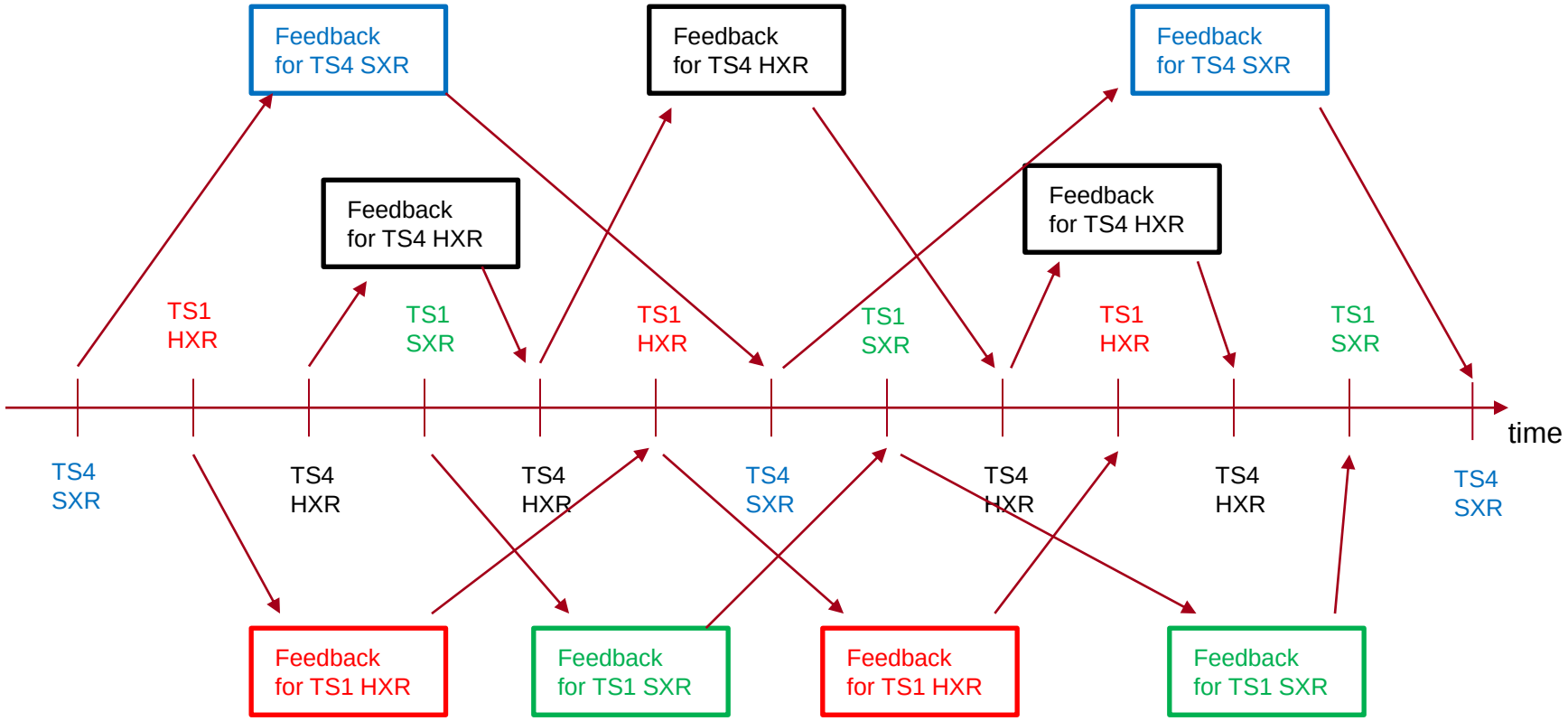
$$\begin{cases} t = t_{AC} + 6n & \text{; Destination aware timeslot from AC timeslot and destination index} \\ n \in \{0 : \mathrm{HXR}, 1 : \mathrm{SXR}\} & \text{; Destination Index} \end{cases}$$

Remark) Since, we have 18 virtual timeslots,
we can have up to 3 different

Timeslot Aware Operation (Current Implementation)

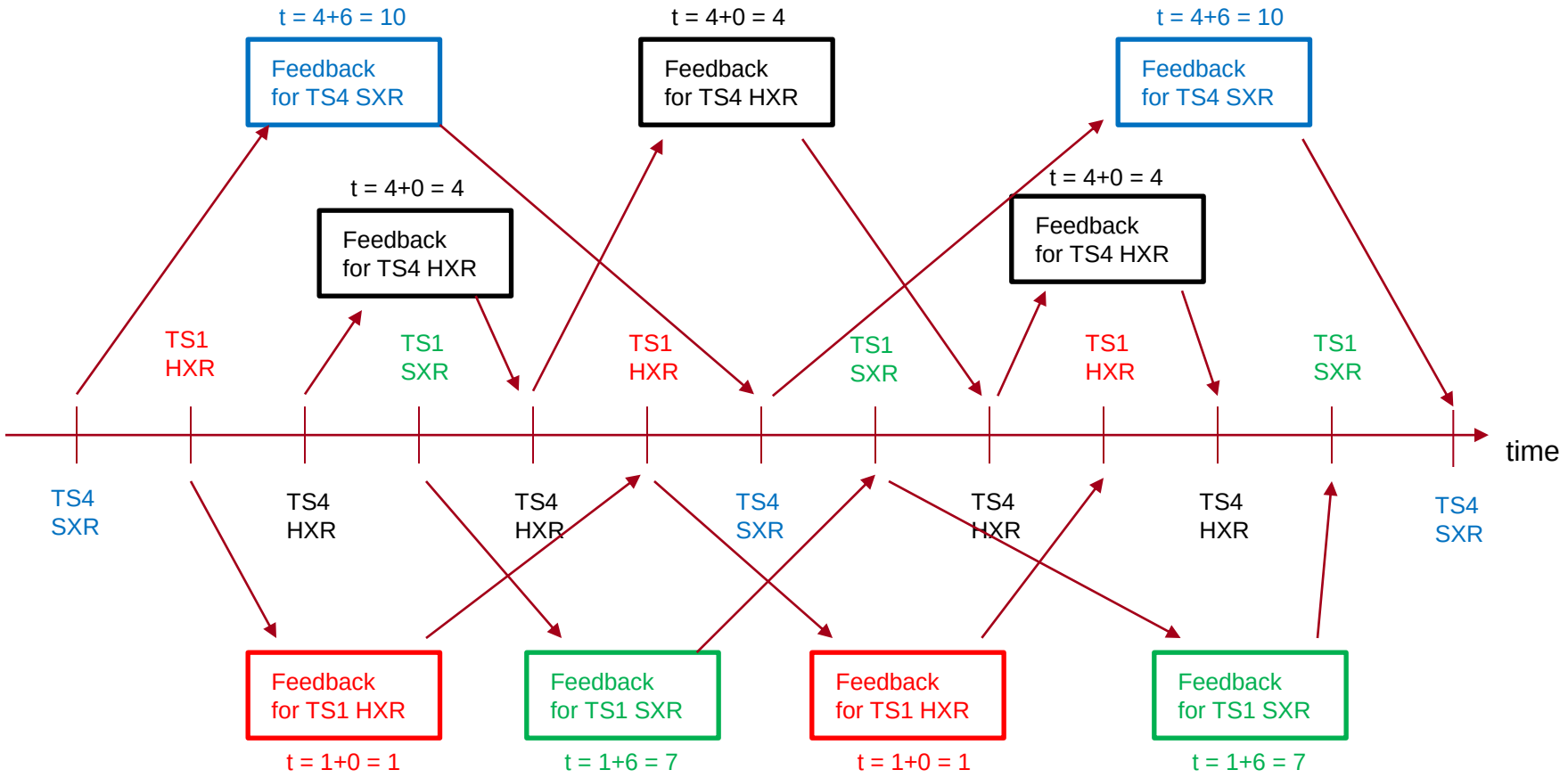


Pattern Aware (Timeslot Aware + Destination Aware)



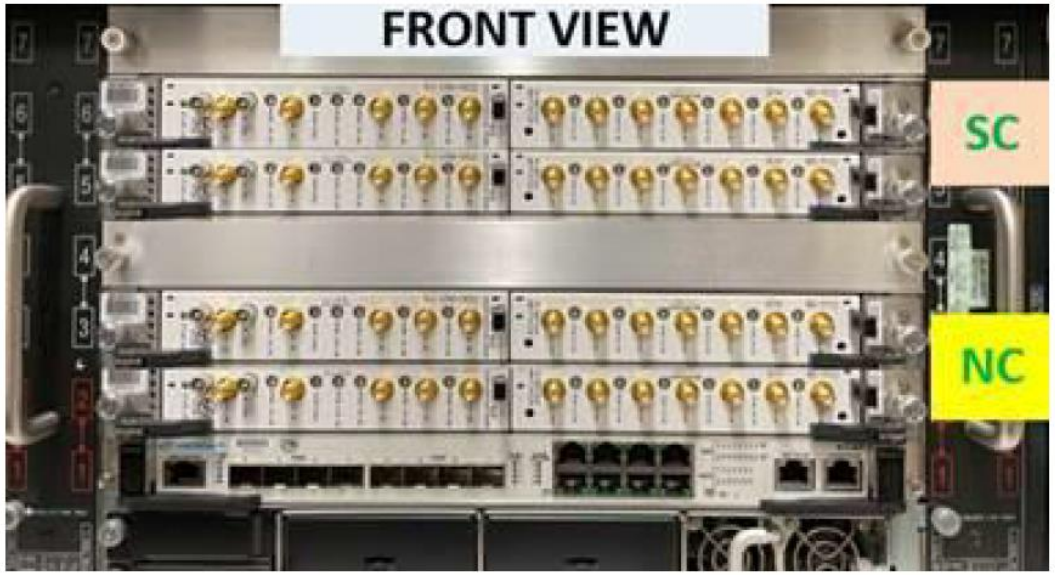
Pattern Aware with Virtual Timeslot

$$\begin{cases} t = t_{AC} + 6n & \text{; Destination aware timeslot from AC timeslot and destination index} \\ n \in \{0 : \mathrm{HXR}, 1 : \mathrm{SXR}\} & \text{; Destination Index} \end{cases}$$



XTCAV In B921

Installation (Timing & PRL)



Slot 6 SC - HXR & SXR 2856 MHz LLRF Diagnostic

Slot 5 SC - HXR & SXR 2856 MHz LLRF Controller

Slot 3 NC - HXR & SXR 2856 MHz LLRF Diagnostic

Slot 2 NC - HXR & SXR 2856 MHz LLRF Controller

- Work with Richard Burgess for LCLS-I/LCLS-II timing fiber drops. Work with Matt Weaver for 2856 MHz PRL.

Slot 6 SC - HXR & SXR LLRF RTM (LCLS-II Timing)

Slot 5 SC - HXR & SXR LLRF RTM (LCLS-II Timing)

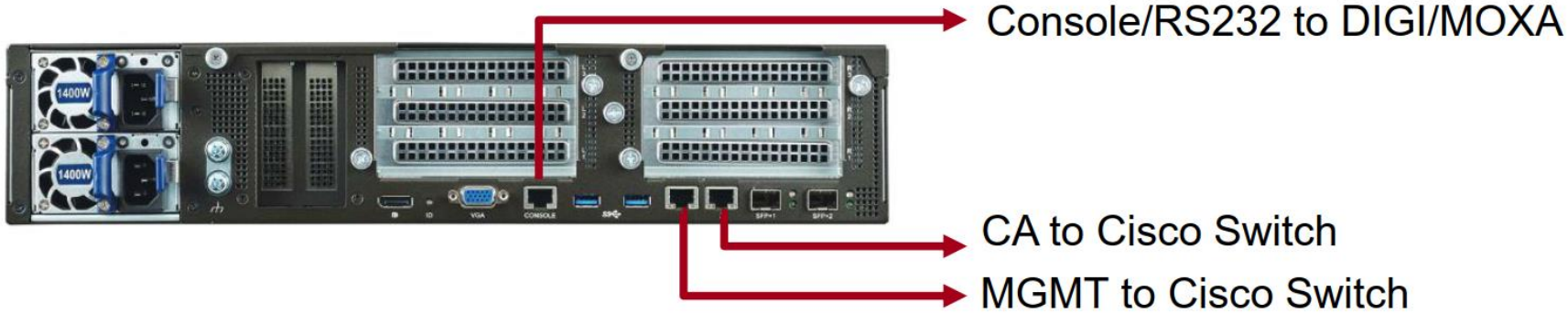
Slot 3 NC - HXR & SXR LLRF RTM (LCLS-I Timing)

Slot 2 NC - HXR & SXR LLRF RTM (LCLS-I Timing)

Installation (2U Advantech Server, SKY-8201)

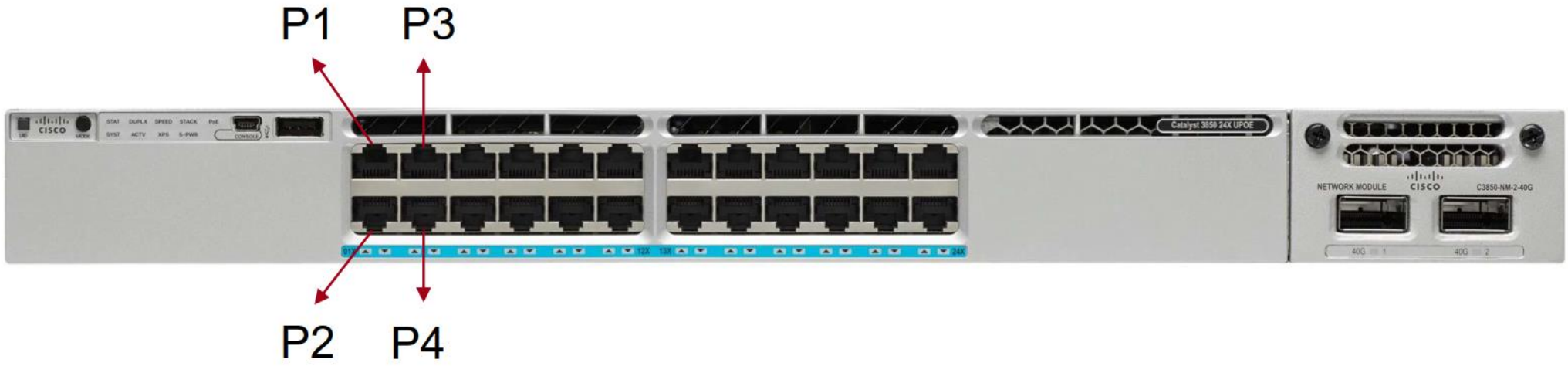
Front View

Rear View

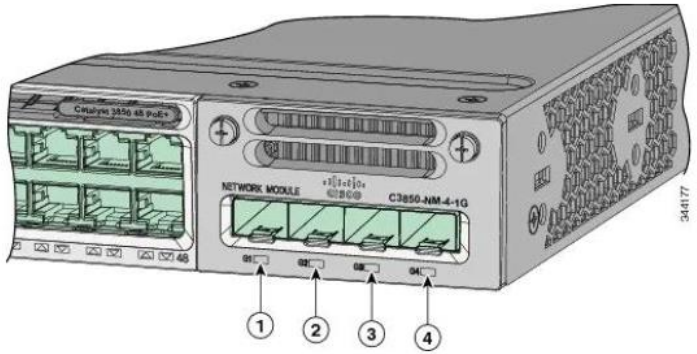


Installation (Vadatech Switch, ATCA Crate Slot 1)

Installation (Network)



Port 1 – 2U Advantech Server MGMT
Port 2 – 2U Advantech Server CA
Port 3 – ATCA Shelf Manager
Port 4 – ATCA Switch (Slot 1)



Fiber network module can be swapped out for more capacity

Installation (Console RS232)

Test stand for XTCAV In B15

Test stand for the LLRF Control system in B15

< RACK No.: B015-121-R06 >

< Front >

VME CRATE - LCLSI TIMING FANOUT

FEEDTHRU

CPU-B15-SP02

FEEDTHRU

TEKTRONIC SCOPE 4CH
Digital oscilloscopes

FEEDTHRU/WORKSPACE

ATCA CRATE: SHM-B15-SP02-1

Slot 7: Empty - Available
Slot 6: Empty - Available
Slot 5: Empty - Available
Slot 4: Empty - Available
Slot 3: Empty - Available
Slot 2: LLRF Upconverter LLRF Down Converter
Slot 1: Switch Blade 10G

FEEDTHRU/WORKSPACE

CPU-B15-RF03

FEEDTHRU/WORKSPACE

ATCA CRATE: SHM-B15-RF03-1

Slot 7: Empty - Available
Slot 6: LLRF Upconverter LLRF DownConverter(SC) (SC-SXR 2856 Mhz PRL)
Slot 5: LLRF Upconverter LLRF DownConverter(SC) (SC-HXR 2856 Mhz PRL)
Slot 4: Empty - Available
Slot 3: LLRF Upconverter LLRF Down Converter(NC) (NC-SXR 2856 Mhz PRL)
Slot 2: LLRF Upconverter LLRF Down Converter(NC) (NC-HXR 2856 Mhz PRL)
Slot 1: Switch Blade 10G

< Rear >

VME CRATE - LCLSI TIMING FANOUT

FEEDTHRU

CPU-B15-SP02

FEEDTHRU

TEKTRONIC SCOPE 4CH
Digital oscilloscopes

FEEDTHRU/WORKSPACE

ATCA CRATE: SHM-B15-SP02-1

Slot 7: Empty - Available
Slot 6: Empty - Available
Slot 5: Empty - Available
Slot 4: Empty - Available
Slot 3: Empty - Available
Slot 2: LLRF Upconverter LLRF Down Converter
Slot 1: Switch Blade 10G

STCAV2 TEST STAND

FEEDTHRU/WORKSPACE

CPU-B15-RF03

FEEDTHRU/WORKSPACE

ATCA CRATE: SHM-B15-RF03-1

Slot 7: Empty - Available - Ai filler panel
Slot 6: RF Interlock RTM (SC-SXR_LCLS-II Timing)
Slot 5: RF Interlock RTM (SC-HXR_LCLS-II Timing)
Slot 4: Empty - Available - Air filler panel
Slot 3: RF Interlock RTM (NC-SXR_LCLS-I Timing)
Slot 2: RF Interlock RTM (NC-HXR_LCLS-I Timing)
Slot 1: Empty - Air filler panel

XTCAV TEST STAND

Test stand for the XTCAV2 LLRF Control system in B15 (1)

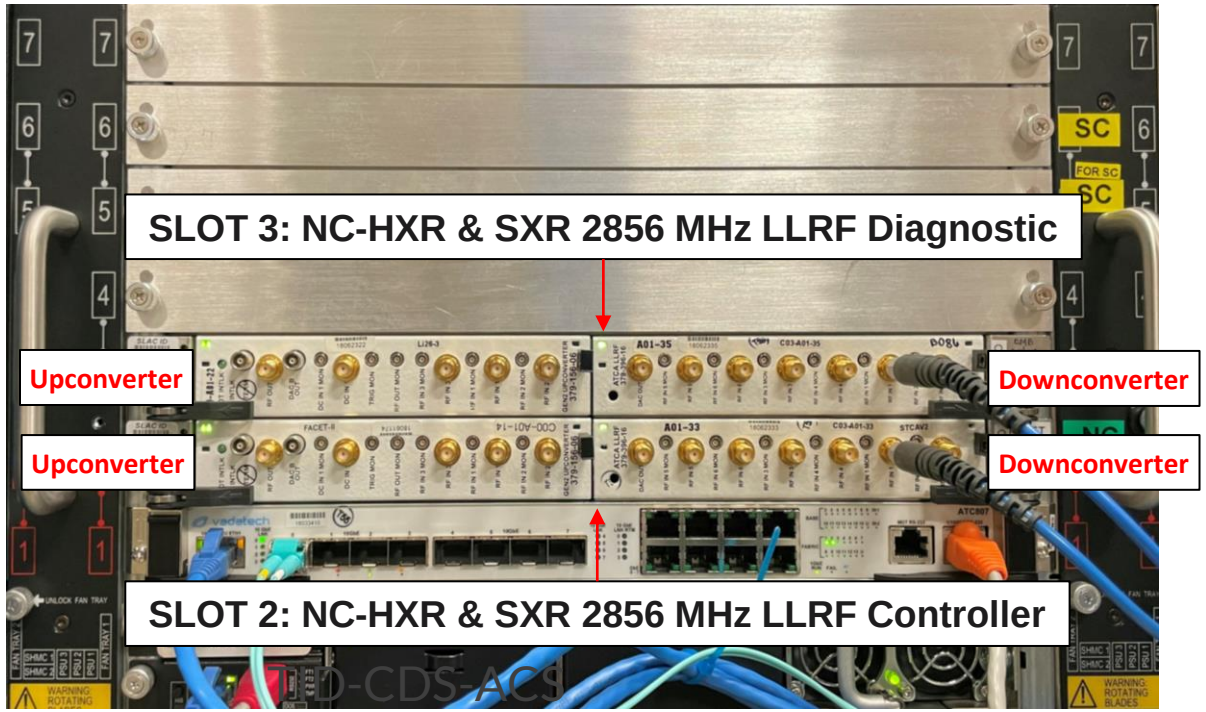
Shelf Manager: SHM-B15-RF03-1

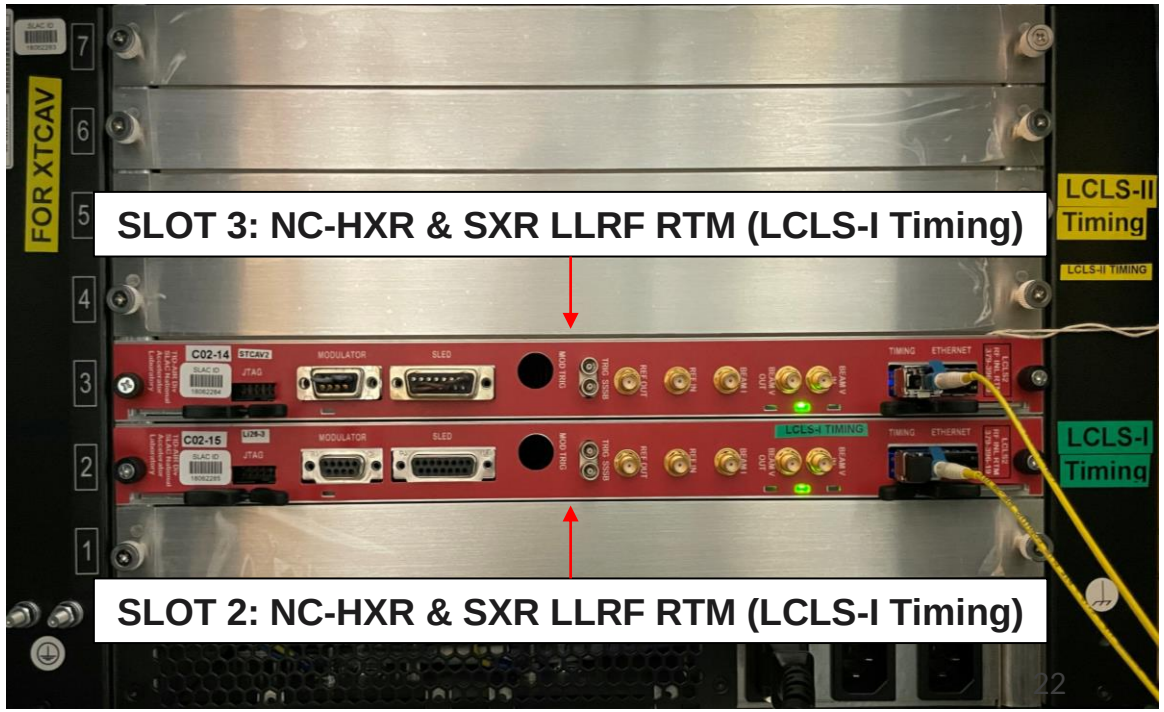
Supervisory Controller CPU: CPU-B15-RF03

< Front >

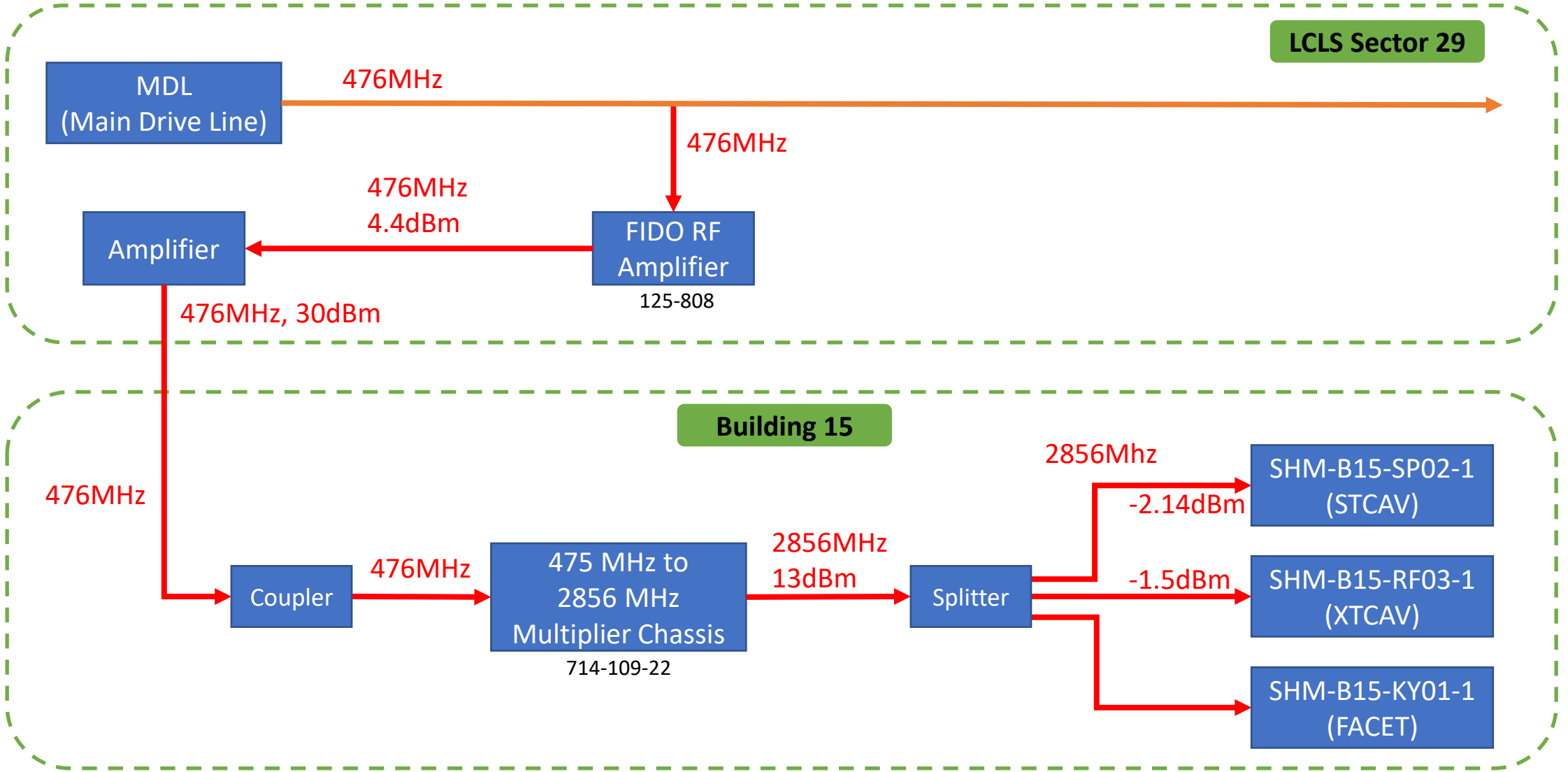
< Rear >

SHM-B15-RF03-1



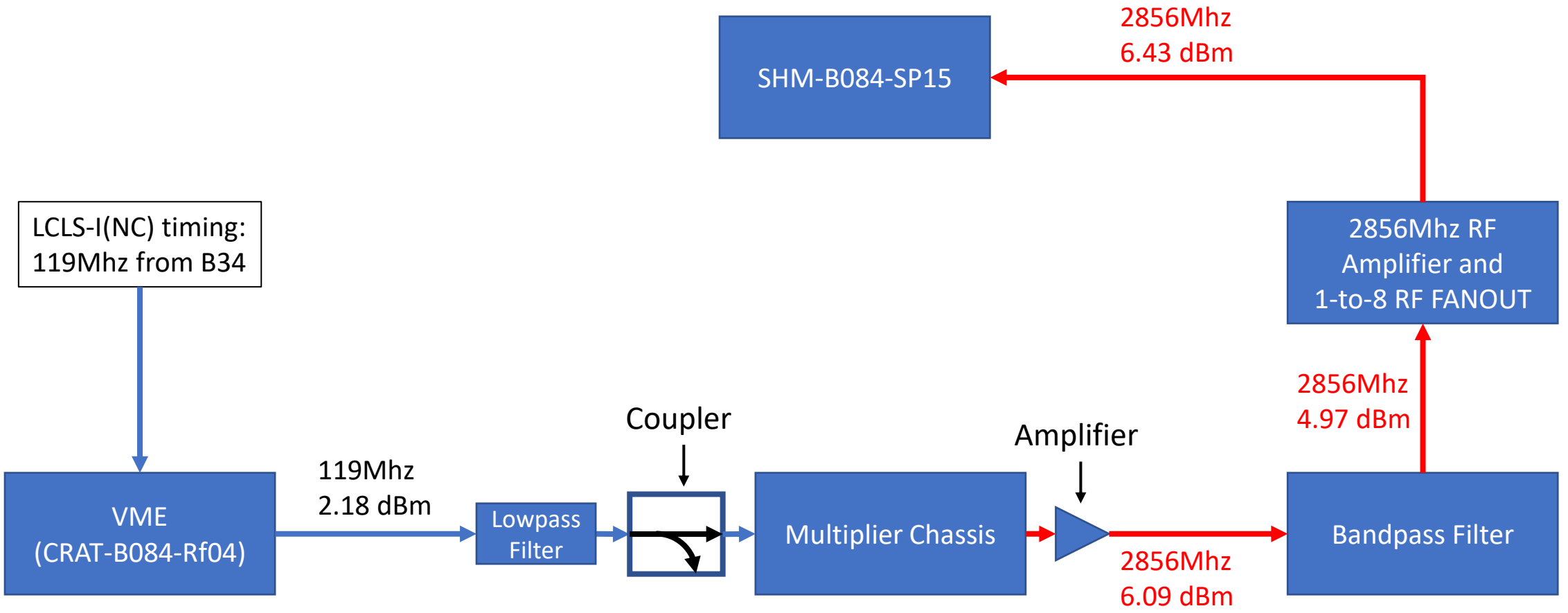


LCLS-I (NC) RF Reference Flow in B15



*Click each blue block to jump to more details

LCLS-I(NC) Timing Signal Flow in B84

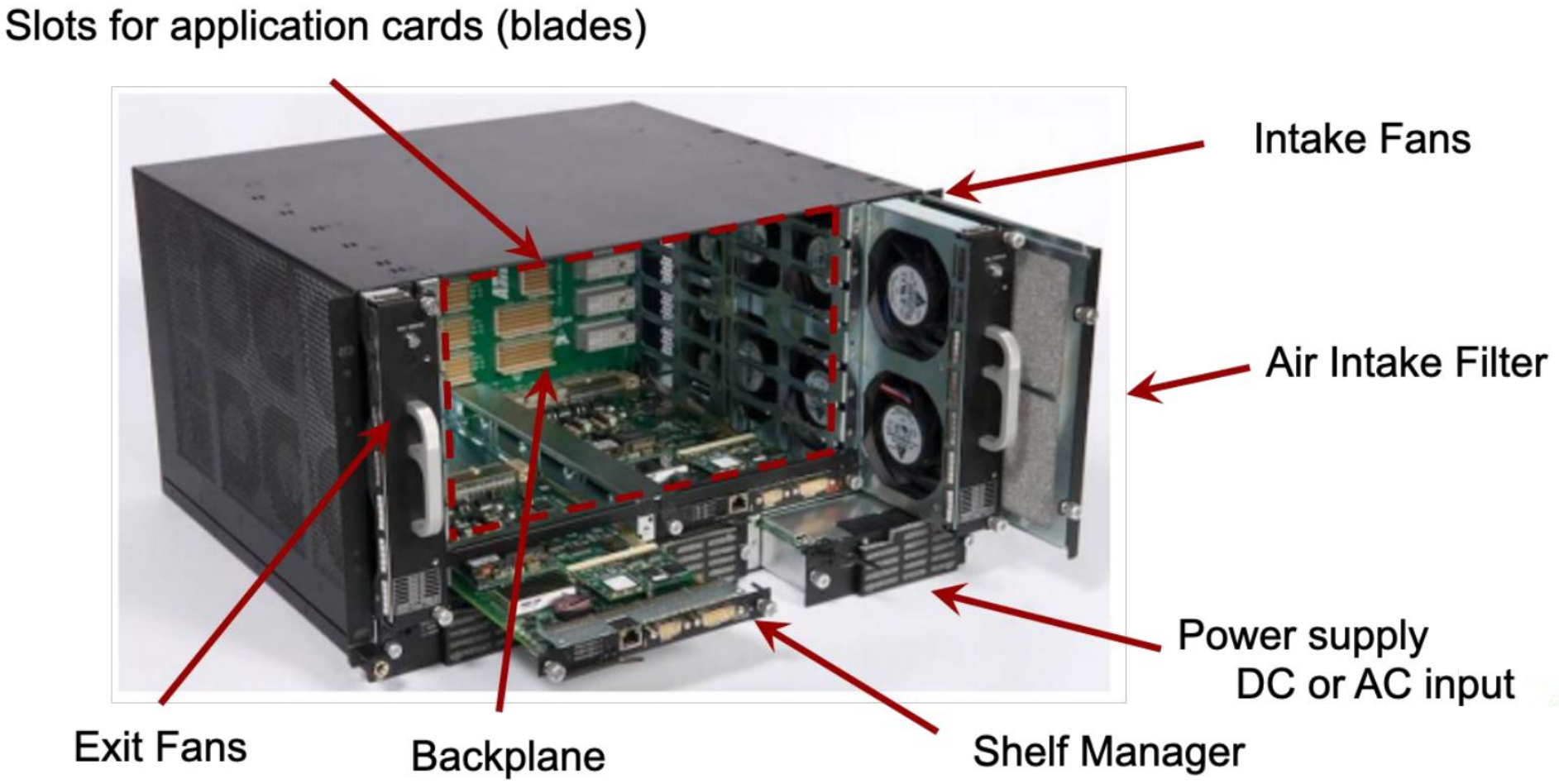


*Click each blue block to jump to more details

ATCA-based Control System Platform

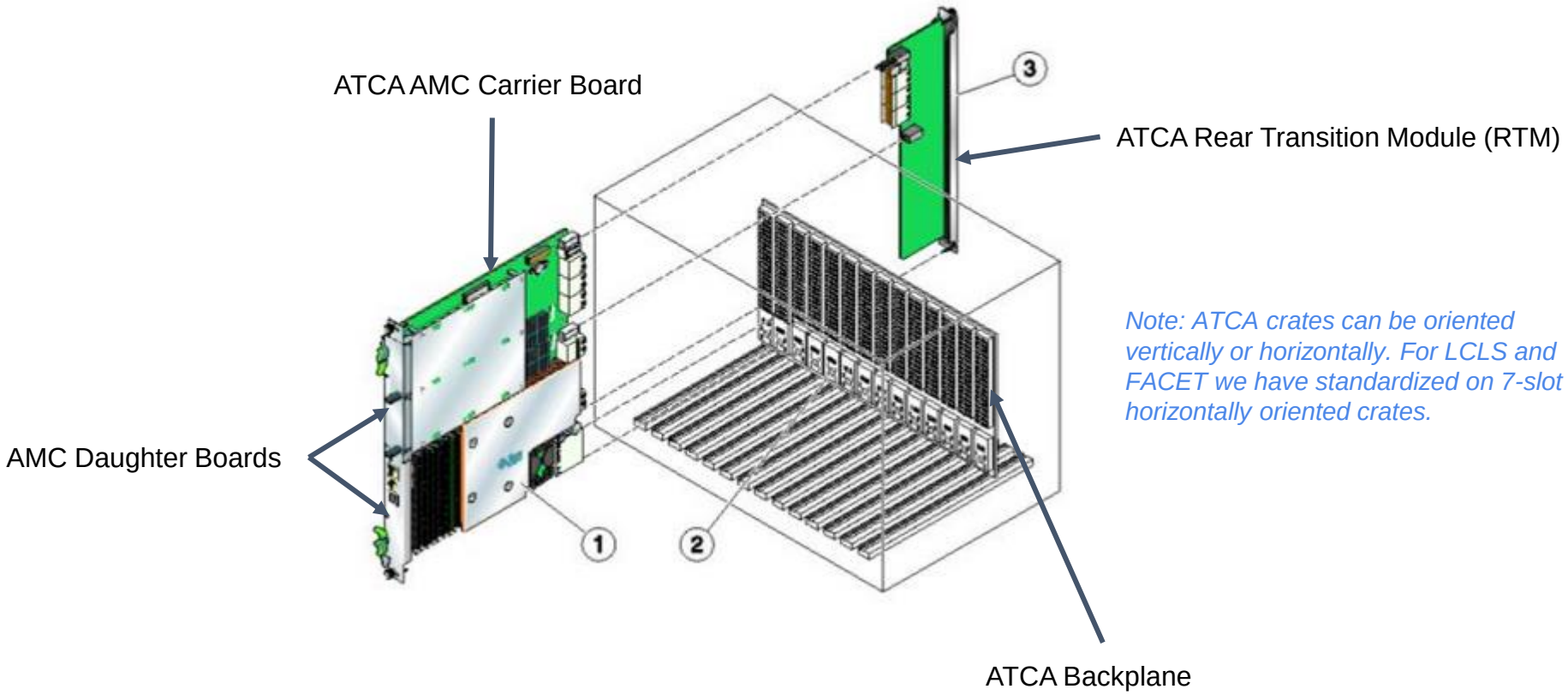
ATCA-based Control System Platform (1)

The Crate (aka -- Shelf)



ATCA-based Control System Platform (2)

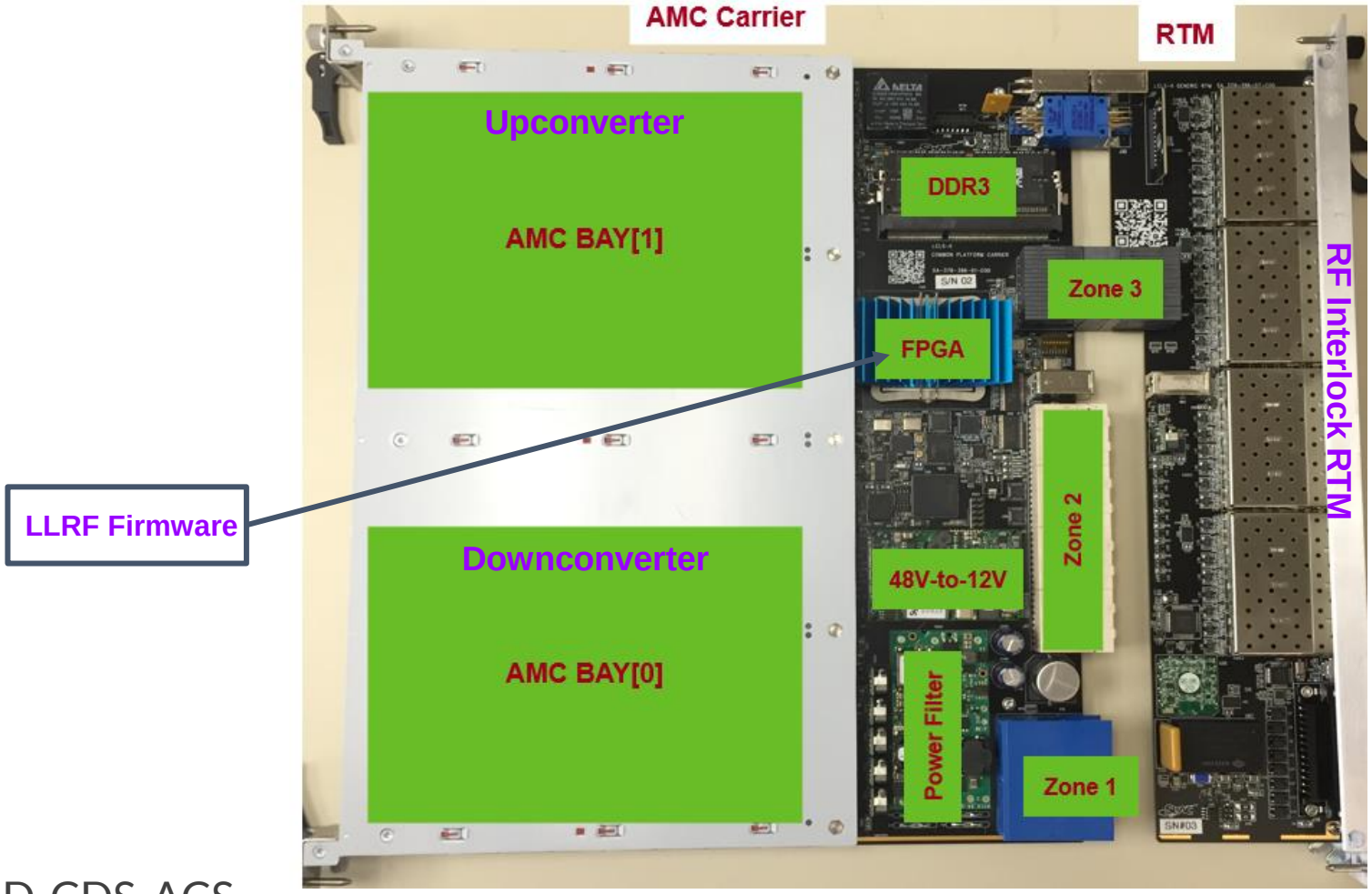
Application Card/Module components



Note: ATCA crates can be oriented vertically or horizontally. For LCLS and FACET we have standardized on 7-slot horizontally oriented crates.

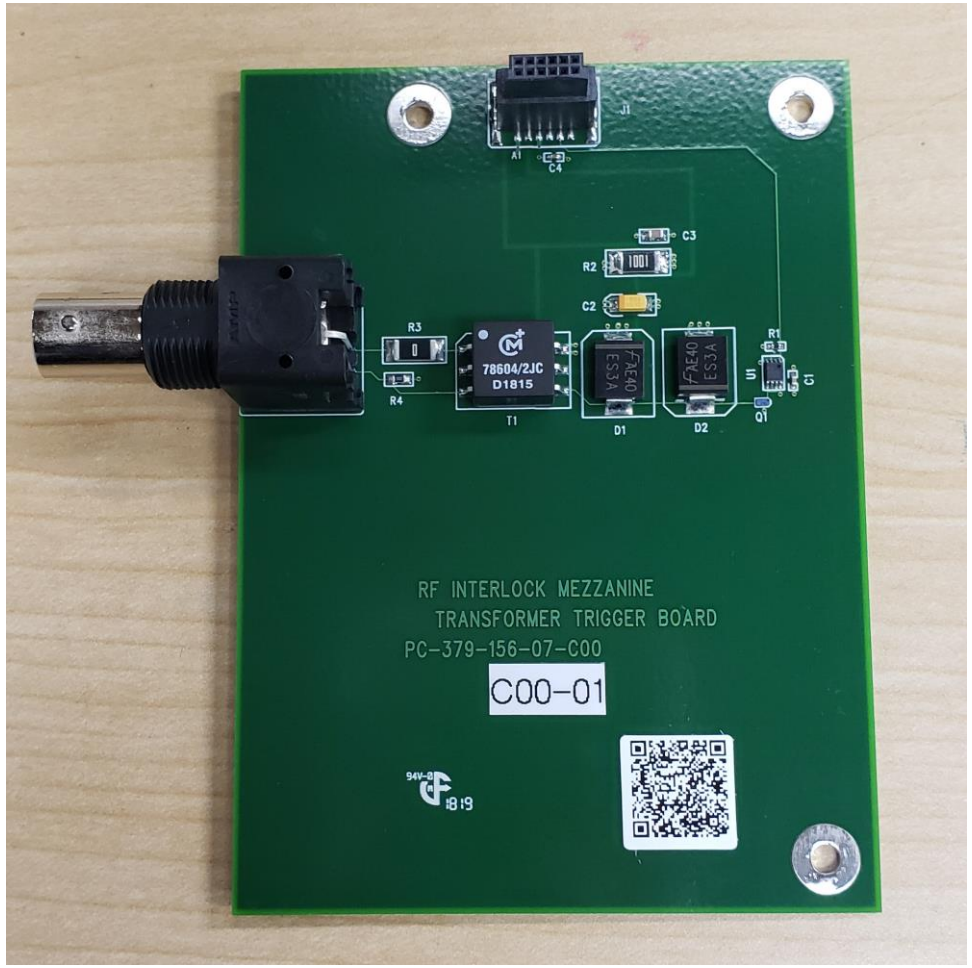
ATCA-based Control System Platform (3)

LLRF Application Card = AMC Carrier + AMCs + RTM



ATCA-based Control System Platform (4)

RF Interlock Transformer Trigger Daughter Board



ATCA-based Control System Platform

Front Panel + Connector Interface to the outside world

Downconverter AMC (PC_379_396_16_C03_A01)

Upconverter AMC (PC_379_156_06_C00_A01)

RF Interlock RTM (PC_379_396_19_C02)

ATCA board part numbers for LLRF Application (1)

- **AMC Carrier Board**, Product Part Number: **PC_379_396_01_C06_A00**

  Xilinx Kintex KU040 – 371 MHz Timing

  Ref: https://confluence.slac.stanford.edu/display/AIRTRACK/PC_379_396_01_C06

  Note: When ordering new boards use: PC_379_396_01_C09_A00

- **Downconverter AMC**, Product Part Number: **PC_379_396_16_C03_A01**

  LLRF: AMC Precision ADC Card Version C03_A01 ***(2856 MHz LO)***

  Ref: https://confluence.slac.stanford.edu/display/AIRTRACK/PC_379_396_16_C03

- **Upconverter AMC**, Product Part Number: **PC_379_156_06_C00_A01**

  LLRF GEN2 Upconverter Version C00_A01, w/interlocks **(2856 MHz LO)**

  Ref: https://confluence.slac.stanford.edu/display/AIRTRACK/PC_379_156_06_C00

- **RF Interlock RTM**, Product Part Number: **PC_379_396_19_C02**

  Interfaces to High Power RF (HPRF) System

  Modulator – RF Amplifier – Klystron

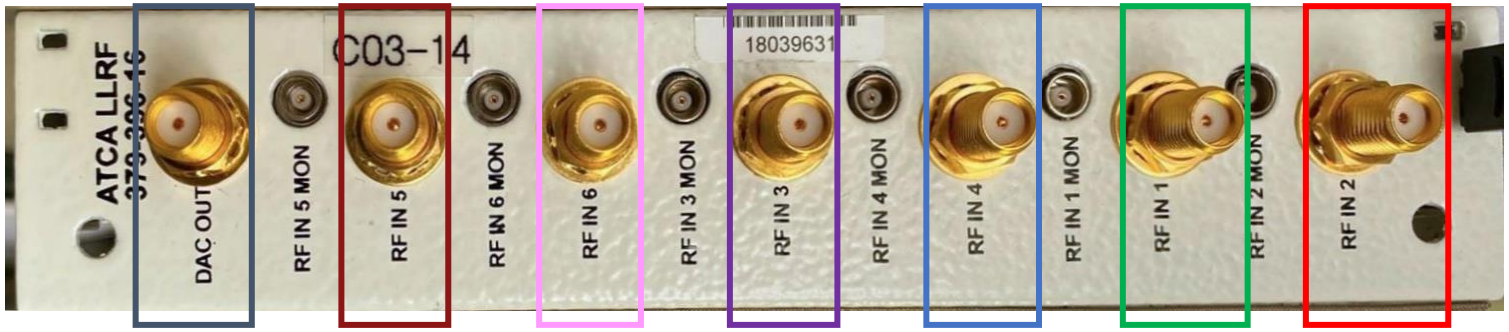
  Ref: https://confluence.slac.stanford.edu/display/AIRTRACK/PC_379_396_19_C02

ATCA board part numbers for LLRF Application (2)

- **RF Interlock Transformer Trigger Daughter Board (RTM daughter board or RTM trigger board)**, Product Part Number: **PC_379_156_07_C00**
  Ref: https://confluence.slac.stanford.edu/display/AIRTRACK/PC_379_156_07_C00

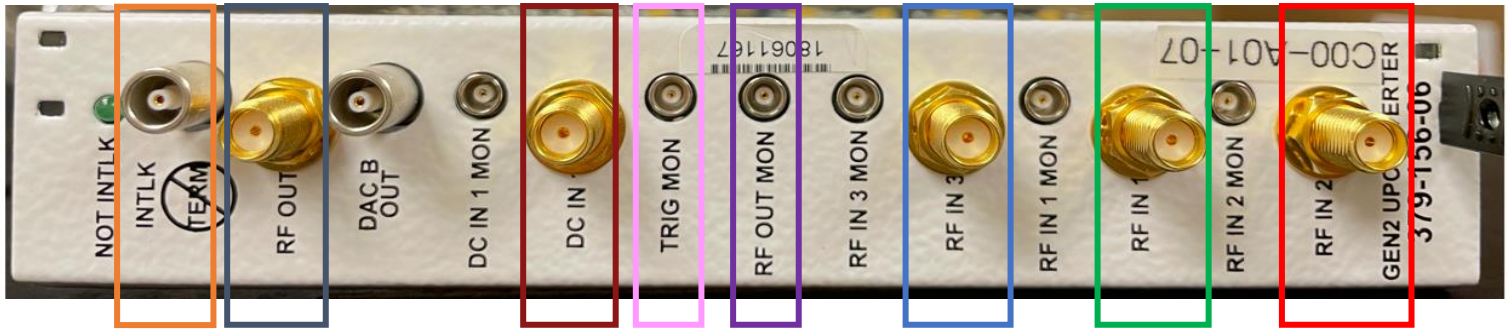
Front Panel Inputs Mapping

Downconverter AMC (PC_379_396_16_C03_A01)



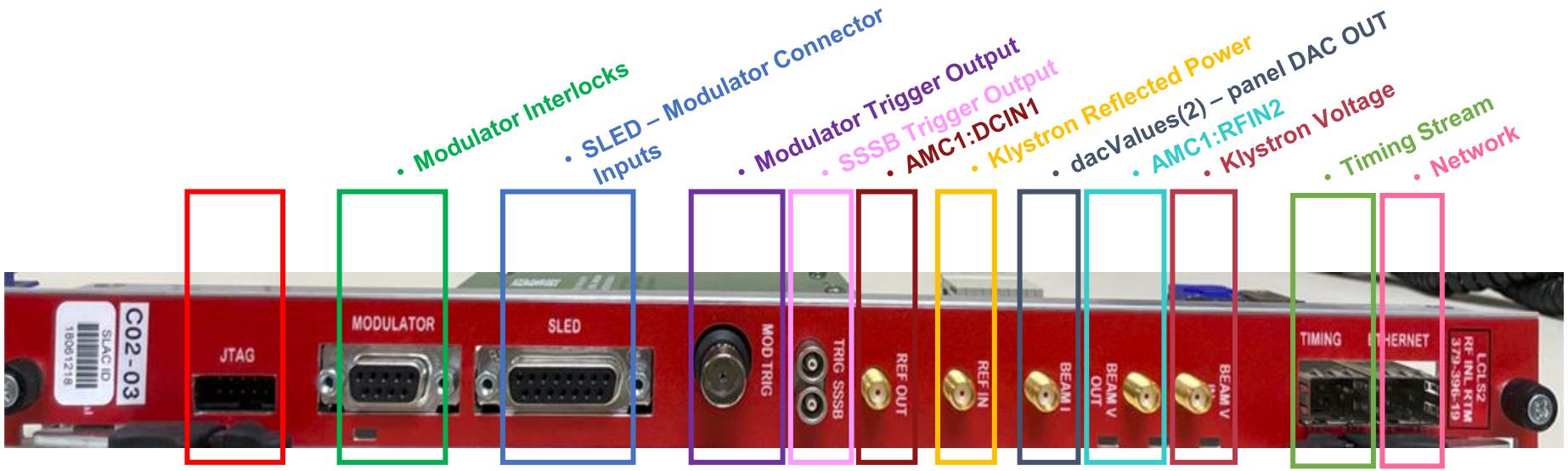
- dacValues(2) – panel DAC OUT
- adcValues(5) – panel RF IN 5
- adcValues(4) – panel RF IN 6
- adcValues(3) – panel RF IN 3
- adcValues(2) – panel RF IN 4
- adcValues(1) – panel RF IN 1
- adcValues(0) – panel RF IN 2

Upconverter AMC (PC_379_156_06_C00_A01)



- Interlock the DAC output – IN TLK
- dacValues(0) – panel RF OUT
- adcValues(5) – panel DC IN 1
- adcValues(4) – panel TRIG MON
- adcValues(3) – panel RF OUT MON
- adcValues(2) – panel RF IN 3
- adcValues(1) – panel RF IN 1
- adcValues(0) – panel RF IN 2

RTM Panel Inputs

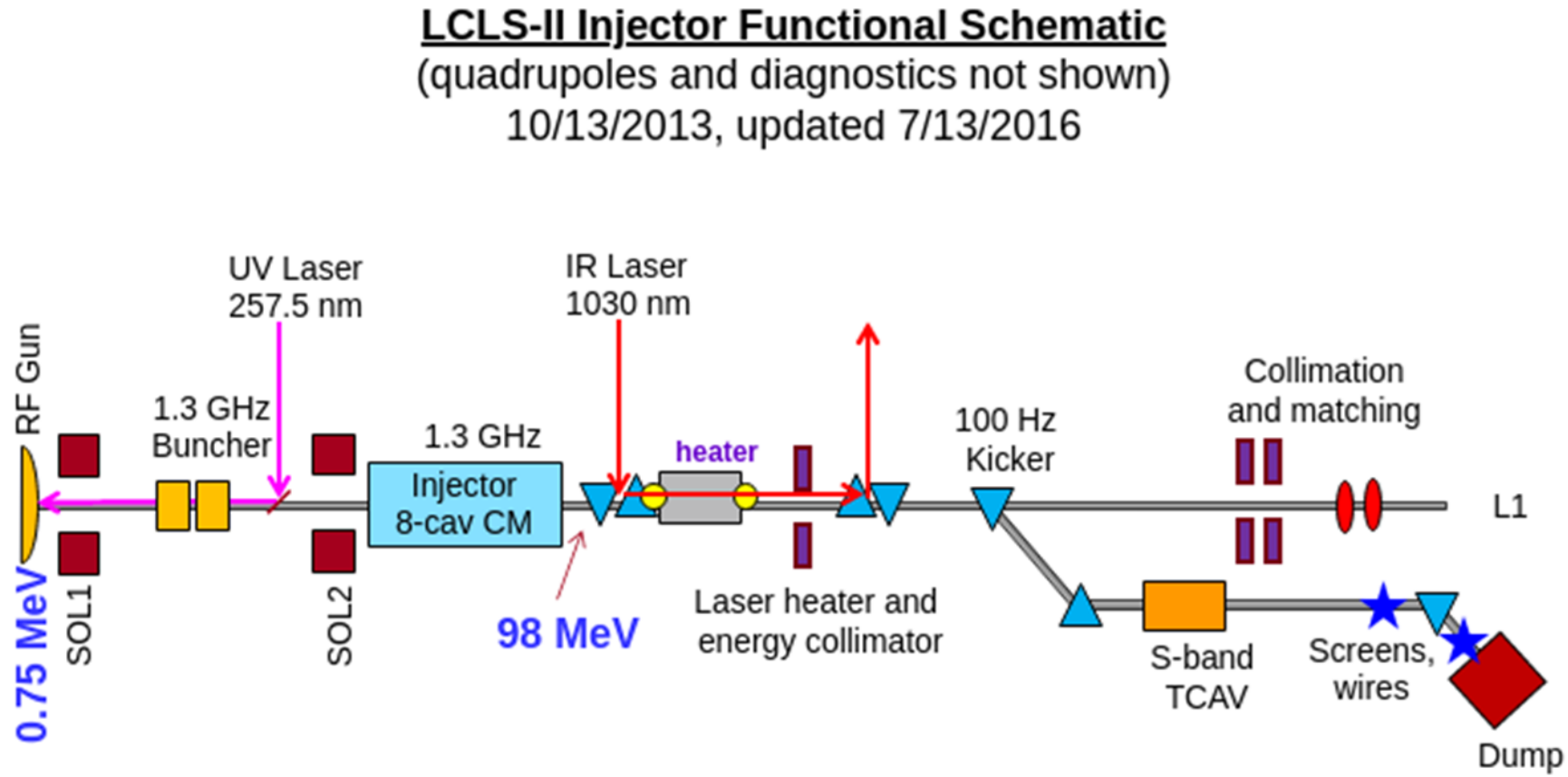


RF Interlock RTM (PC_379_396_19_C02)

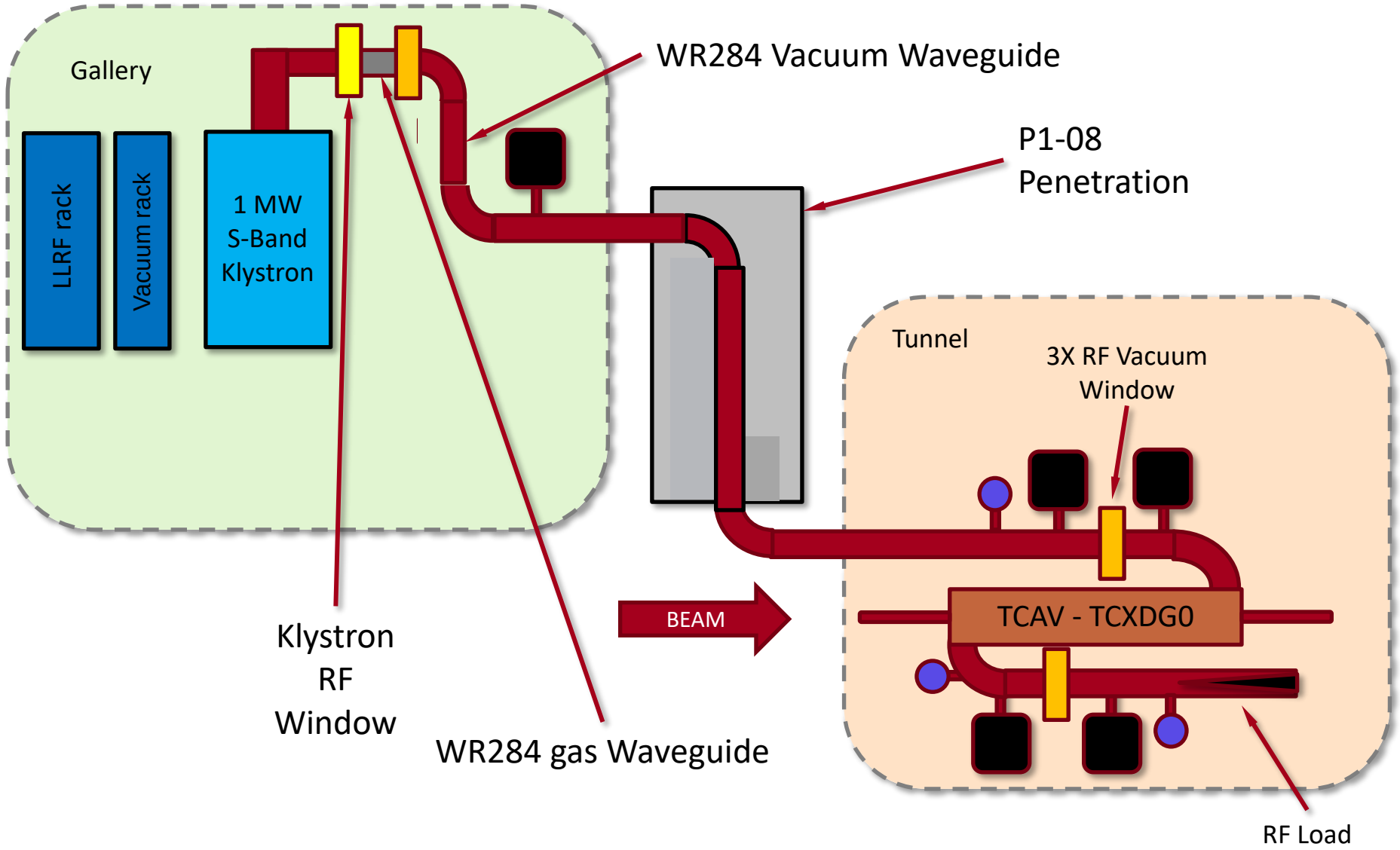
2

STCAV

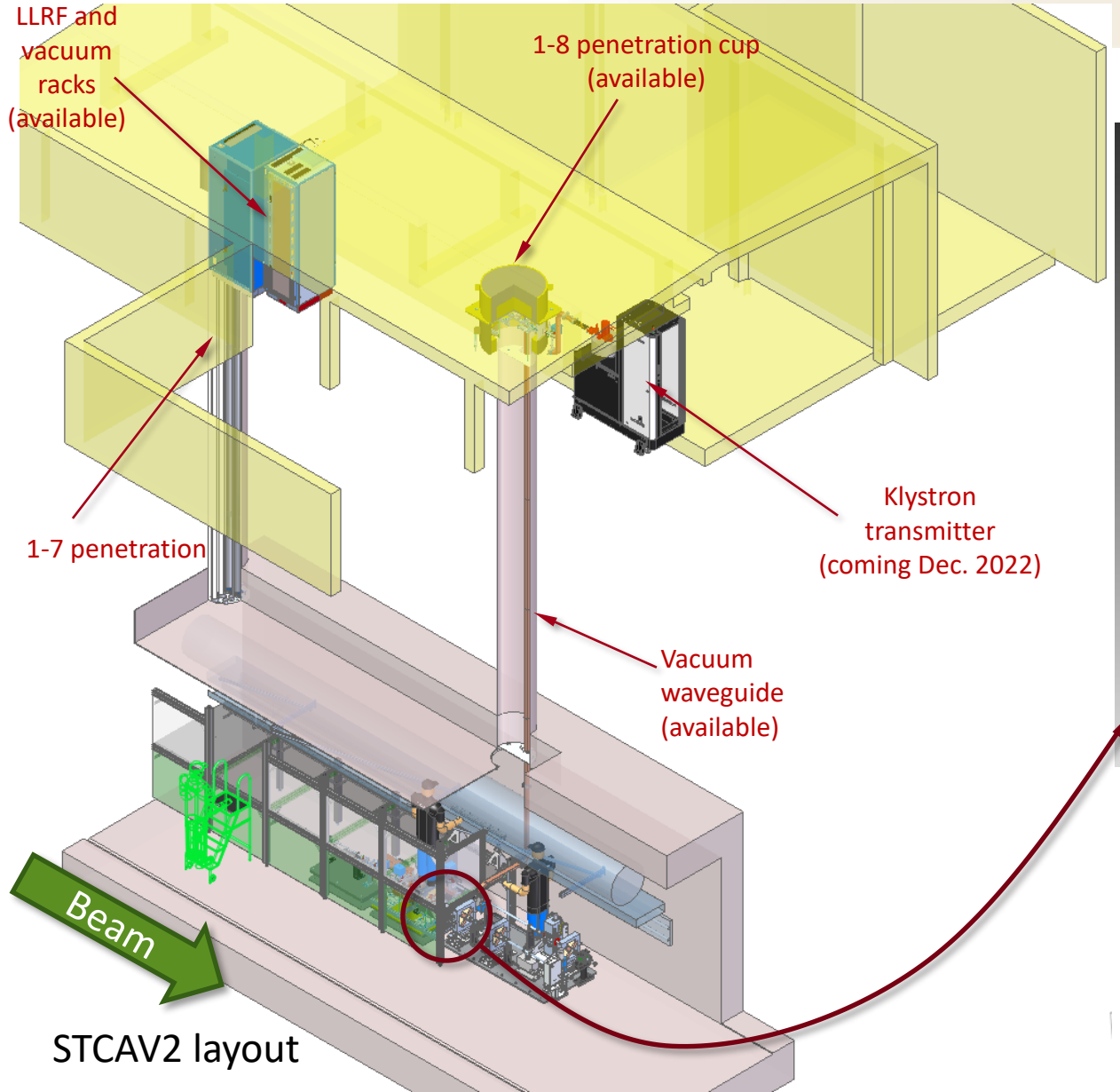
LCLS-II Injector Beamline



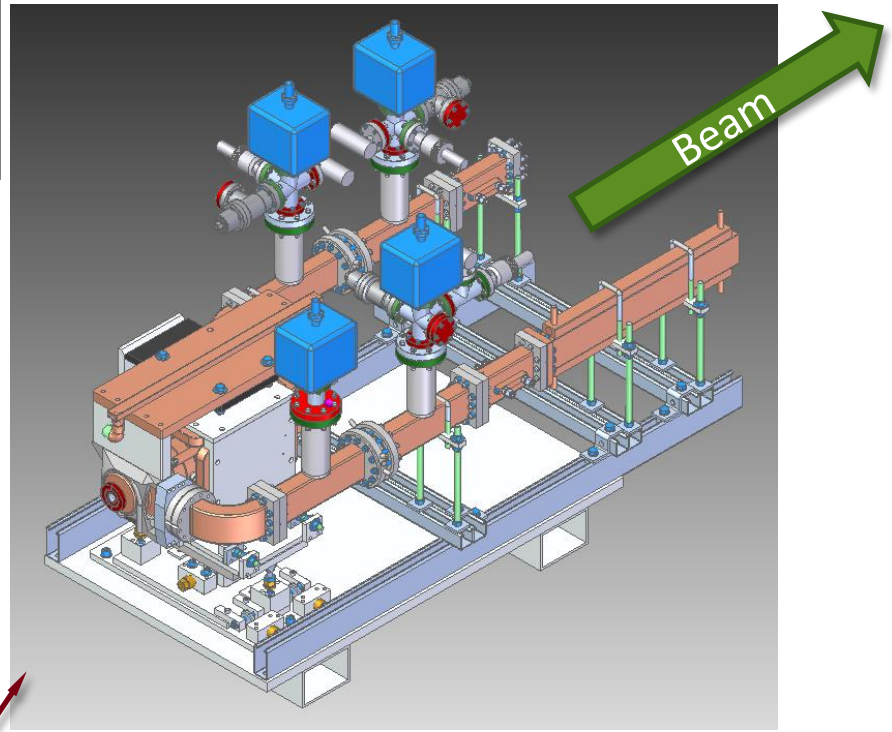
S-band **T**ransverse deflecting **CAV**ity **2** feet **(STCAV2)** System Overview



STCAV2 system layout



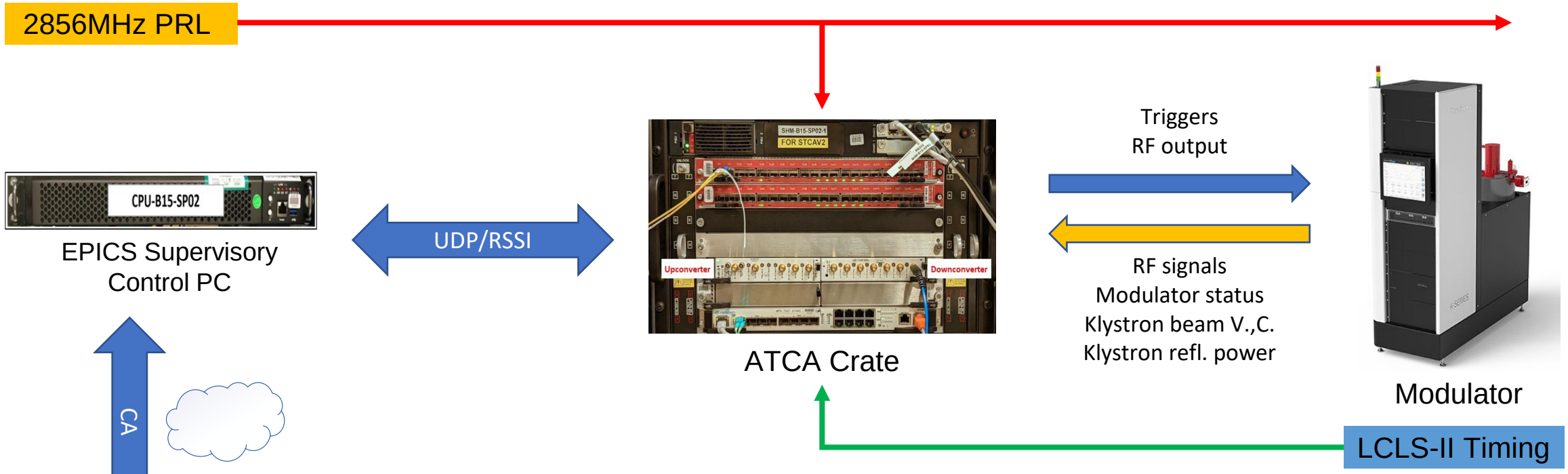
STCAV2 layout



Cavity module is in manufacturing

LLRF System Design

LLRF Control System Design Overview



- We have 2856MHz PRL like we have for FACET
- Unlike FACET, 2856 MHz reference will be locked to LCLS-I and LCLS-II Linac
- LLRF Algorithm tweaks for STCAV2 Frequency offset
- ATCA LLRF platform sends trigger and RF output signals to modulator
- Modulator sends RF signals, modulator status, Klystron beam voltage, current, and reflected power to ATCA crate
- ATCA crate connects to the IOC through UDP

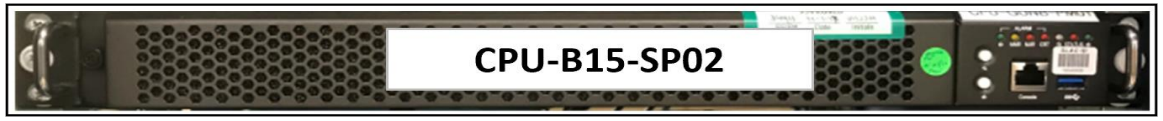
SLAC

ATCA-based Control System Platform -Test Stand for the STCAV2 LLRF Control system in B15

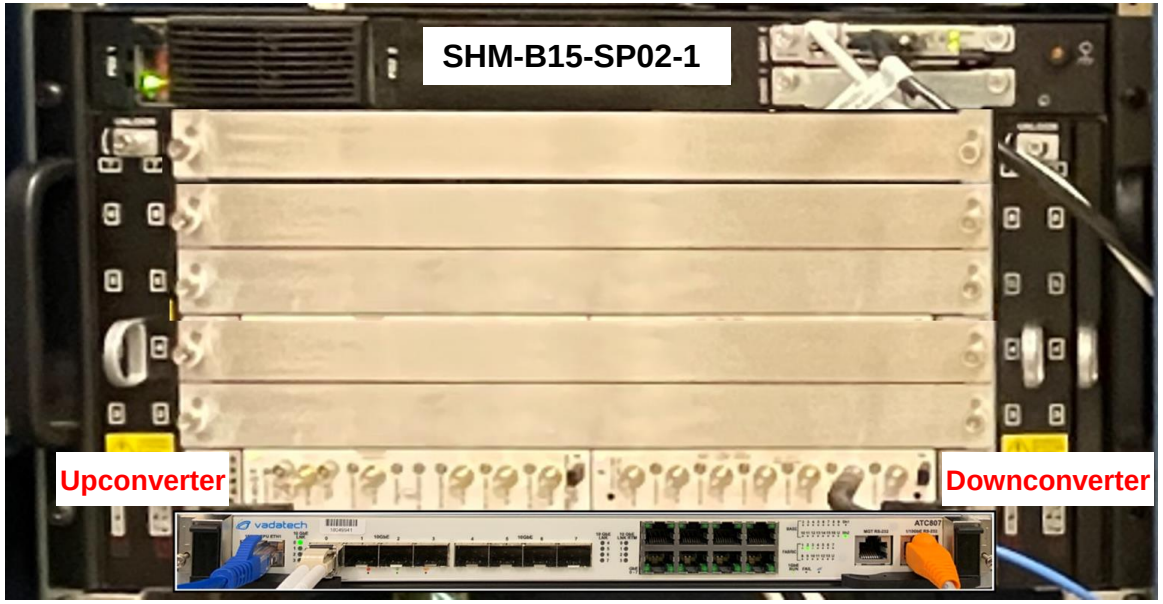
Shelf Manager: SHM-B15-SP02-1

Supervisory Controller CPU: CPU-B15-SP02

< Front >



< Rear >



ATCA-based Control System Platform

Front Panel + Connector Interface to the outside world

Downconverter AMC0 (PC_379_396_16_C03_A01)

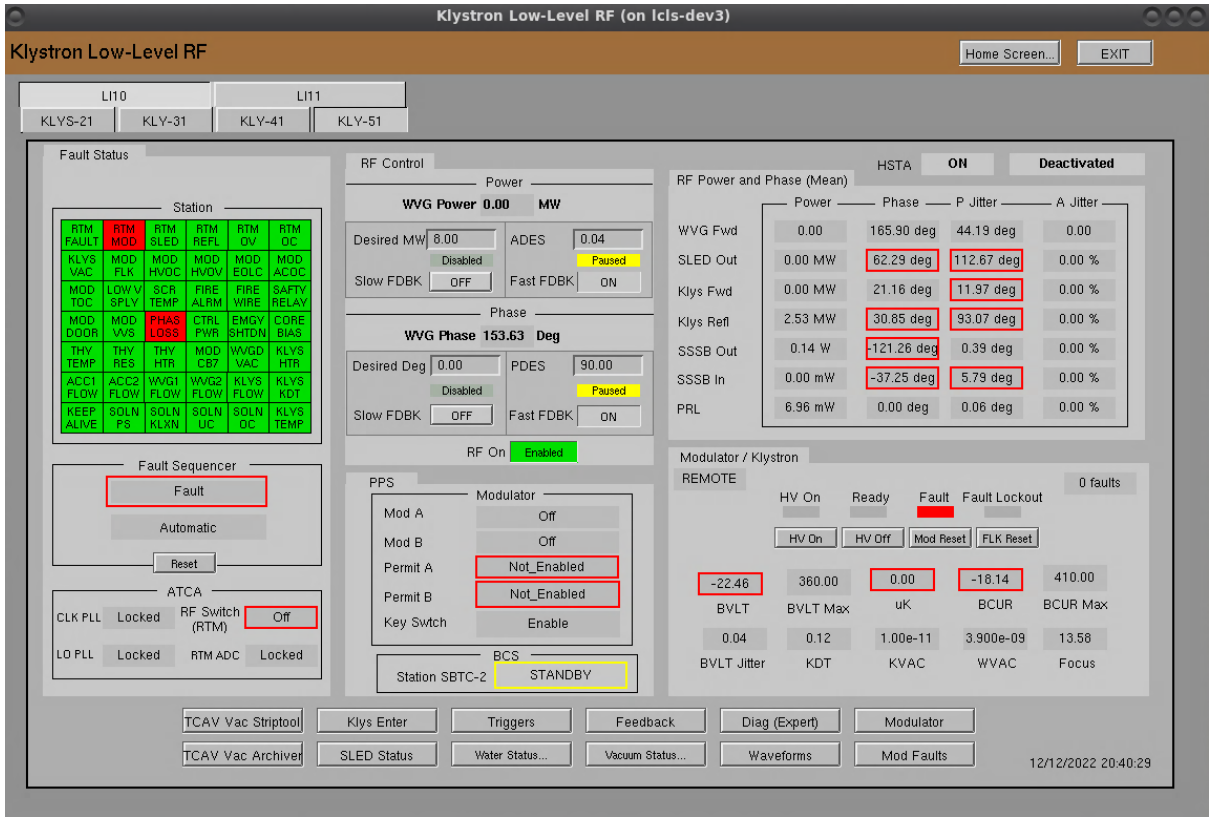
Upconverter AMC1 (PC_379_156_06_C00_A01)

RF Interlock RTM (PC_379_396_19_C02)

LLRF Controls System Design - GUI

< GUI from SC RF >

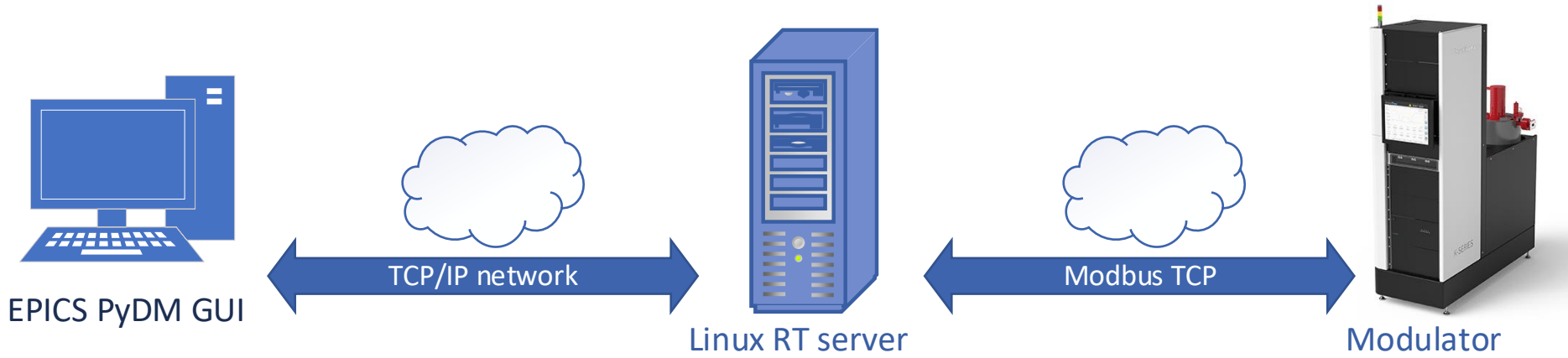
< GUI from FACET >



- GUI from FACET and LCLS-II
- GUI will be based on them and update according to actual PVs and user request
- We will follow PV naming convention and check with naming czars
- PV naming convention: Device name – **DeviceType : Area : Position,** PV name – **DeviceType : Area : Position : Attribute**
  ex) ACCL:L0B:0110:PACTMEAN, ACCL:L0B:0110:SSA:RefPwr, TCAV:DIAG0:xxx:xxx

HPRF System Design

HPRF Control System Design Overview



- Modulator exposes a modbus TCP interface for knobs, buttons, statuses
- Modulator contains a control system app (touchscreen/mouse/keyboard) – but no PVs
- EPICS IOC app runs on Linux RT, uses the modbus module - PVs
- EPICS GUI accesses PVs exported by EPICS app

Modbus registers

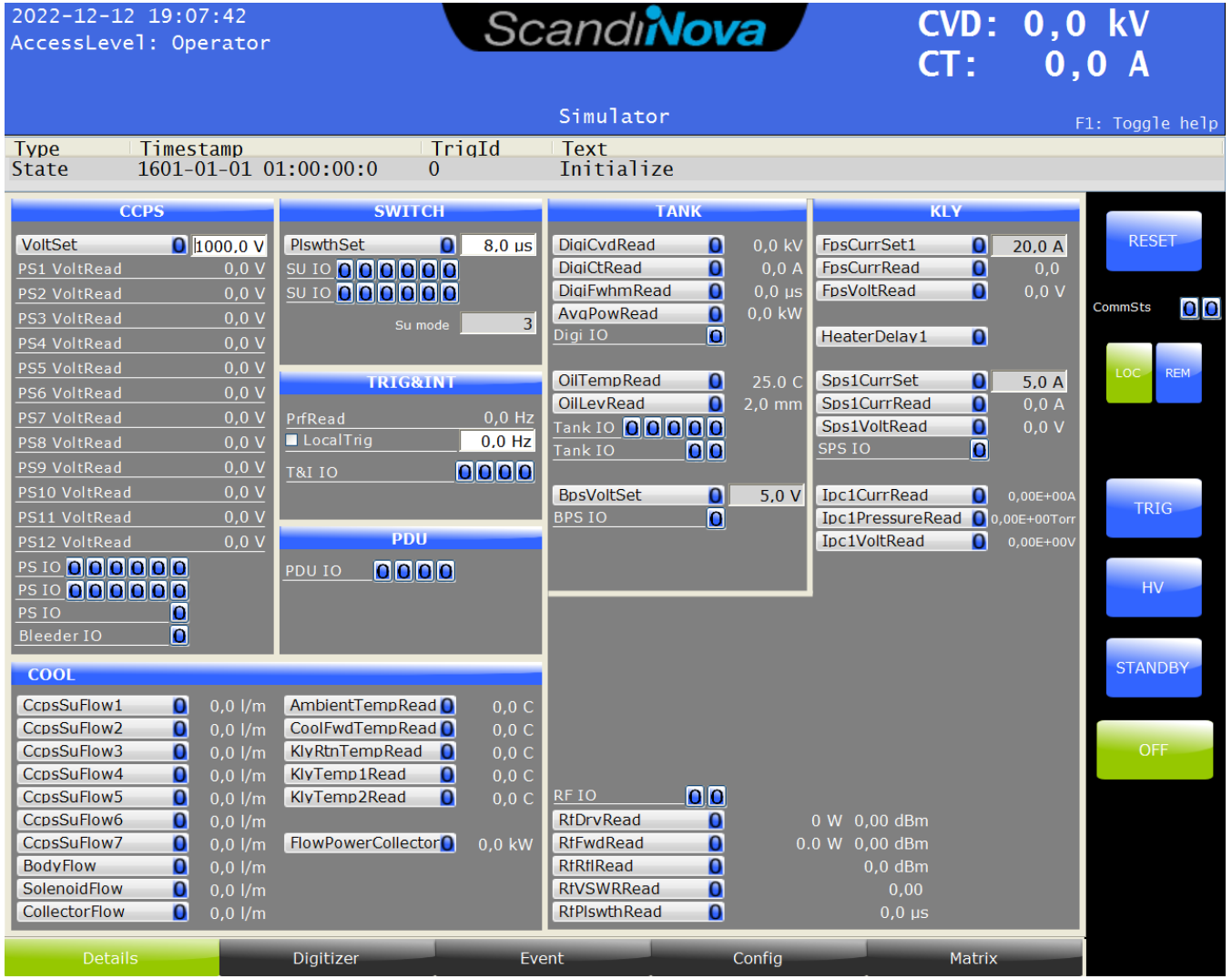
- ~100 registers exposed
- Many of them are temperatures, rates, statuses
- 50 events (state changes, interlocks), but the IOC app saves all events to a file
- State change requests, resets
- Set voltages and currents

< Example register map from ScandiNova >

address	type	input/output	description
0	int16	output	protocol ID
1	int16	output	protocol rev
2	uint16	ouput	watchdog
3	int16	output	modulator state
4	uint16	output	modulator status
5	int16	output	access level
6	float	output	warm-up timer
8	float	output	pulse rep freq
20	int	output	modulator target state
21	float	output	CCPS voltage
25	float	output	pulse width
800	float	output	water flow rate
999	int16	output	event log index
1715	struct	output	first interlock event
0	uint16	input	watchdog
1	int16	input	modulator state
2	uint16	input	command bits (reset)
100	float	input	CCPS voltage
300	float	input	pulse width

HPRF Controls System Design - GUI

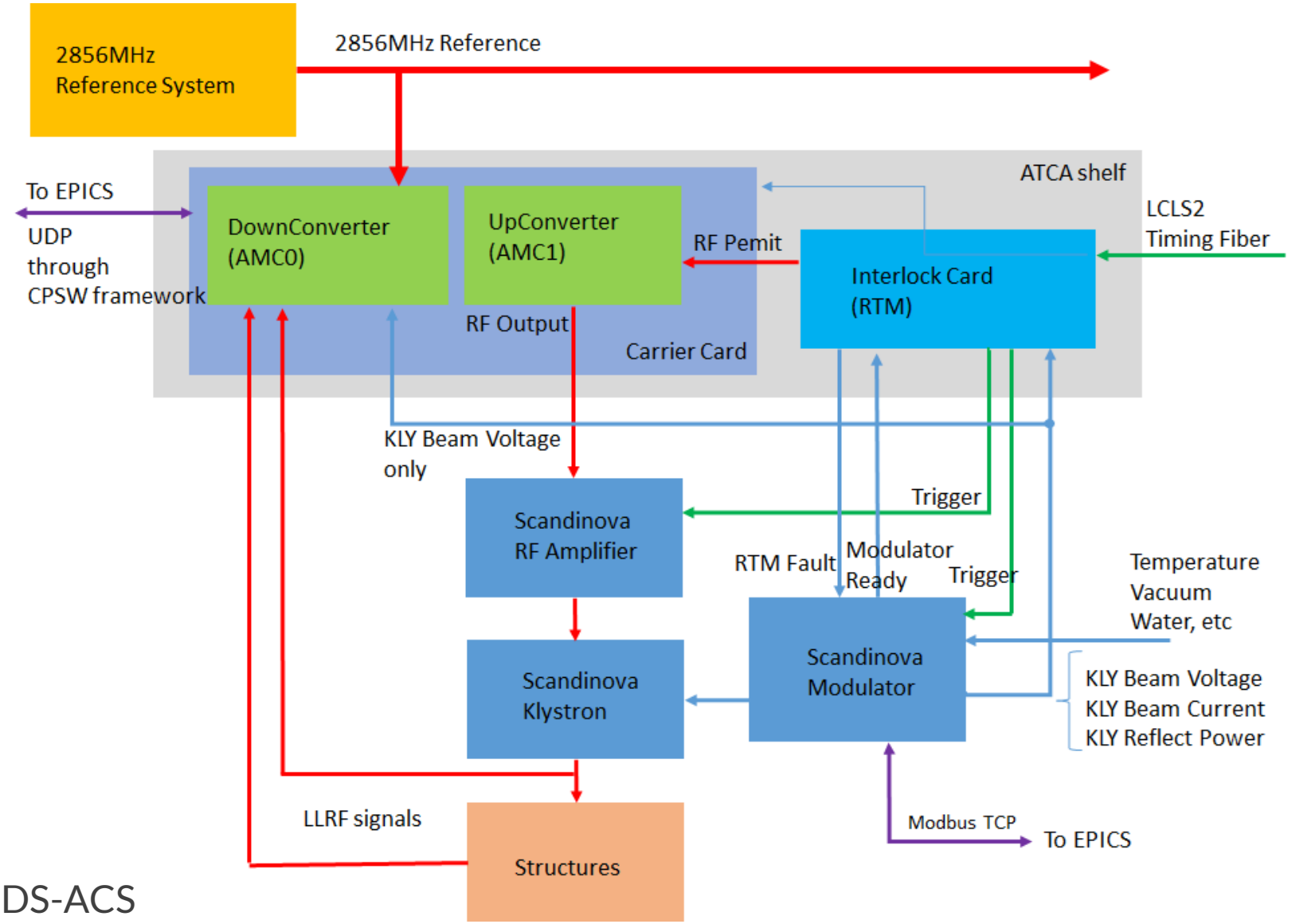
- Simulator provided by ScandiNova
- Actual GUI will be as close as possible with this
- We are working with operators and engineers to provide appropriate user interfaces and full IOC integration
  - Joe wants the GUI exposes the same functionality as the GUI that comes with the ScandiNova cabinet.
- UED and Berkeley already have the ScandiNova modulator, and we will keep GUI as close as possible with our collaborator



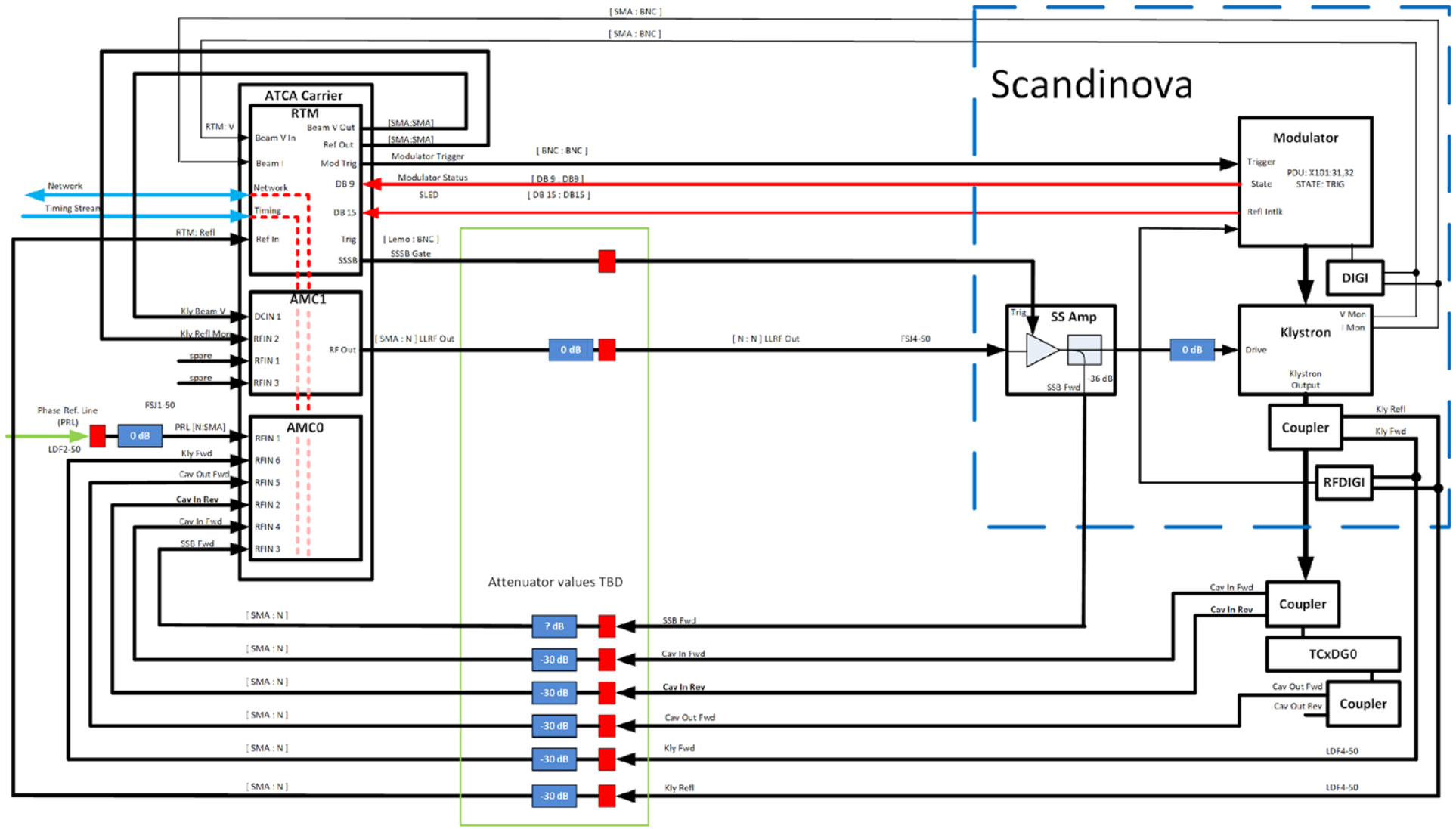
Documents from ScandiNova

- Control Systems Manual: https://slac.sharepoint.com/:b:/r/sites/lcls/lcls-2/as/linac/Shared_docs/TCXDG0/modulator/Scandinova/controls%20documents/new_17Nov2022/FOL-00500_rev_00/DOC-014478-04_KSERIES%20ScandiCAT%20control%20system%20manual.pdf?csf=1&web=1&e=Wh6UD6 –
- Modbus TCP Specification document : https://slac.sharepoint.com/:b:/r/sites/lcls/lcls-2/as/linac/Shared_docs/TCXDG0/modulator/Scandinova/controls%20documents/new_17Nov2022/FOL-00500_rev_00/Appendixes/DOC-000295-14%20ScandiCAT%20Generic%20ModbusTCP%20spec.pdf?csf=1&web=1&e=F2re4h –
- Software installation guide document: https://slac.sharepoint.com/:b:/r/sites/lcls/lcls-2/as/linac/Shared_docs/TCXDG0/modulator/Scandinova/controls%20documents/new_17Nov2022/FOL-00500_rev_00/Appendixes/DOC-007184_02%20ScandiCAT%20software%20installation%20instruction.pdf?csf=1&web=1&e=Dgxdrt -

Concept of STCAV2 RF control system

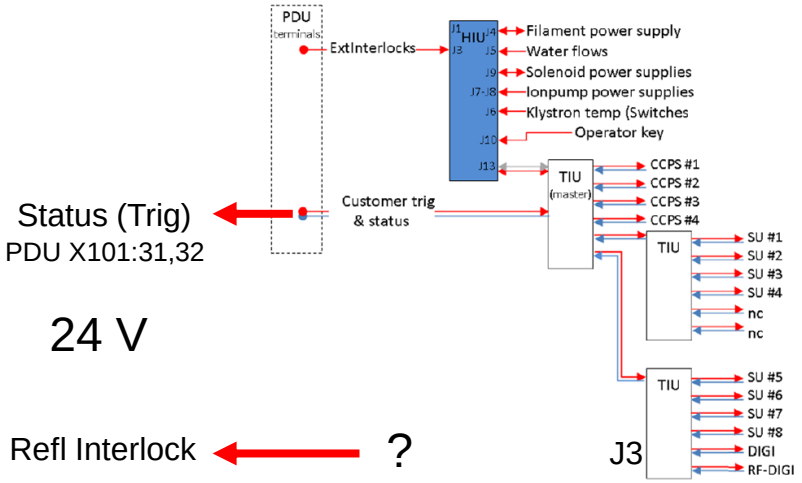


STCAV2 Interlocks (1)



STCAV2 Interlocks (2)

System: 014478-04



Conn	Name	Type	Function	Part number
J1:L	SumIntlk	SC duplex	Sum interlock, Light=No INTLK input is missing	HFBR-14E4Z
J1:R	TrigIn		Trigger input, Light=Trig	HFBR-24E2Z
J2	TrigIn	BNC	Trigger input, 5-10VDC=Trig, input impedance 50Ω	
J3:1	I/O	Dsub9F	24VDC, opto-coupler power from HIU	
J3:2			GND, opto-coupler ground from HIU	
J3:3			Input: HiuTrigEna	
J3:4			Input: SpiCs	
J3:5			Input: SpiClk	
J3:6			Input: SpiMosi	
J3:7			Output: SumIntlk	
J3:8			Output: SpiMiso	
J3:9			Output: HiuTrigOut, trig to HIU/PLC, a 82 us long pulse for every enabled trig.	

Source?
0 – 8 MHz?

FWD

REFL

REFL Intlk (TTL)
?

Conn	Name	Type	Function		
J1	RF FWD	SMA	Forward power	0-8MHz, max -5dBm, DNR >50dB	Analog Devices HMC713LP3E
J2	RF RFL	SMA	Reflected power		
J3	Trig in	SMA	TTL, Hi=Start digitizing. (not used)		
J4	INLK out	SMA	TTL, Hi=OK / Lo=Interlock, <100ns reaction speed		
J5	T&I	SC Duplex	Left	Trigger input	HFBR-24E2Z
			Right	Interlock return, Light=OK / Dark=Interlock	HFBR-14E4Z

RFDIGI: 014775-03

PDU “Status” will communicate Beam Voltage Interlock (Trig state).
How do we get the RF Reflected Power Interlock to the LLRF?

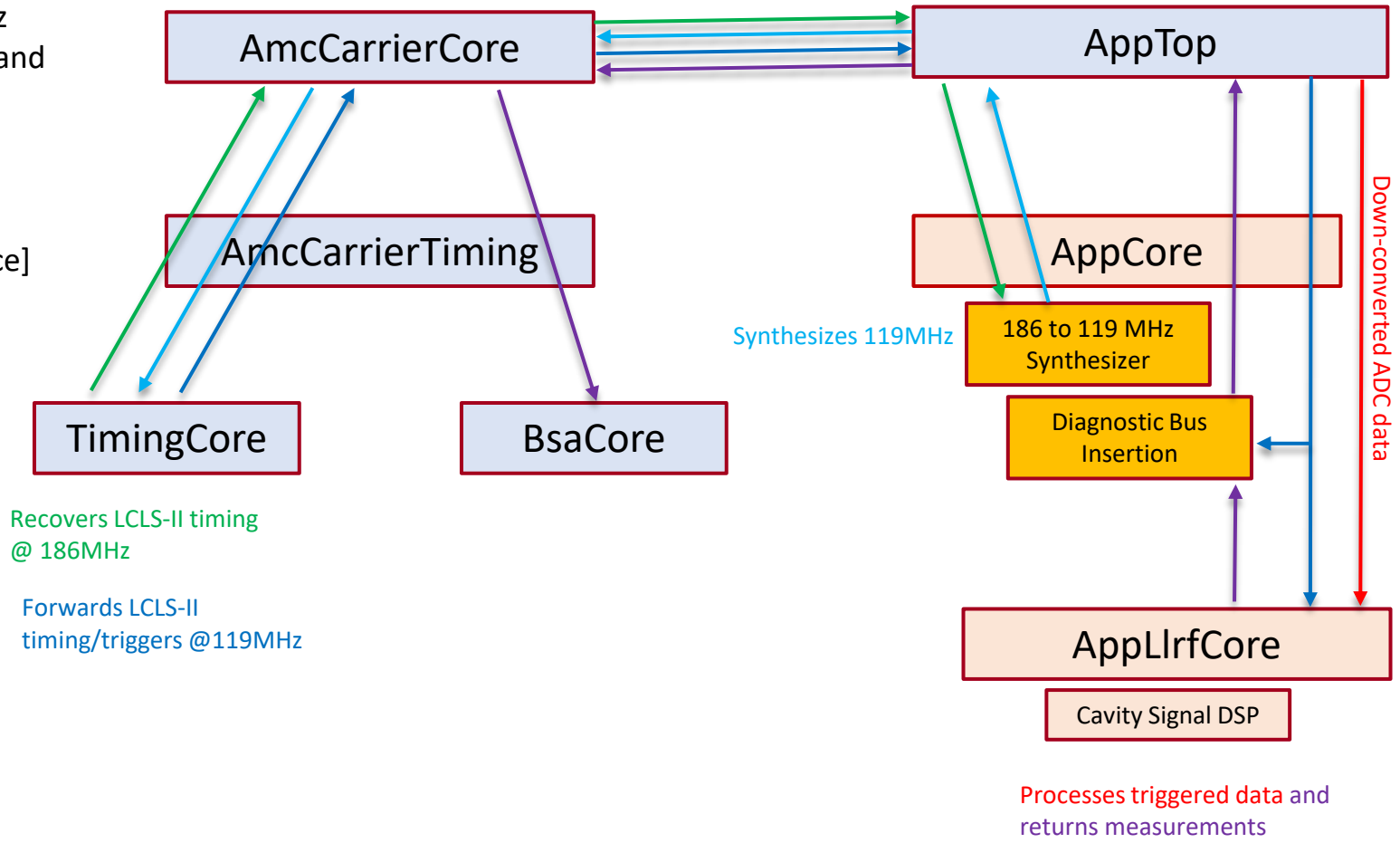
Functional Blocks of Firmware/Software

- Timing
  - Timing Core firmware listens timing stream from TPG (LCLS-II) and generates triggers and clocks for other parts of firmware
  - tprTrigger software module configures trigger and rate settings for The Timing Core, and monitor the status
- RFCommon
  - RFCommon firmware measures RF phase and amplitude and generates RF signal from the input of llrf_hls (baseband waveform and phase/amplitude)
  - RFCommon software module configure/monitors the RFCommon firmware (ex, Clock and PLL locking status, select input channels for LO,…)
- LLRF HLS
  - Llrf_hls firmware provides the following functions:
    - Get Phase/Amplitude measurements from RF Demod, and calculates Window Average, Channel Weight Average
    - Phase Reference Subtraction
    - Provides bunch by bunch feedback
    - Interfaces to the llrfHlsAsyn software module
  - LlrfHlsAsyn software module
    - Configures/Monitors the llrf_hls firmware status

Firmware Structural View

The new firmware functions for this application consist of gluing the 2856 MHz DSP modules with the core LCLS-II timing and diagnostics modules.

The clock domain crossing remains synchronous since the two sources [2856 MHz reference and LCLS-II timing reference] are locked.

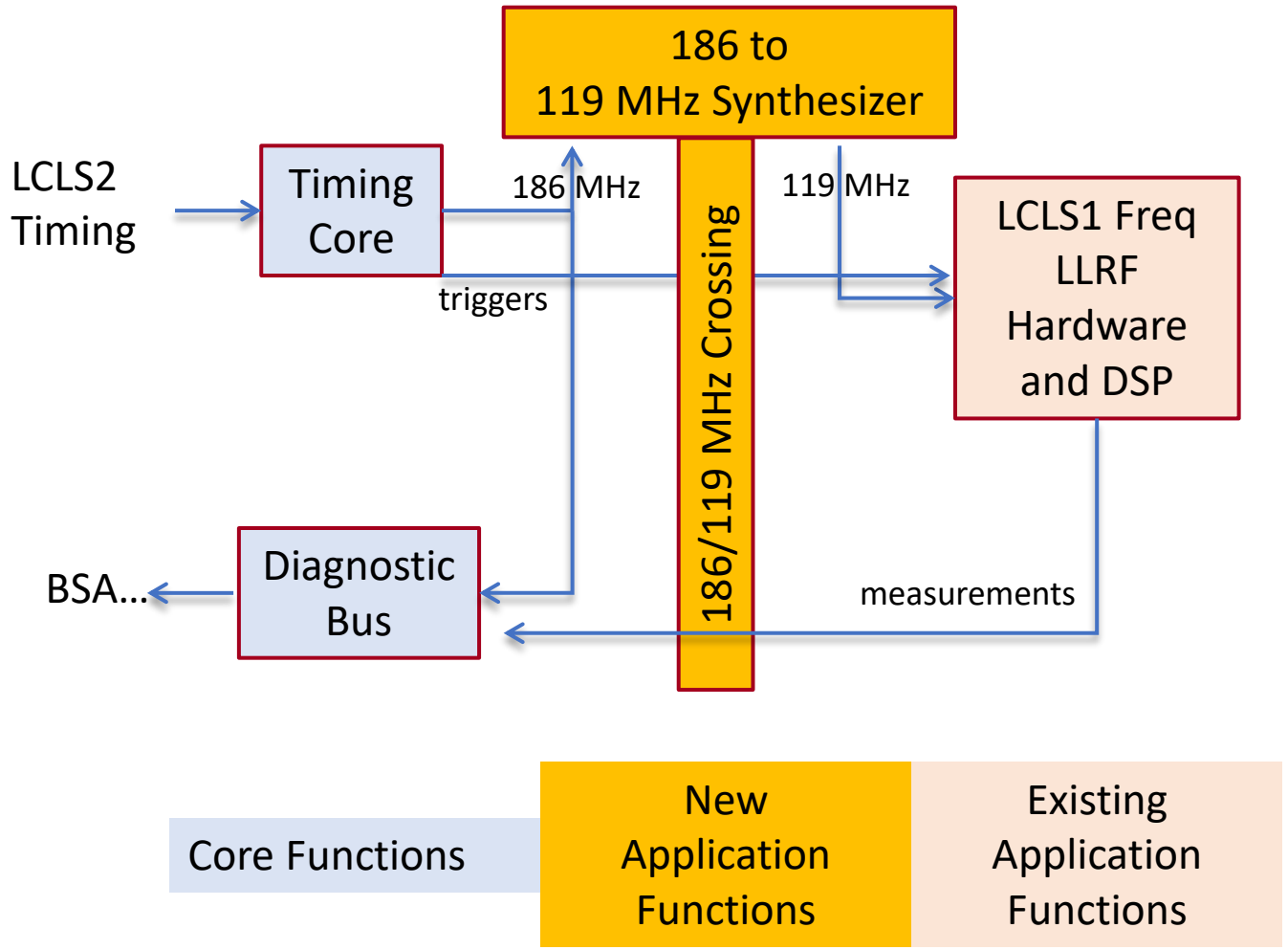


Implemented in git slaclab/llrf-hls project.

Firmware Functional View

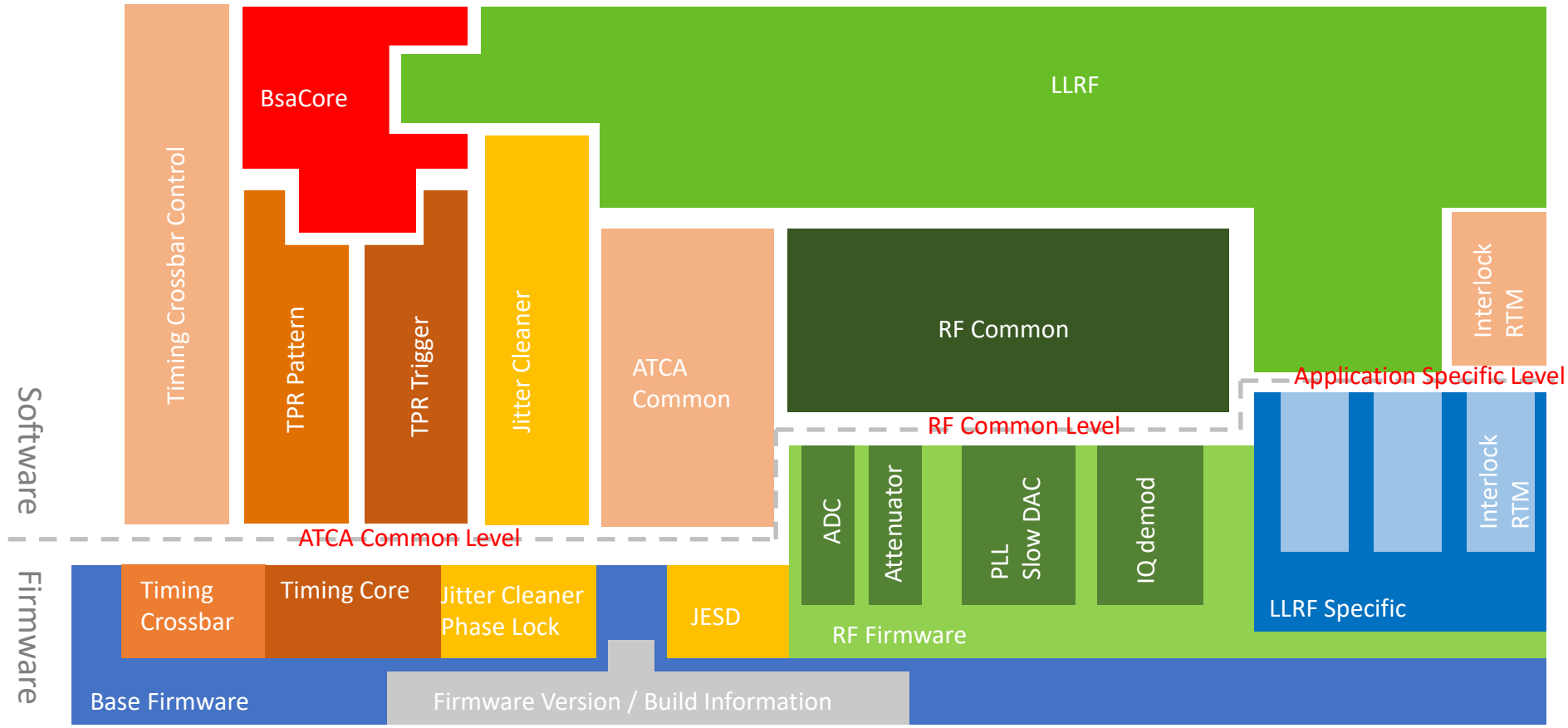
The new firmware functions for this application consist of gluing the 2856 MHz DSP modules with the core LCLS-II timing and diagnostics modules.

The clock domain crossing remains synchronous since the two sources [2856 MHz reference and LCLS-II timing reference] are locked.

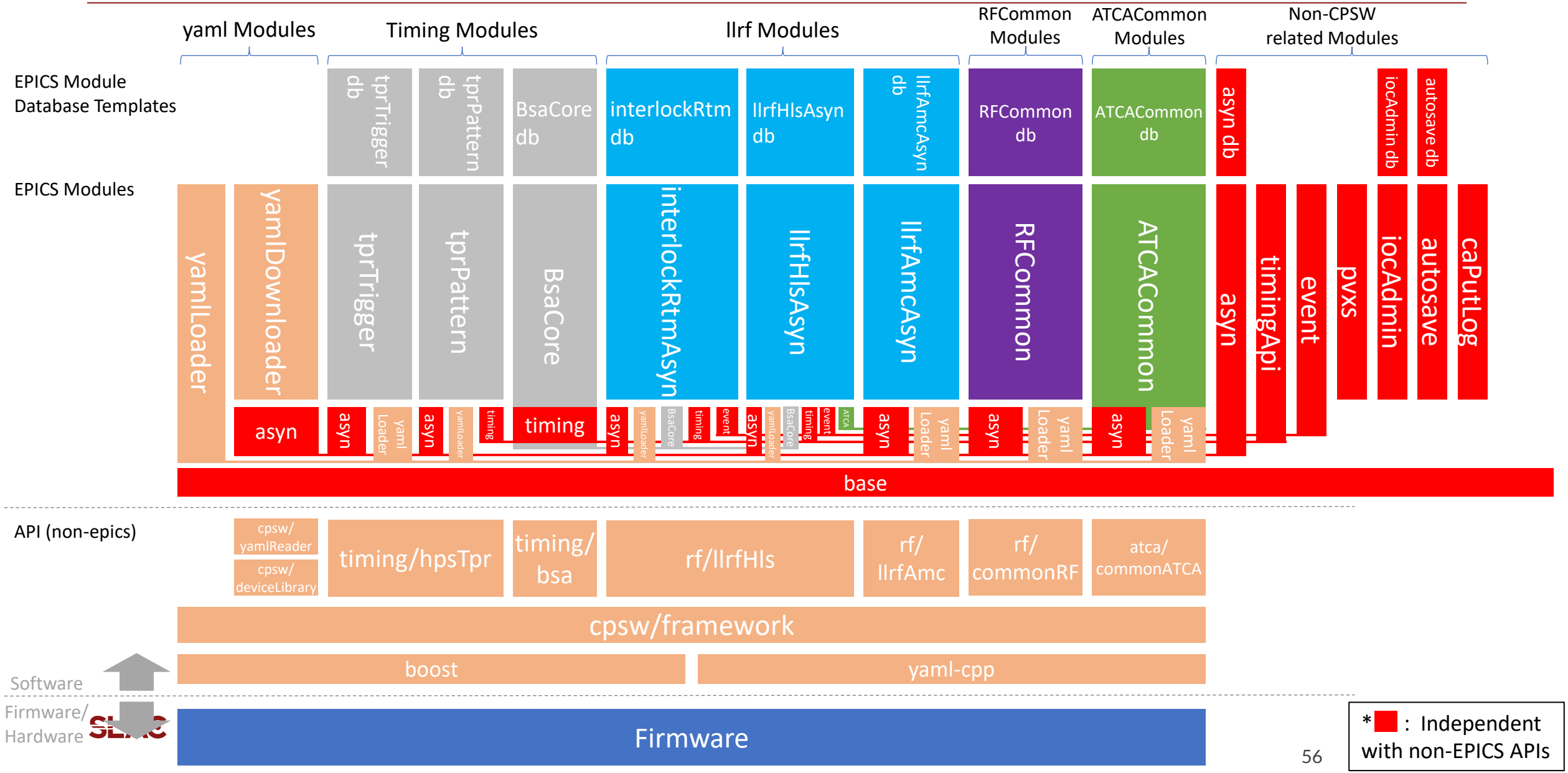


Firmware/Software Stacks for NC LLRF Application (Firmware focused)

Modular Design for UED LLRF (Firmware focused)



Firmware/Software Stacks for NC LLRF Application (LCLS-I timing only)



Firmware/Software Stacks for SC LLRF Application (LCLS-II timing only) - FDR