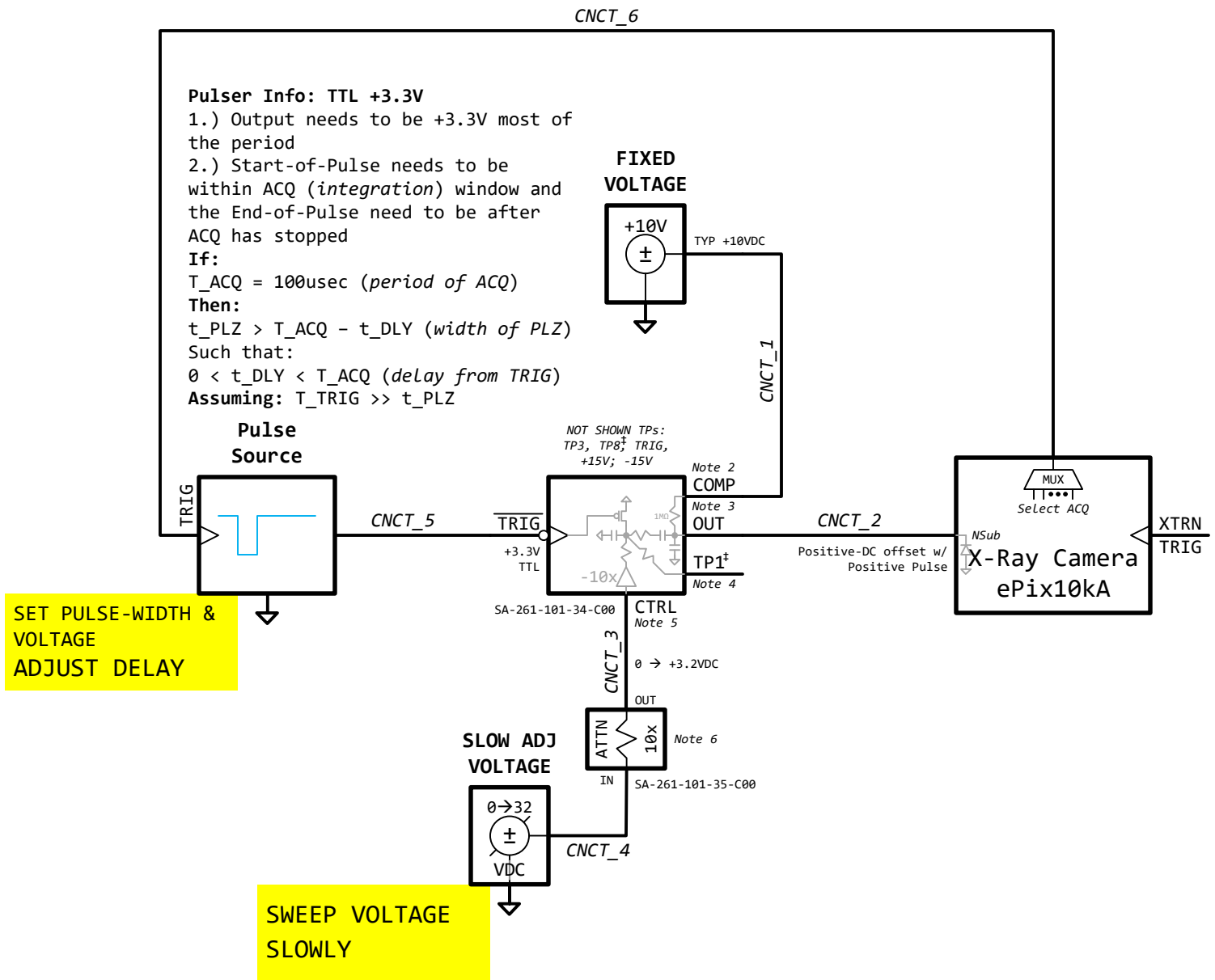


# TYPICAL SETUP: SA-261-101-34-C00

## CABLE INFO:

CNCT\_1: ADPTR x2\_Banana-M-to-BNC-F → CBL BNC-M-to-SMA-M  
 CNCT\_2: CBL SMA-M-to-BNC-M → ADPTR BNC-F-to-x2\_Banana-F  
 CNCT\_3: CBL SMA-M-to-SMA-M  
 CNCT\_4: ADPTR x2\_Banana-M-to-BNC-F → CBL BNC-M-to-SMA-M  
 CNCT\_5: CBL BNC-M-to-SMA-M  
 CNCT\_6: CBL BNC-M-to-BNC-M



## Notes:

- 1.) SYMBOL † Current limited to 5mA due absolute-voltage-potential-relative to ground > 50VDC
- 2.) **LIMIT**,  $|V_{COMP} - (-10 * V_{CTRL})| \leq 180\text{VDC}$ : C10 to C12 on SD-144-174-04 are limited to 200VDC
  - a.) COMP is used to set the DC-bias on the substrate
  - b.) The resistance between COMP and OUT is currently 1MΩ
    - i.) This is adequate unless substrate locks up—can reduced if lockup becomes an issue
  - c.)  $V_{COMP} \geq 0\text{VDC}$ : The closer to 0 the larger the substrate capacitance (*less likely to Lockup*)
- 3.) OUT is generate a positive  $0 \rightarrow +10\text{V}$  pulse relative to  $V_{COMP}$
- 4.) **FOR ALL** TEST-POINTS (TP) Use  $\geq 1\text{M}\Omega$  probe
- 5.) **LIMIT**,  $|V_{CTRL}| \leq +10\text{VDC}$ : Input resistance on CTRL node is 1kΩ
- 6.) ATTN 10x SA-261-101-35-C00
  - a.) Designed to work at max voltage  $\pm 32\text{VDC}$  input with 1kΩ load
  - b.) Had directionality (*non-symmetric voltage divider*)
  - c.) Used so can sweep pulse voltage in smaller steps
- 7.) ALL NODES ARE CLAMPED FOR PROTECTION to GND with zener-diodes: Except OUT is clamped to COMP with diode to only produce positive pulses relative to COMP (*to avoid possibly reverse biasing substrate*)