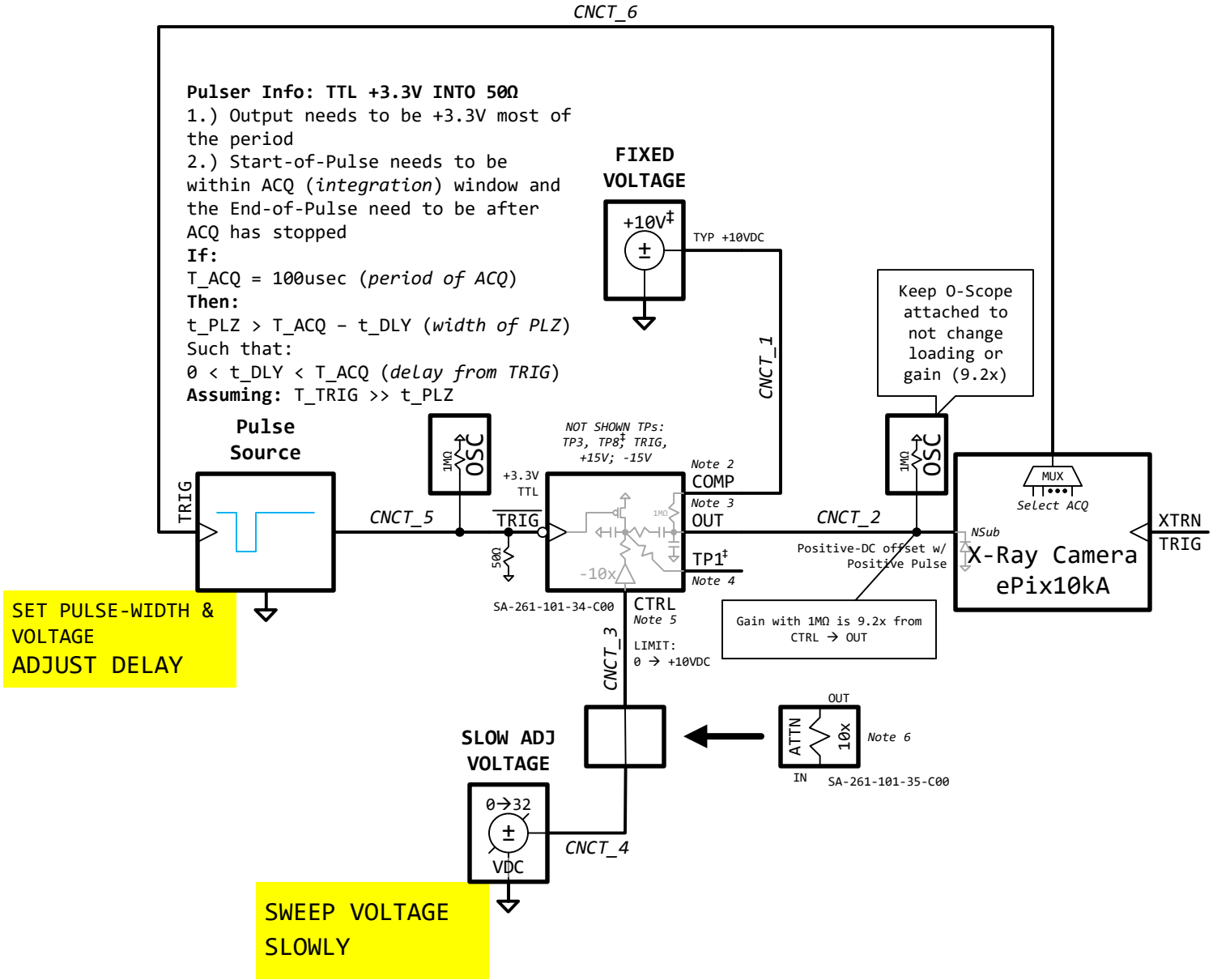
# TYPICAL SETUP: SA-261-101-34-C00

**CABLE INFO:**
CNCT_1: ADPTR x2_Banana-M-to-BNC-F → CBL BNC-M-to-SMA-M
CNCT_2: CBL SMA-M-to-BNC-M → BNC-T → ADPTR BNC-F-to-x2_Banana-F
CNCT_3: CBL SMA-M-to-SMA-M (*USE WITH ATTN*)
CNTC_4: ADPTR x2_Banana-M-to-BNC-F → CBL BNC-M-to-SMA-M
CNCT_5: CBL BNC-M-to-SMA-M → SMA-T loaded with 50Ω
CNCT_6: CBL BNC-M-to-BNC-M




**Notes:**
1.) SYMBOL ‡ Current limited to 5mA due absolute-voltage-potential-relative to ground > 50VDC
2.) **LIMIT**, |V_COMP – (-10*V_CTRL)| ≤ 180VDC: C10 to C12 on SD-144-174-04 are limited to 200VDC
    a.) COMP is used to set the DC-bias on the substrate
    b.) The resistance between COMP and OUT is currently 1MΩ
        i.) This is adequate unless substrate locks up—can reduced if lockup becomes an issue
    c.) V_COMP ≥ 0VDC: The closer to 0 the larger the substrate capacitance (*less likely to lockup*)
3.) OUT is generate a positive 0 → +100V pulse relative to V_COMP
4.) *FOR ALL* TEST-POINTS (TP) Use ≥ 1MΩ probe
5.) **LIMIT**, 0 ≤ V_CTRL ≤ +10VDC: Input resistance on CTRL node is 1kΩ
6.) **OPTIONAL**: ATTN 10x SA-261-101-35-C00
    a.) Designed to work at max voltage ±32VDC input with 1kΩ load
    b.) Had directionality (*non-symmetric voltage divider*)
    c.) Used so can sweep pulse voltage in smaller steps
7.) ALL NODES ARE CLAMPED FOR PROTECTION to GND with zener-diodes: Except OUT is clamped to COMP with diode to only produce positive pulses relative to COMP (*to avoid possibly reverse biasing substrate*)