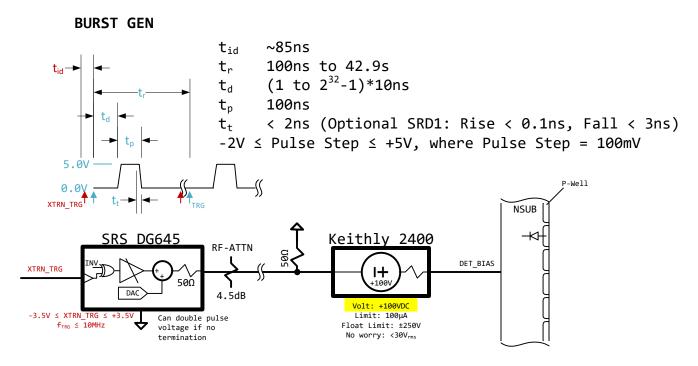
ePix10kA: Proposed Idea for Voltage-Pulse to substrate 20230213

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What I know... DET_BIAS \approx +100V to reverse bias substrate Pair creation energy in Si is ~3.6[eV] PIX_TOT = 4 x 176x192 = 135168 pixels C_pix \approx 150fF (*not sure if at this bias*) Trip point: 2.4MeV/pix \rightarrow 6.6e5 electrons \rightarrow 107fC of charge over 50psec Max Pulse is 10MeV/pix

What this means to generate same charge, as we can't generate same pulse, is we need to hit the back plain with $V = Q/C_{pix} = 712[mV]$ in at least the integration window time. Our integration window is 100µsec (10kHz) this setup can do it. Just need an attenuator of 12dB gives us steps from 0 to 1.2V in 24mV steps. The 1.2V is to give us close to the same charge seen at max pulse value.

What will change this setup slightly is measuring substrate capacitance to get a better idea of what it really is when biased, but all that would change is the attenuator value.

Really need to measure the total camera cap vs. bias curve to see what it really is... as Chris is say 1pF per chip and Philip 5nF per chip, which is a big difference... will have to see what I can adjust it to and maybe decrease bias voltage to increase cap will help.

Where my work is...

https://colab.research.google.com/drive/1UixspSZB9yI2C3I9ExHIxnj23dLeqB0M#scrollTo=4MsMp45MP3I9