ePix100a

Prototype Datasheet

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U.S. DEPARTMENT OF ENERGY
Office of Science

RED ***Integrated Circuits***

SLAC NATIONAL ACCELERATOR LABORATORY

Outline

- Pad Frame
- Terminations
- Power up and Pulsing
- Configuration
- Calibration
- Acquisition and Read-out
- Test Points
- Chip ID
- Additional features (Temperature Compensation, Interleaved Read-out)

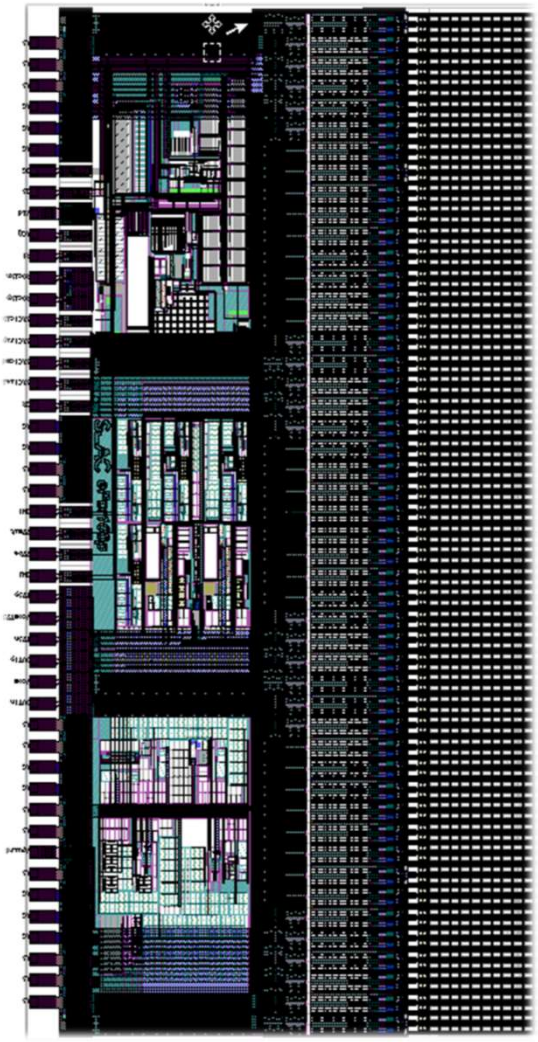
Pad Frame - Supplies

Analog Supply (AS) = 2.5V

Analog Ground (AG) = 0V

Digital Supply and Ground (DS,DG) = 2.5V and 0V

1	AS
2	AS
3	AS
4	AG
5	AG
6	AG
7	DG
8	DS
9	Vid
10	ACQ
11	R0
12	ROCLKn
13	ROCLKp
14	SACIclk
15	SACIrsp
16	SACIcmd
17	SACIsel
18	GR
19	AG
20	AG
21	AS
22	AS
23	DM1
24	PPmat
25	PPbe
26	DM2
27	TPSp
28	VcomTPS
29	TPSn
30	OUT1p
31	Vcom
32	OUT1n
33	AS
34	AS
35	AG
36	AG
37	AS
38	AS
39	Vguard
40	AS
41	AG
42	AG
43	AG
44	AS
45	AS
46	AS



- *Note: AS should be the reference on the PCB.*

Pad Frame

DIGITAL

Vid (High Voltage) and Digital Supply
(Once ChipID has been programmed Vid must be connected to DS =2.5V)

Acquisition and Reset inputs
(Default state low)

Read Out Clock
(LVDS inputs MUST BE low by default)

SACI in/out

General Reset input
(Default State Low – means under reset)

Digital Monitor Outputs

Power Pulsing Signals

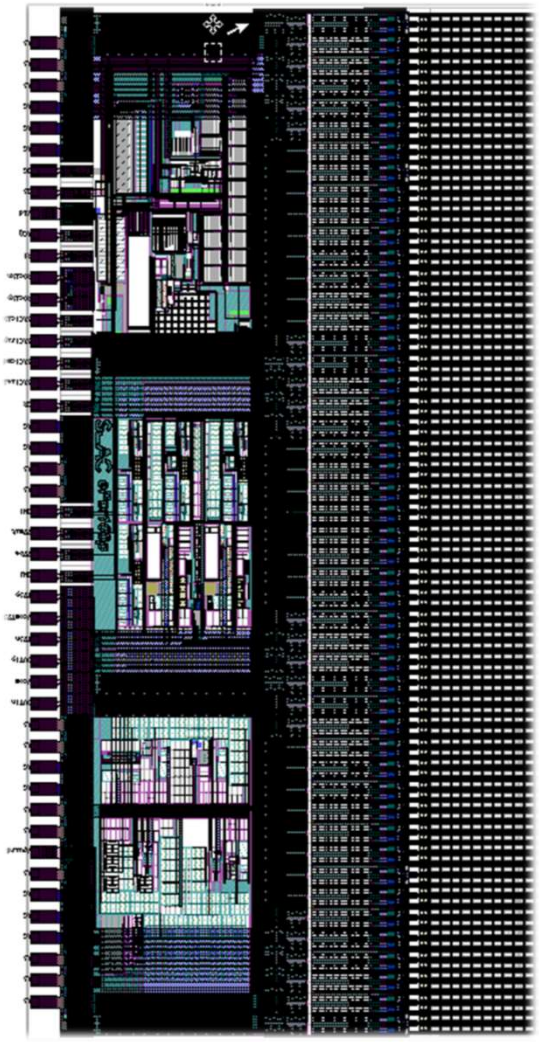
ANALOG

Test Point System
(VcomTPS[in] = 1V connected to AD9259 VREF Pin)

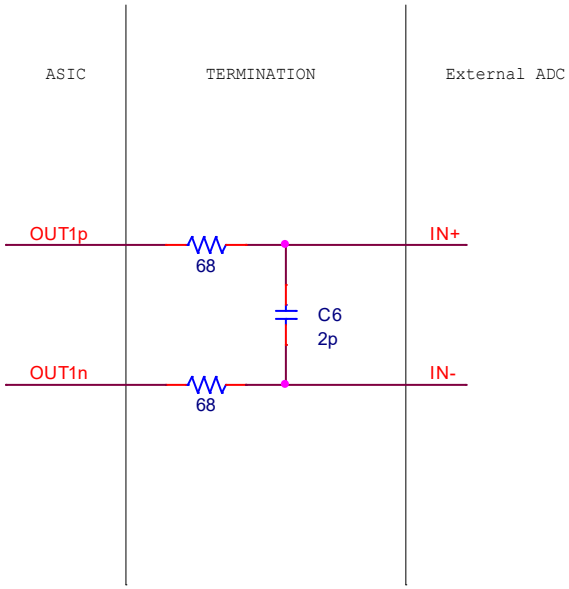
Analog Out and Vcom
(Vcom[in] = 1V connected to AD9259 VREF Pin)

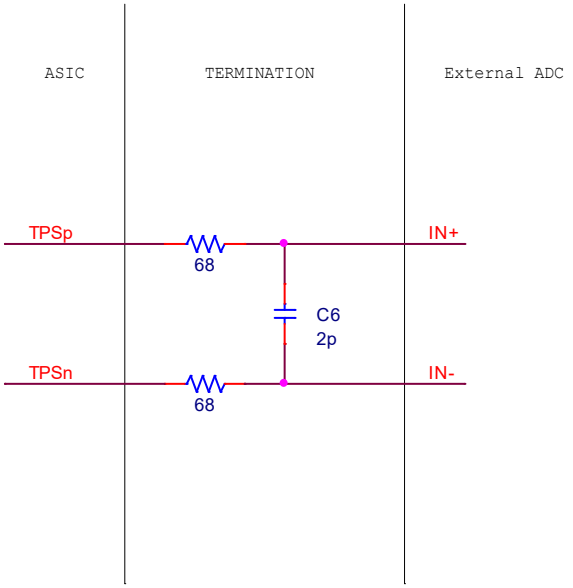
Vguard
(Sensors Guard Ring Voltage)

1	AS
2	AS
3	AS
4	AG
5	AG
6	AG
7	DG
8	DS
9	Vid
10	ACQ
11	R0
12	ROCLKn
13	ROCLKp
14	SACIclk
15	SACIrsp
16	SACIcmd
17	SACIsel
18	GR
19	AG
20	AG
21	AS
22	AS
23	DM1
24	PPmat
25	PPbe
26	DM2
27	TPSp
28	VcomTPS
29	TPSn
30	OUT1p
31	Vcom
32	OUT1n
33	AS
34	AS
35	AG
36	AG
37	AS
38	AS
39	Vguard
40	AS
41	AG
42	AG
43	AG
44	AS
45	AS
46	AS



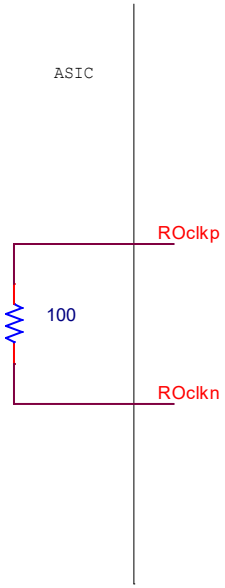
Terminations – Analog Outputs





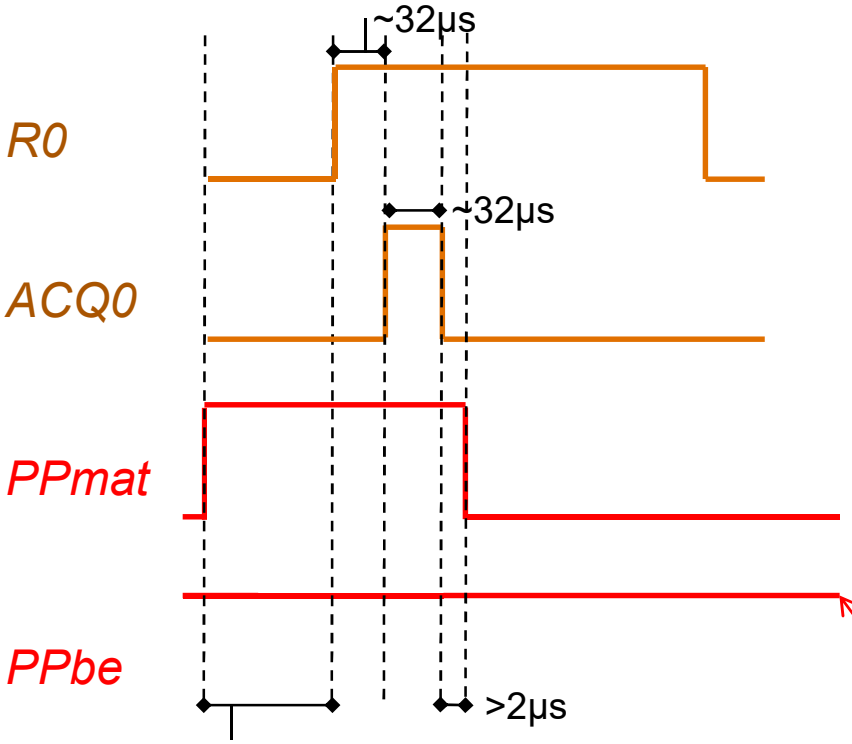
The value of the filter capacitor should be tweaked according to test results.

Terminations – Read-out Clock



There is a 100 Ohm Termination if SLVDSbit (reg6 bit 4) is 1. (Default is 0 – Open Circuit Termination)

Power Up and Pulsing Signals



fastPP on: 30µs
fastPP off: 300µs

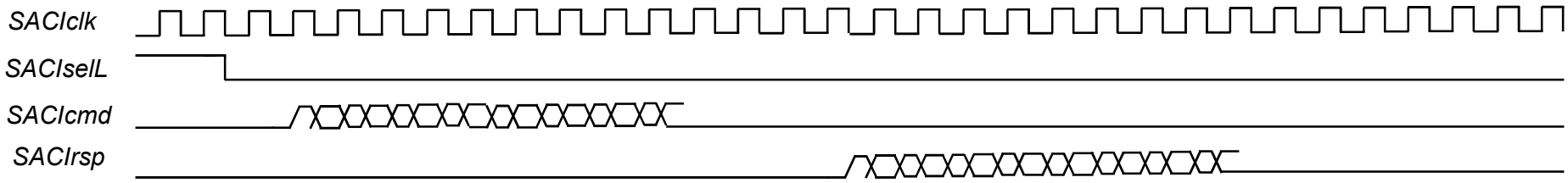
The Back-End by default is always ON. In order to enable the BE Power Pulsing PP_OCB_S2D bit (reg10 b0) must be set to 0.

- *Note: fastPP bit is reg10 bit 7 and the fastPP is activated by default*

Configuration

- SACI Commands
- Global Registers
- Counters Registers
- Chip ID Registers
- Multiple Pixels Configuration
- Single Pixel
- Dummy Pixel Configuration

Configuration – SACI Commands



Configuration – SACI Commands

RW	CMD	Function	Clock Cycle
0	0	Prepare for Read-out	
0/1	1	Read/Write Global/Counter Stop/Chip ID Register	
1	2	Write Row	
1	3	Write Column	
1	4	Write Matrix	
0/1	5	Read/Write Pixel	
0/1	6	Read/Write Start Row/Column Counter Register	2
0	7	Read Chip ID must be executed after programing	2
1	7	Prepare to Write Chip ID	
x	8	Prepare for Row/Column/Matrix Configuration	

- The ASIC decoded the command last 4 bits. Any given command longer than 4 bits will be interpreted as a 4 bit command.

Configuration - Global Registers

		Address															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
BIT	0	Monost_Pulser 0	Pixel Dummy	Pulser 0	DM1 0	Pulser_DAC 0	DM1en	VREF_DAC 0	TPS_tcomp	TPS_GR 0	PP_OCB_S2D	Preamp 0	S2D_tcomp	tc 0	TPS_tcDAC 0	S2D_tcDAC 0	test_BE
	1	Monost_Pulser 1		Pulser 1	DM1 1	Pulser_DAC 1	DM2en	VREF_DAC 1	TPS_MUX 1	TPS_GR 1	OCB 0	Preamp 1	Filter_DAC 0	tc 1	TPS_tcDAC 1	S2D_tcDAC 1	is_en
	2	Monost_Pulser 2		Pulser 2	DM1 2	Pulser_DAC 2		VREF_DAC 2	TPS_MUX 1	TPS_GR 2	OCB 1	Preamp 2	Filter_DAC 1	S2D 0	TPS_DAC 0	S2D_DAC 0	DelEXEC
	3			Pulser 3	DM1 3			VREF_DAC 3	TPS_MUX 2	TPS_GR 3	OCB 2		Filter_DAC 2	S2D 1	TPS_DAC 1	S2D_DAC 1	DelCCKreg
	4			Pulser 4	DM2 0		SLVDSbit	VREF_DAC 4	TPS_MUX 3	S2D_GR 0	Monost 0	Pixel_CB 0	Filter_DAC 3	S2D 2	TPS_DAC 2	S2D_DAC 2	
	5			Pulser 5	DM2 1			VREF_DAC 5	RO_Monost 0	S2D_GR 1	Monost 1	Pixel_CB 1	Filter_DAC 4	S2D_DAC_Bias 0	TPS_DAC 3	S2D_DAC 3	
	6			Pulser 6	DM2 2				RO_Monost 1	S2D_GR 2	Monost 2	Pixel_CB 2	Filter_DAC 5	S2D_DAC_Bias 1	TPS_DAC 4	S2D_DAC 4	
	7			Pulser 7	DM2 3				RO_Monost 2	S2D_GR 3	fastPP_enable			S2D_DAC_Bias 2	TPS_DAC 5	S2D_DAC 5	
	8			Pulser 8													
	9			Pulser 9													
	10			Pbit													
	11			atest													
	12			test													
	13			Sab_test													
	14			Hrtest													
	15																

- Bias Point
- Calibration Blocks
- Test Points
- Matrix Read-out
- Output Voltage Range
- Temperature Compensation Blocks
- LVDS and Digital Monitors
- Power Pulsing

Configuration Registers

- WRITE Configuration Registers:

- READ Configuration Registers:

Configuration – Other Registers

Counters Registers and Chip ID Registers

Address (cmd = 6 for Start Register cmd=1 for Stop Registers)				
17	18	19	20	21
Row Start (9bits)	Row Stop (9bits)	Column Start (7bits)	Column Stop (7bits)	CHIP ID (16 bits)
		Not Available		

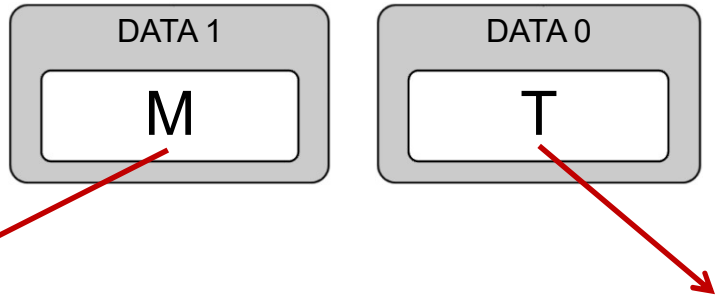
- Row Stop is 97 and Column Stop is 95 by default in the prototype version (Row Stop will be 353 in the full analog version);
- If the stop register values are not defined the default values are assumed;
- When the stop value is reached the counter cycle starts again automatically;
- If stop value is smaller than start value a central region of the matrix can be masked (Additional feature to be tested).

Configuration – Other Registers

- WRITE Start Counter Registers (requires 2 Clock Cycle):

- WRITE Stop Counter Registers:

Pixel Registers



Pixel Mask Bit

- 0 = Pixel ready for acquisition or test
- 1 = Pixel “Masked”, Reset Applied + Analog Output is the Baseline.

Pixel Test Bit

- 0 = Pixel in acquisition mode
- 1 = Pixel in test mode, i.e. connected to test pulser

* Pixel Registers are not connected to Master Reset, therefore Matrix and Dummy Pixel **MUST** be configured

Pixels Configuration

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	x	8	x	x

CMD = Prepare for Multiple Pixels configuration

Row = 9 bit row address

Bank+Col = 7 bit column address (LSB) + 4 bit Bank disable [A B C D]; D = MSB
if A/B/C/D = 0 then the corresponding Bank (A/B/C/D) will be written
if A/B/C/D = 1 then the corresponding Bank (A/B/C/D) will not be written

Configure Row in a Bank

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	17	Row

CMD = Selects Row Counter and writes addr R

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	19	Bank+x...x

CMD = Selects Col Counter and writes addr C

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	2	x	x…xMT

CMD = Activates all columns and shifts data in

Configure Pixel

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	17	Row

CMD = Selects Row Counter and writes addr R

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	19	Bank+Col

CMD = Selects Col Counter and writes addr C

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	5	x	x…xMT

CMD = Shift data in addressed pixel

Configure entire Matrix

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	4	x	x…xMT

CMD = Select Matrix and shifts data in all pixels

Configure Row

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	17	Row

CMD = Selects Row Counter and writes addr R

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	2	x	x…xMT

CMD = Activates all columns and shifts data in

Configure Column

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	19	Bank+Col

CMD = Selects Col Counter and writes addr C

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	3	x	x…xMT

CMD = Activates all rows and shifts data in

Dummy Pixel Configuration

- Dummy Pixel is configured as a Register:

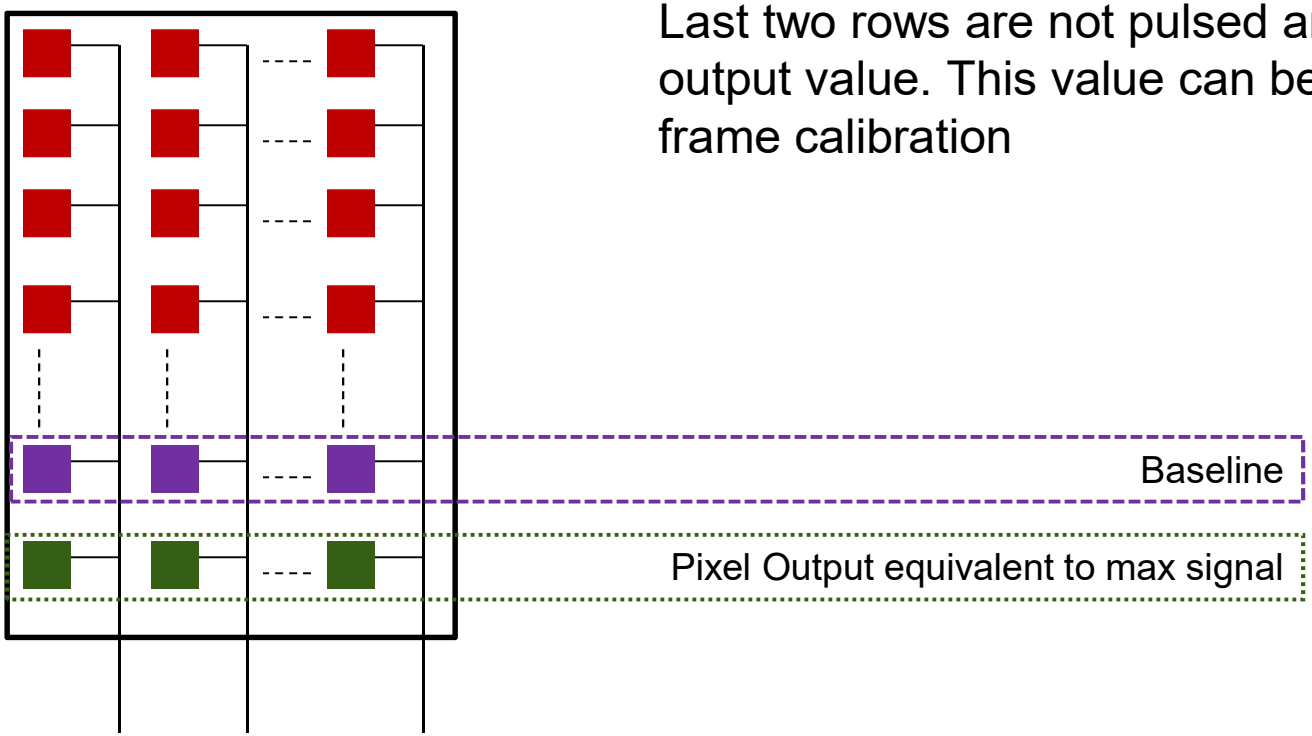
CMD = Selects Register 2 (Dummy Pixel) and writes data

- Dummy Pixel Nodes connected to the Analog Monitor:
  - **in** – Pixel input node (Analog Monitor 0)
  - **fin** – Pixel Filter input node (Analog Monitor 1)
  - **fo** – Pixel Filter output node (Analog Monitor 2)
  - **abus** – Pixel output node (Analog Monitor 3)
  - **cdso3** – Pixel sampling node (Analog Monitor 4)

Calibration

- In-Frame Calibration
- Offline Calibration
  - Matrix Test Mode
  - Output Voltage Range Adjustment
  - Back-End Calibration

In-Frame Calibration

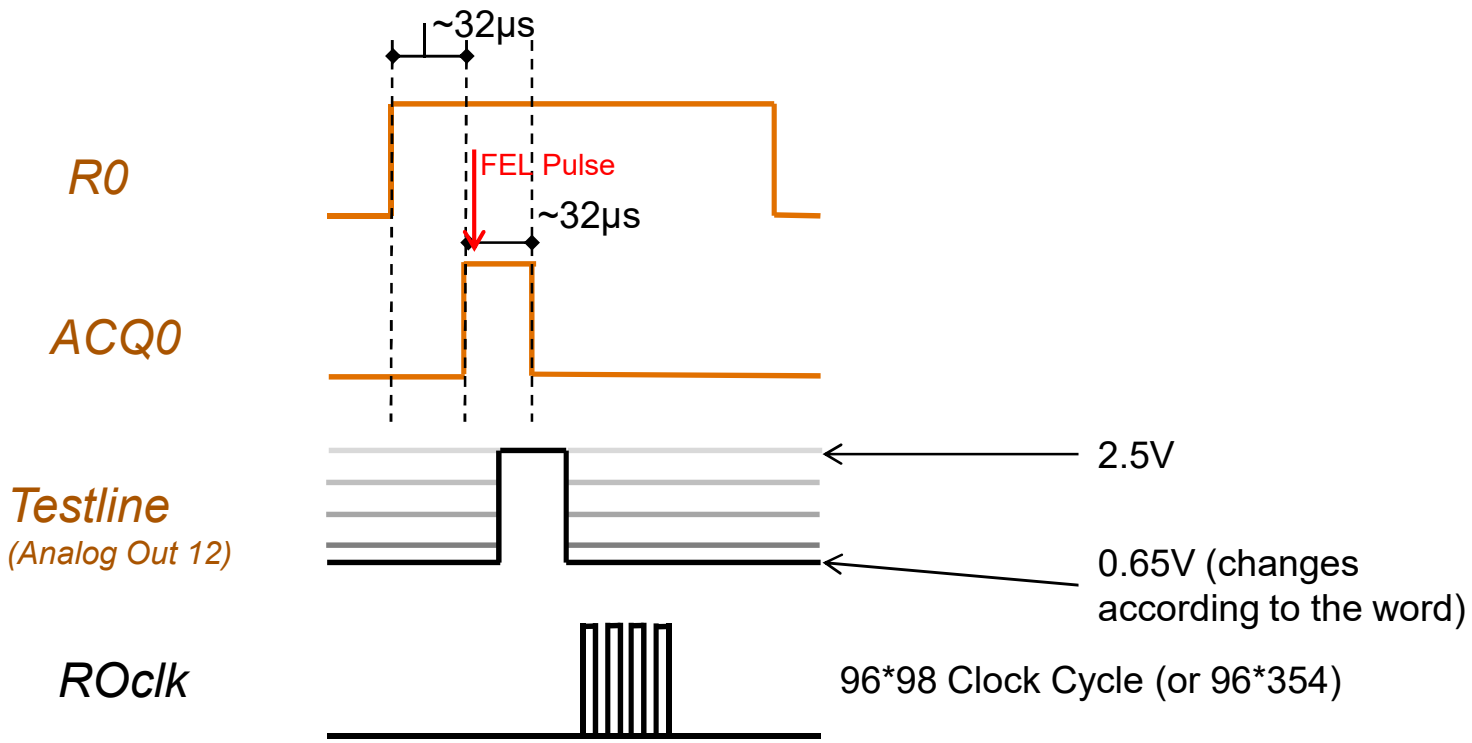


Last two rows are not pulsed and give a fixed output value. This value can be use for an in-frame calibration

Matrix Test Mode

- **Configure Matrix with T = 1**
- **Configure Test Pulser, i.e. write Register 3:**
  - DATA 0:9: **10 bit Pulser Code** – Test Pulser Signal Level
    0 = Min signal injected in the pixels
    1023 = Max signal injected in the pixels
  - DATA 10: **Pbit** – Pulser Counter Direction
    0 = increasing
    1 = decreasing
  - DATA 11: **atest** – Automatic Test Mode
    0 = OFF, i.e. Pulser injects the signal defined by the 10 bit code (register bits 0:9)
    1 = ON, i.e. Pulser injects signals defined by the counter. Counter starts with the value 0 and increases / decreases (**Pbit**) its value at each / every second (**Sab-test**) ACQ pulse
  - DATA 12: **test** – Pulser Activation
    0 = Pulser OFF
    1 = Pulser ON
  - DATA 13: **Sab_test** – Counter Clock Option
    0 = Counter changes its value at each ACQ pulse
    1 = Counter changes its value every second ACQ pulse
  - DATA 14: **Hrtest** – Pulser High Resolution Mode
    0 = High Resolution OFF
    1 = High Resolution ON
- **Provide ACQ and R0 pulses in order to inject the Pulser signal into pixels**

Matrix Test Mode



Output Voltage Range Coarse Optimization

Configure Pulser bits Register Value to max;

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	1	3	1023

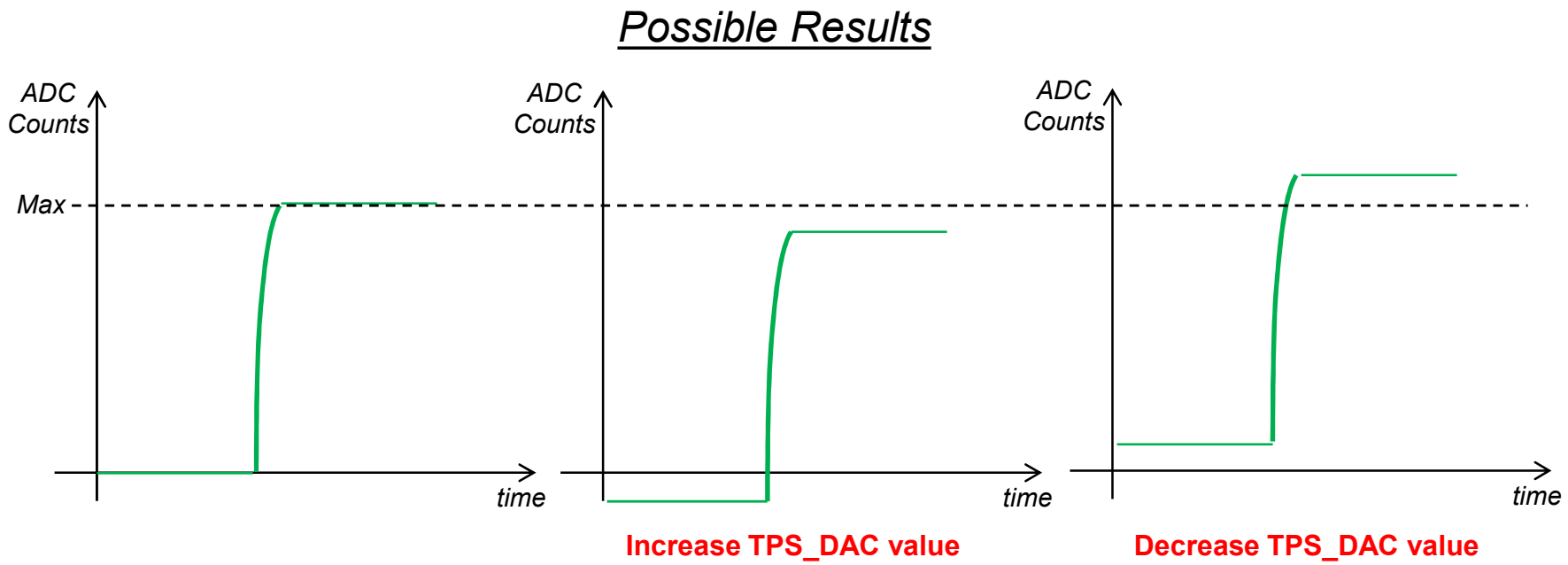
NOTE: This will also delete previous Pulser Settings.

Apply ACQ;

Reduce TPS_GR bit (optional);

Sample *TPSp-TPSn;*

Output Voltage Range Coarse Optimization



Copy TPS_DAC value in S2D_DAC value;

Output Voltage Range Fine Optimization

Prepare for Matrix Configuration (CMD=8):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	x	8	x	x

Test BE Enable (reg16 bit0 = 1):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	1	16	1

Select Row 97

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	17	97

Mask = S2D_tcomp bit (reg12 bit 0);

for *word* = 0 to 63 step 63

Configure FilterDAC Register with *word;*

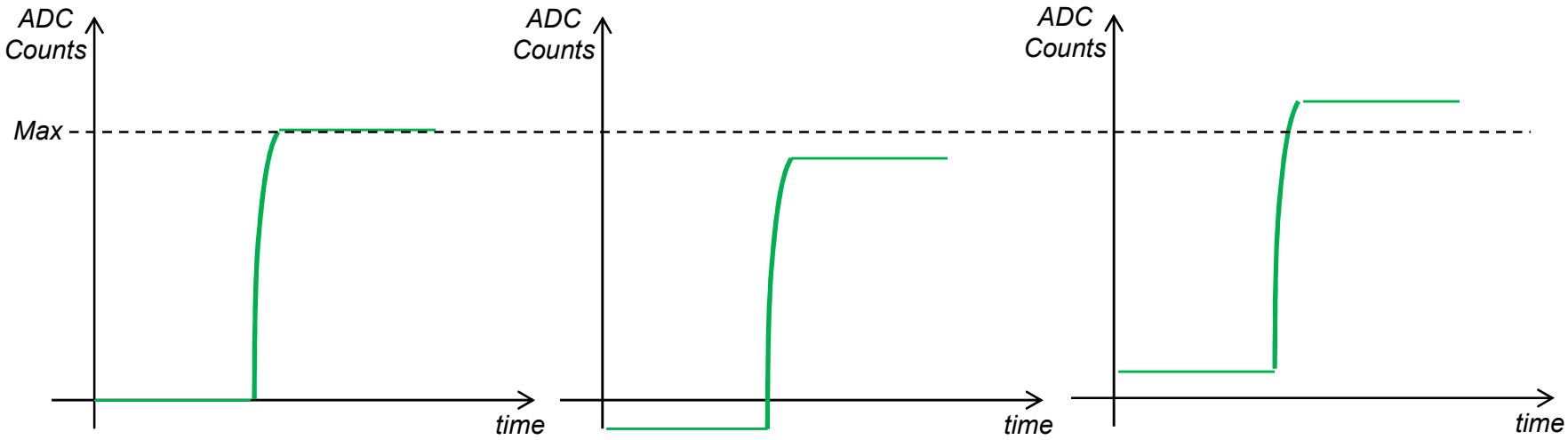
SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	1	12	[word][Mask]

run Read Out Clock for 96 periods;

end

Output Voltage Range Fine Optimization

Possible Results



Increase S2D_DAC value

Decrease S2D_DAC value

Back – End Calibration

Prepare for Matrix Configuration (CMD=8):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	x	8	x	x

Test BE Enable (reg16 bit0 = 1):

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	1	16	1

Select Row 97

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	6	17	97

Mask = S2D_tcomp bit (reg12 bit 0);

for *word* = 0 to 63

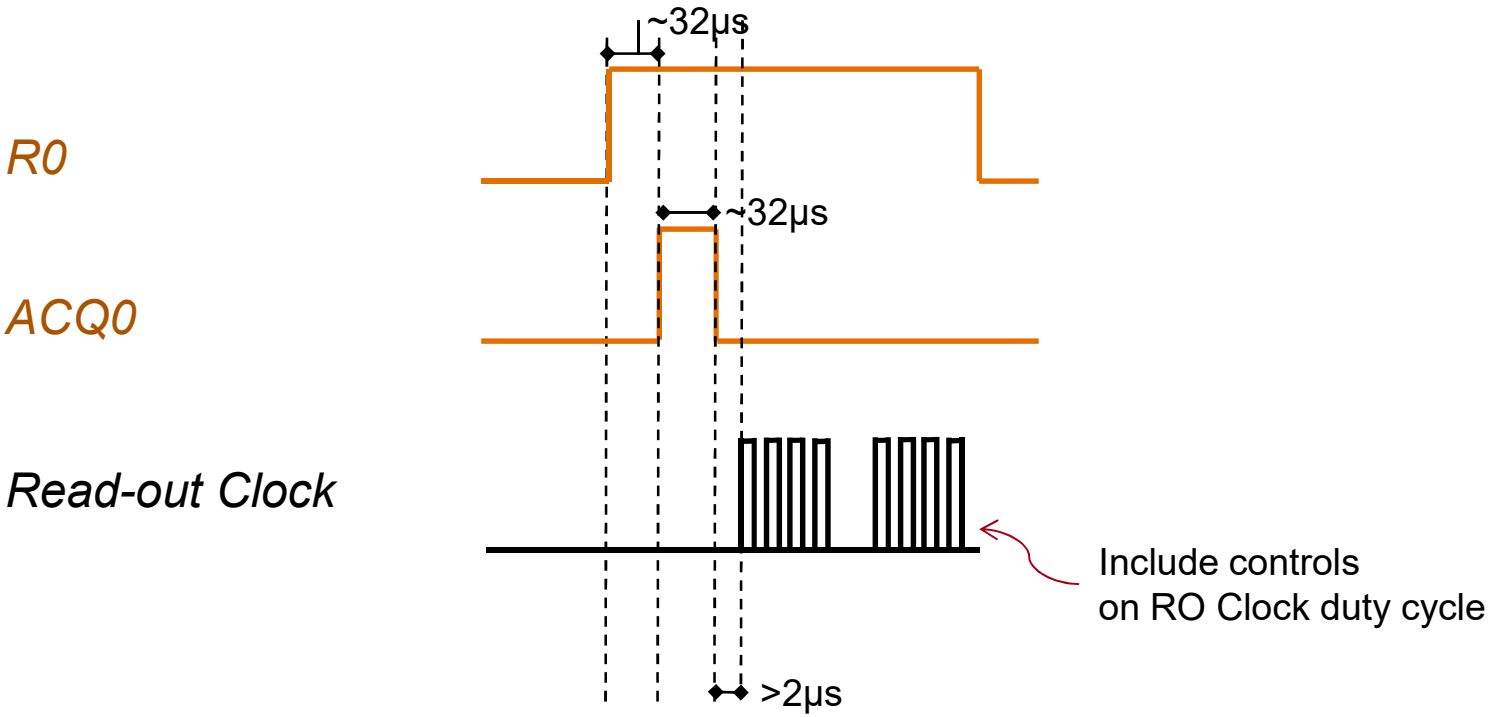
Configure FilterDAC Register with *word;*

SET (1bit)	RW (1bit)	CMD (7bit)	ADDR (12bit)	DATA (32bit)
1	1	1	12	[word][Mask]

run Read Out Clock for 96 periods;

end

Acquisition and Read-out Signals



- IMPORTANT: when not used Read-out clock MUST BE LOW;
- Before the first read-out cycle *CMD=0* is required. After the ASIC gives the *ack,* it is ready to receive the read-out clock.
- In order to resynchronize the pointer position inside the matrix the FPGA must give the exact number of clock cycles (96*98 or 96*354 for the full version) or,
- Alternatively give prepare for Read-Out command (*CMD=0*) between frames.

Test Points – Digital Monitors

SLAC

DM1

	Mux
0	clk
1	exec
2	ro_rst
3	ack
4	is_en
5	ROWclk
6	ADDR0
7	ADDR1
8	ADDR2
9	ADDR3
10	ADDR4
11	CMD0
12	CMD1
13	CMD2
14	CMD3
15	config

DM2

	Mux
0	clk
1	exec
2	ro_rst
3	ack
4	is_en
5	ROWclk
6	DB0
7	DB1
8	DB2
9	DB3
10	DB4
11	DB5
12	DB6
13	DB7
14	ADDRmat
15	config

Note: Digital Monitors are deactivated by default (DM1en and DM2en are 0)

Test Points – Analog

	Mux		Description	
Analog	0	in	ok	
	1	fin	ok	
	2	fo	ok	
	3	abus	ok	
	4	cdso3	ok	
	5	bgr_2V	ok	*bgr voltage (should be equal to 2V)*
	6	bgr_2vd	ok	*bgr variable voltage*
	7	vx_comp	ok	*Output Driver DAC Reference (the temperature variation on this will decide the temperature compensation bits)*
	8	vcmi	ok	*Output Driver Reference*
	9	Pix_Vref	ok	*Baseline Control Voltage to the Pixel*
	10	VtestBE	ok	*BE Calibration Voltage*
	11	Pix_Vctrl	ok	*Filter Voltage*
	12	testline	ok	*Pulser Output*
	13	PTAT	ok	
	14	Not Assigned		
	15			

Chip ID - Programming

- WRITE Chip ID Register (ADDR=21)[1 bit per cycle]:

- Prepare to Write Chip ID :

- Apply *High Voltage* for *x* ms then return to 2.5V;
- Repeat until all bits are written.

Chip ID - Reading

- Prepare to Read Chip ID :

- Read Chip ID Register:

Additional Features

- Temperature compensation is activated by default;
  - S2D_tc, TPS_tc = 1 (by default);
  - If deactivated S2D_DAC and TPS_DAC value will change (the value will be around 46);
- Interleaved Read – Out (reg16 bit 1)
  - is_en = Interleaved Column Selection Enable = 0 means enabled.
  - During Row/Column/Matrix Configuration command is_en will be automatically deactivated;
  - MUST BE deactivated when reading out a part of the matrix that does not go beyond the 47th column.

Appendix – Global Register Comments

	Number of Bits	Dec Value	Bin Value	Function	
tc	2	0	00	*BGR temperature Compensation Bits*	ANALOG
TPS_DAC	6	22	010110	*TestPoint System Input Common Mode*	
TPS_GR	4	3	0011	*TestPoint System Output Dynamic Range*	
TPS_MUX	4	0	0000	*TestPoint System Input Selector*	
TPS_tcomp	1	1	1	*TestPoint System temperature Compensation On/Off*	
TPS_tcDAC	2	0	00	*TestPoint System temperature Compensation Gain*	
RO_Monost	3	3	011	*Programmable Read Out Delay*	
S2D	3	3	011	*Output Driver Driving Capabilities and Stability*	
S2D_DAC	6	22	010110	*Output Driver Input Common Mode*	
S2D_GR	4	3	0011	*Output Driver Output Dynamic Range*	
S2D_tcDAC	2	1	01	*Output Driver temperature Compensation Gain*	
S2D_tcomp	1	1	1	*Output Driver temperature Compensation On/Off*	
S2D_DAC_Bias	3	3	011	*Output Driver Input Common Mode*	
Pulser_DAC	3	3	011	*Test Pulser Current*	
PP_OCB_S2D	1	1	1	*Balcony On/Off (1 is On)*	
OCB	3	3	011	*Balcony Driver Current*	
Monost	3	3	011	*Fast Power Pulsing Speed*	
Filter_DAC	6	33	100001	*Pixel Filter Level (Default 1V)*	
VREF_DAC	6	22	010110	*Baseline DAC (Default 1.65V)*	
Preamp	3	4	100	*Preamplifier Current*	
Pixel_CB	3	4	100	*Pixel Output Buffer Current*	
fastPP_enable	1	1	1	*Fast Power Pulsing Enable*	
Pulser	10	0	0000000000	*Test Pulser Level*	DIGITAL
test	1	0	0	*test mode*	
atest	1	0	0	*Automatic test mode On/Off (0 is off)*	
Pbit	1	0		*Pulser Counter Direction*	
HRtest	1	0	0	*High Resolution Mode Test*	
Sab_test	1	0	0	*test mode with Dark Frame*	
is_en	1	0	0	*Interleaved ReadOut Enable*	
Monost_Pulser	3	0		*Pulser vs Pixel ON delay*	
DM1	4	0	0000	*Digital Monitor Mux 1*	
DM2	4	1	0001	*Digital Monitor Mux 2*	
DelEXEC	1	0	0	*EXEC Delay ENABLE*	
DelCCKreg	1	0	0	*CCKreg Delay ENABLE*	
test_BE	1	0	0	*test BackEnd*	Matrix
DM1en	1	0	0	*Digital Monitor 1 Enable*	PADS
DM2en	1	0	0	*Digital Monitor 2 Enable*	
SLVDSbit	1	0	0	*LVDS Impedence Matching Enable*	