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Design and Characterization of the ePix10k prototype: a High Dynamic Range integrating pixel ASIC for LCLS detectors.

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ABSTRACT

ePix10k is a variant of a novel class of integrating pixel ASICs architectures optimized for the processing of signals in second generation LINAC Coherent Light Source (LCLS) X-Ray cameras. The ASIC is optimized for high dynamic range application requiring high spatial resolution and fast frame rates. ePix ASICs are based on a common platform composed of a random access analog matrix of pixel with global shutter, fast parallel column readout, and dedicated sigma-delta analog to digital converters per column. The ePix10k variant has 100umx100um pixels arranged in a 176x192 matrix, a resolution of 140e- r.m.s. and a signal range of 3.5pC (10k photons at 8keV). In its final version it will be able to sustain a frame rate of 2kHz. A first prototype has been fabricated and characterized. Performance in terms of noise, linearity, uniformity, cross-talk, together with preliminary measurements with bump bonded sensors are reported here.

Keywords: ASIC, front-end electronics, photon science, mixed-signal, detectors, high dynamic range, integrating, pixel.

1. INTRODUCTION

The first years of the Linac Coherent Light Source (LCLS) operation have shown the need to support a wide variety of experiments with a correspondent variety of detectors. Modular scalable detectors with dedicated interfaces are key elements to provide time and cost effective cameras that are easy to adapt and support. ePix is a novel class of ASIC architectures based on a common platform optimized for processing the signals from LCLS cameras. The unique characteristics of Free-Electron Laser (FEL) sources in terms of brilliance and narrow pulse duration have increased the need for new large area detectors with fast readout and specifications that, depending on the experiment, can range from ultra-low noise requirements [1] to extremely large full-scale and dynamic ranges [2]. Cameras based on architectures with a higher level of parallelism have proven to be more suitable for FEL applications. Hybrid pixel detectors seem at the moment the best compromise between complexity, development time, and cost [3].

The ePix platform architecture is composed of a random access analog matrix of pixel with global shutter, fast parallel column readout, and dedicated sigma-delta analog to digital converters per column. It also implements a dedicated control interface and all the required support electronics to perform configuration, calibration and readout of the matrix [4].

The ePix platform development has been scheduled in stages and each stage will produce a device with sufficient functionalities to be used in real experiments.

Based on this platform a class of front-end ASICs and several camera modules [5], meeting different requirements, can be developed designing specific pixel circuits. This approach reduces development time and expands the possibility of integration of detector modules in size, shape or functionality as different modules can be assembled in the same camera.

The ePix platform is currently under development together two integrating pixel architectures:

ePix100 is optimized for **ultra-low noise** applications. It has pixels of 50x50 μm^2 size arranged in a 352x384 matrix and a resolution of less than 50e^- r.m.s. and a signal range of 35fC (100 photons at 8keV). In its final version it will be able to sustain a frame rate of 1kHz.

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ePix10k is optimized for **high dynamic range** applications. It has pixels of 100x100 µm^2 size arranged in a 176x192 matrix and a resolution of 140e$^-$ r.m.s. and a signal range of 3.5pC (10k photons at 8keV). In its final version it will be able to sustain a frame rate of 2 kHz.

The prototype versions of both ASIC do not perform the digital conversion on chip but the in-pixel sampled analog signal is transferred to the output through a fully analog buffer chain. The analog output in then converted with an external ADC. This imposes limits on the read-out speed. The final version where the analog to digital conversion will be performed with Sigma-Delta ADCs inside the ASIC will allow for higher than 120 Hz readout speed. The ePix10k ASIC prototype has a matrix of 48x48 pixels, a size of 6.7×5 mm^2 and is fabricated in TSMC CMOS 0.25µm technology.

In Section 2 the ASIC architecture will be discussed together with the pixel architecture and functionality. Experimental results will be discussed in Section 3.

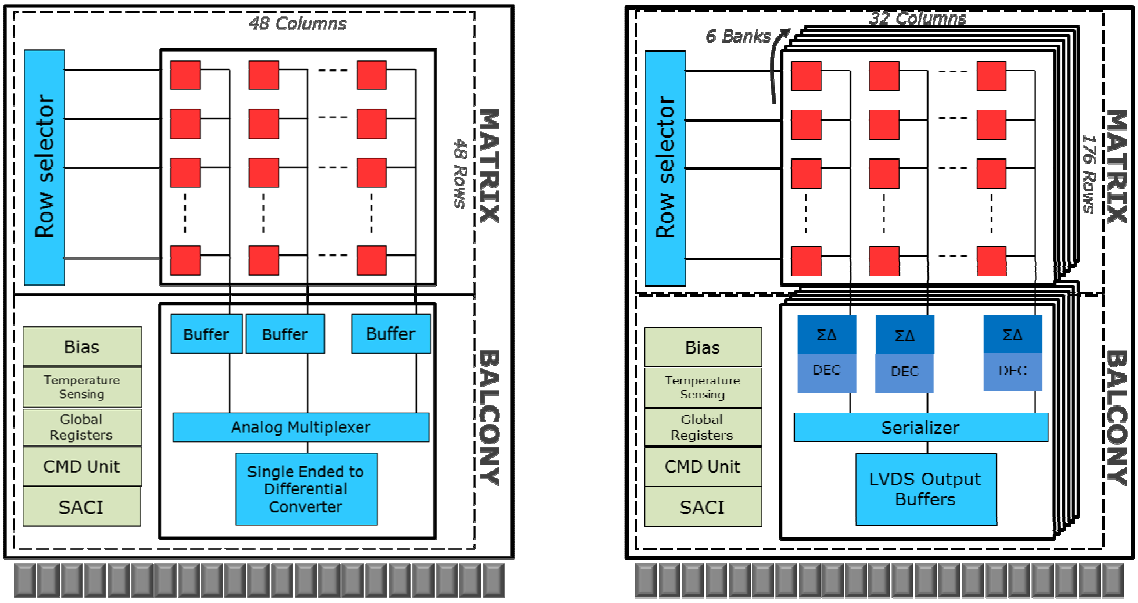


Figure 1. Simplified block diagram of the ePix10k prototype (on the left) and the ePix10k final version (on the right).

2. EPIX PLATFORM ARCHITECTURE

Fig. 1 (right picture) shows a simplified block diagram of the ePix platform. The platform architecture is composed of an analog matrix of pixels. Columns are divided in 6 banks that are read out in parallel in order to speed up the readout. The architecture also features a control interface and all the required support electronics to perform configuration, calibration, and readout of the matrix. In Fig.1 (left picture) the intermediate (prototyping) design stage where ADCs per column are not present, the information from the pixels is read out by multiplexing the columns in a bank on a single analog output and this information is digitalized using an external ADC per bank. In the final stage, the output of all ADCs per bank will be serialized, encoded and transmitted on a single high speed LVDS link.

2.1 ePix10k Pixel Architecture

Fig. 2 shows a simplified block diagram of the ePix10k pixel. It contains a single-stage low-noise charge integrator with a pulsed reset, a first order non-linear programmable LP filter, a correlated double sampler (CDS) and a sample and hold stage followed by a column buffer.

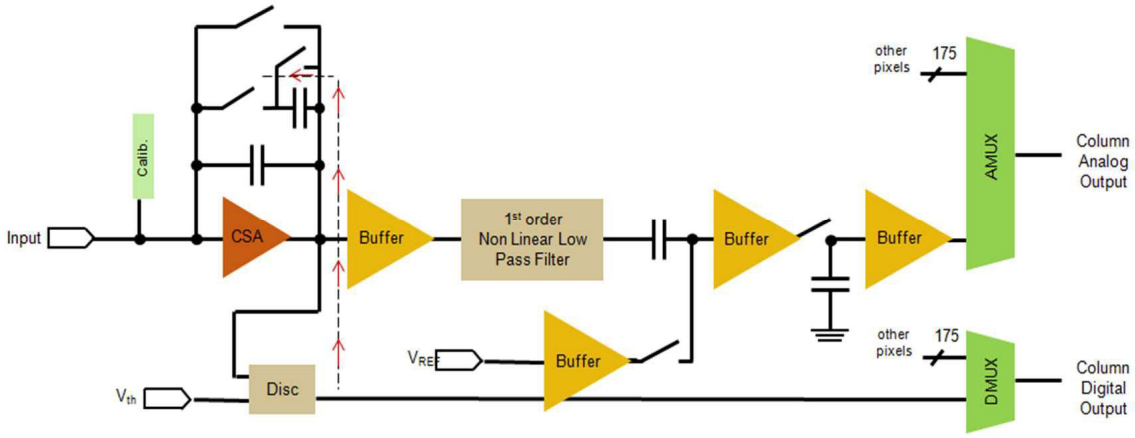
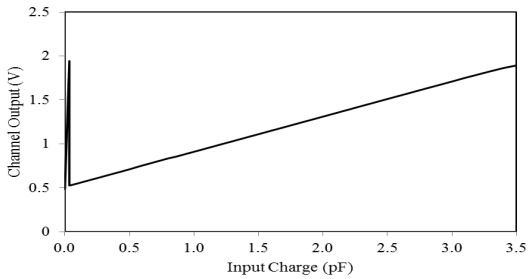
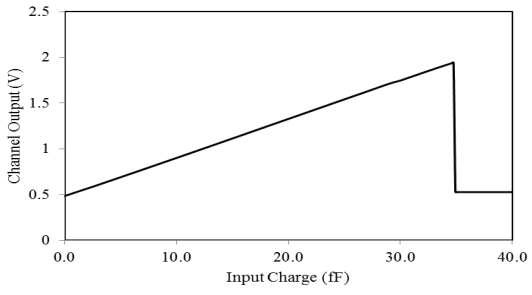


Figure 2. Simplified block diagram of the ePix10k pixel.

The low-noise preamplifiers are implemented using a folded cascode configuration. To minimize the impact of flicker noise, the input device is a PMOS transistor. In ePix10k the large signal range is the dominant requirement. Because of the limited power and speed of the preamplifier compared to the collection time in the sensor, large signals can produce transitory states leading to charge losses. A novel design approach has been used to avoid these phenomena and will be discussed at the meeting. To maintain sufficient resolution for small signals the ePix10k architecture implements multiple gain settings (fixed high gain or fixed low gain) and auto-ranging [7]. A simulated example of this implementation is shown in fig. 3. To increase the output range and to minimize non-linearity effects in the preamplifier response, an output stage using zero-threshold MOSFETs has been implemented in both designs. The 1st order LP filter is designed using active resistors to limit the area used. Active resistors are non-linear but are optimally sized to produce maximum filtering at low number of photons. The time constant of the filter is programmable by an internal DAC. The CDS stage is used to sample and store the filter output, purged from the fluctuations introduced by KTC noise, baseline fluctuations and to reduce low frequency noise. A "quasi-trapezoidal" noise weighting function can be implemented.



a)



b)

Fig. 3: ePix10k simulated transfer characteristic for the whole input range a) and a detail before the feedback capacitor switching b).

3. EPIX10K PROTOTYPE TEST RESULTS

The ePix10k prototype has been fabricated in TSMC CMOS 0.25µm technology. The image of the prototype chip is shown in Fig. 4.

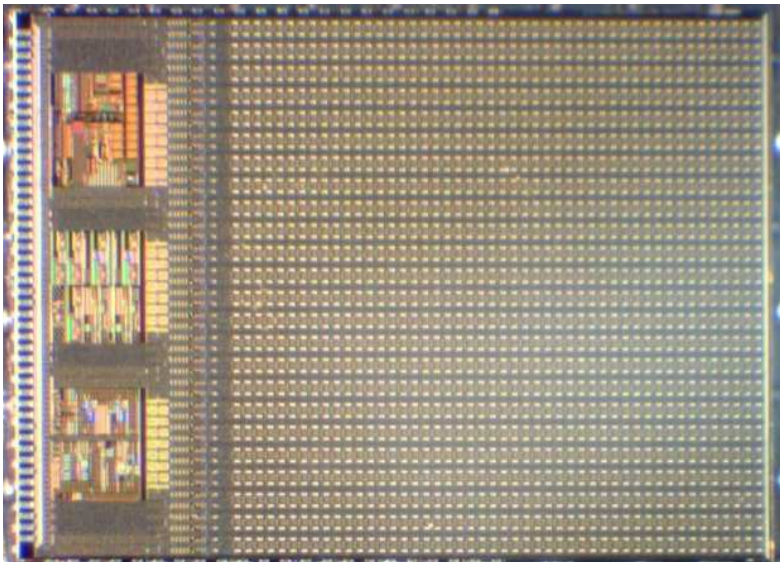


Figure 4. ePix10k prototype chip: 48x48 array of pixels with a measured ENC of 140e- r.m.s. and a signal range of 3.5pC (10k photons at 8keV).

The ASIC performance has been evaluated through a set of measurements. The first set is aimed to test the pixel response as a function of the input charge, as well as the linearity and the gain of the device. The response of a pixel is shown in Fig. 5. The transfer response was scanned using an internal 10-bit pulser, selectively injecting charge in the pixels. The measured results are in agreement with the simulated curves.

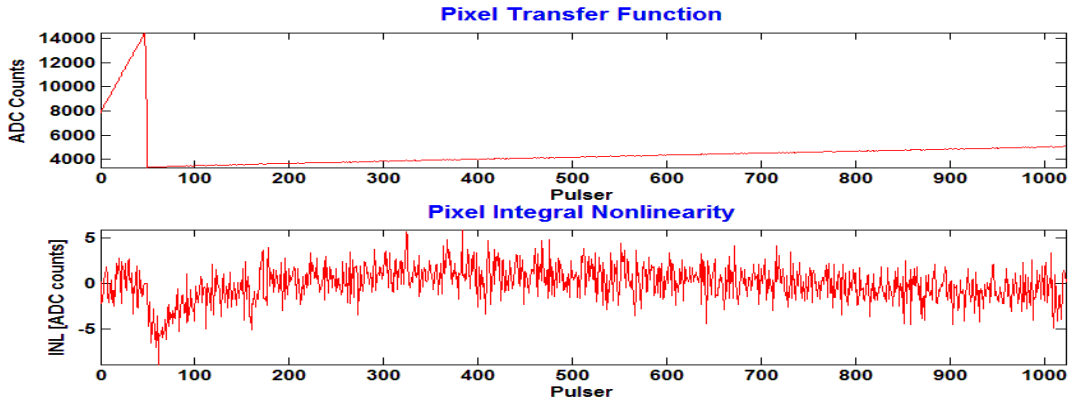


Fig. 5. ePix10k Prototype transfer characteristic measured using the internal calibration system based on a 10-bit programmable pulser.

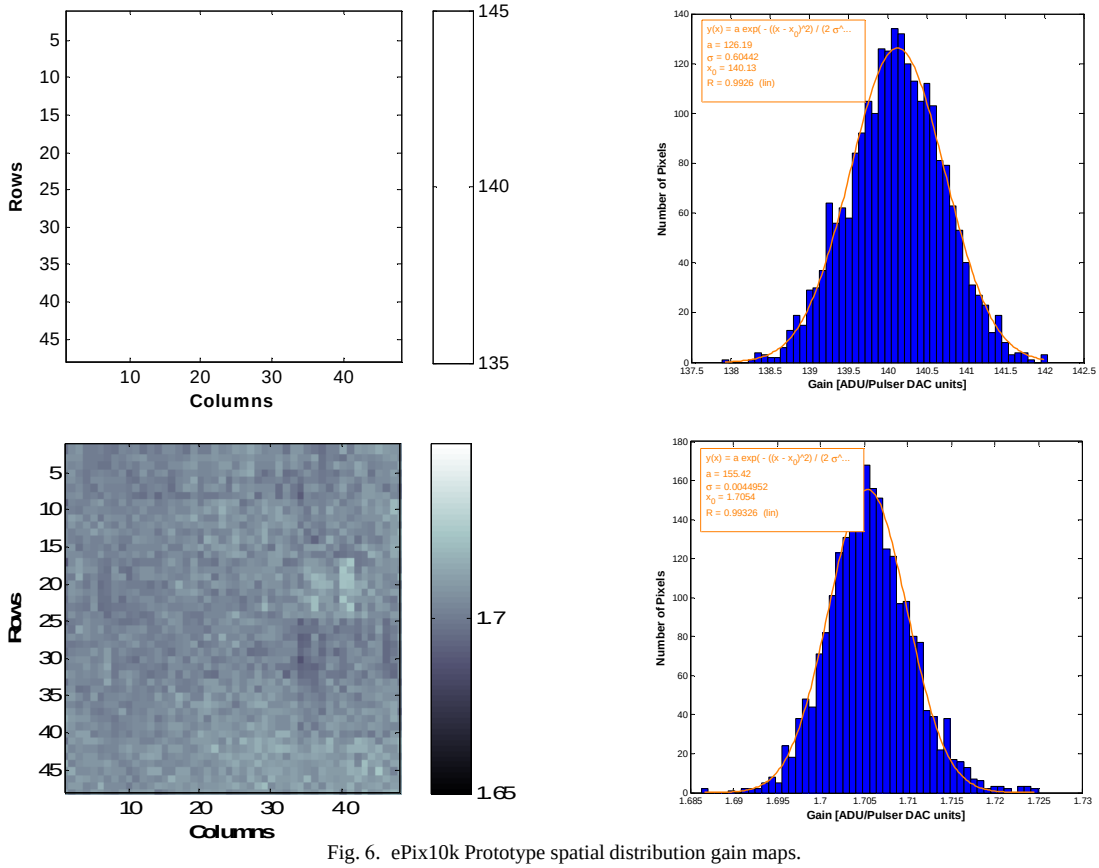


Fig. 6. ePix10k Prototype spatial distribution gain maps.

The gain spatial distribution using the auto-ranging feature is shown in Fig. 6. A good uniformity of gain across the full matrix is achieved in both high gain and low gain region. A gain dispersion of ~0.4% in high gain and ~0.3% in low gain has been achieved. The high gain value is 34mV/fC or 5.6µV/e- and the low gain value is 345mV/pC or 56nV/e-.

Fig. 7 shows a histogram of the cumulative noise distribution of the pixel output noise in ADUs. The standard deviation is about 6.7 ADUs that corresponds to an input referred noise of about 140e$^-$ (or a Signal to Noise Ratio of 18 for single photon at 8KeV).

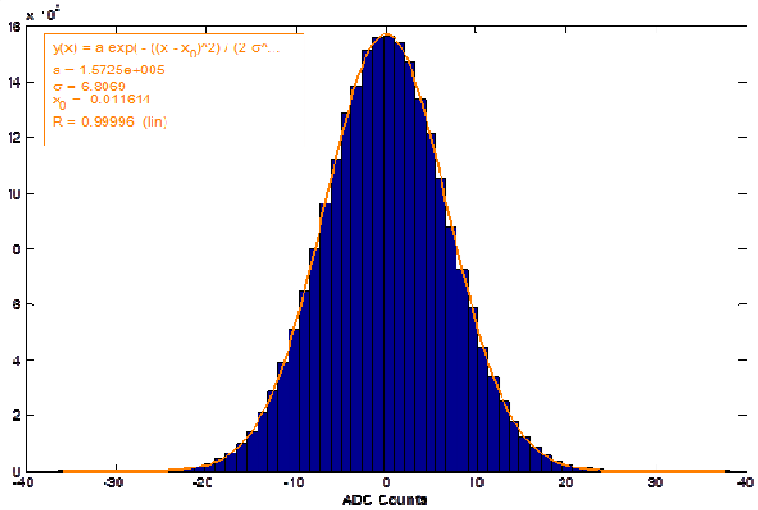


Fig. 7: ePix10k Prototype all pixels cumulative noise distribution.

4. CONCLUSION

A class of front-end ASICs based on a common platform has been designed to satisfy the demanding experiments at LCLS. ePix10k is the front-end ASIC tailored for high dynamic range applications. The 48x48 pixels prototype version has been characterized and the ASIC presents a noise floor of 140e^- r.m.s. at room temperature and it is suitable for applications with input signals up to 10k photons at 8keV. Gain and linearity error within 0.4% has been achieved.

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