LDAC September 15th 2014

ePix: a class of architectures for second generation LCLS cameras

A. Dragone*, P. Caragiulo, B. Markovic, R. Herbst, K. Nishimura, B. Reese, S. Herrmann, P. Hart, G. Blaj, J. Segal, A. Tomada, J. Hasi, G. Carini, C. Kenney, G. Haller

(* dragone@slac.stanford.edu)

U.S. DEPARTMENT OF ENERGY
Office of Science

RED Integrated Circuits Dept.

SLAC NATIONAL ACCELERATOR LABORATORY

Outline

- The ePix approach
  - ePix platform architecture
- ePix100 variant
  - Pixel design
  - 352x384 full reticle prototype performance
- ePix10k ASIC variant
  - Pixel design
  - 96x96 prototype performance
- Summary and conclusions

The ePix family:

	ePix100	ePix10k
Mode of Operation	INT	INT-with auto-ranging
Technology	0.25 µm	0.25 µm
Pixel size	50x50 µm²	100x100 µm²
Array	352x384	176x192
Full Size	Full Reticule	Full Reticule
Frame rate	120Hz (> 1kHz)	120Hz (> 1kHz)
Range	220ke-	22Me-
Effective ENC	<100e- (50e-)	<350e- (120e-)
FE Gain	6.5µV/e-	6.5µV/e-, 64nV/e-
Polarity	positive	positive
Filtering	LP + CDS	LP + CDS
S/N	40	8.8
DC Power cons.	~ 10µW/pix	~ 10µW/pix
Power pulsing	Yes	Yes
PP Power cons.	~ 5µW/pix @ 120Hz	~ 5µW/pix @ 120Hz

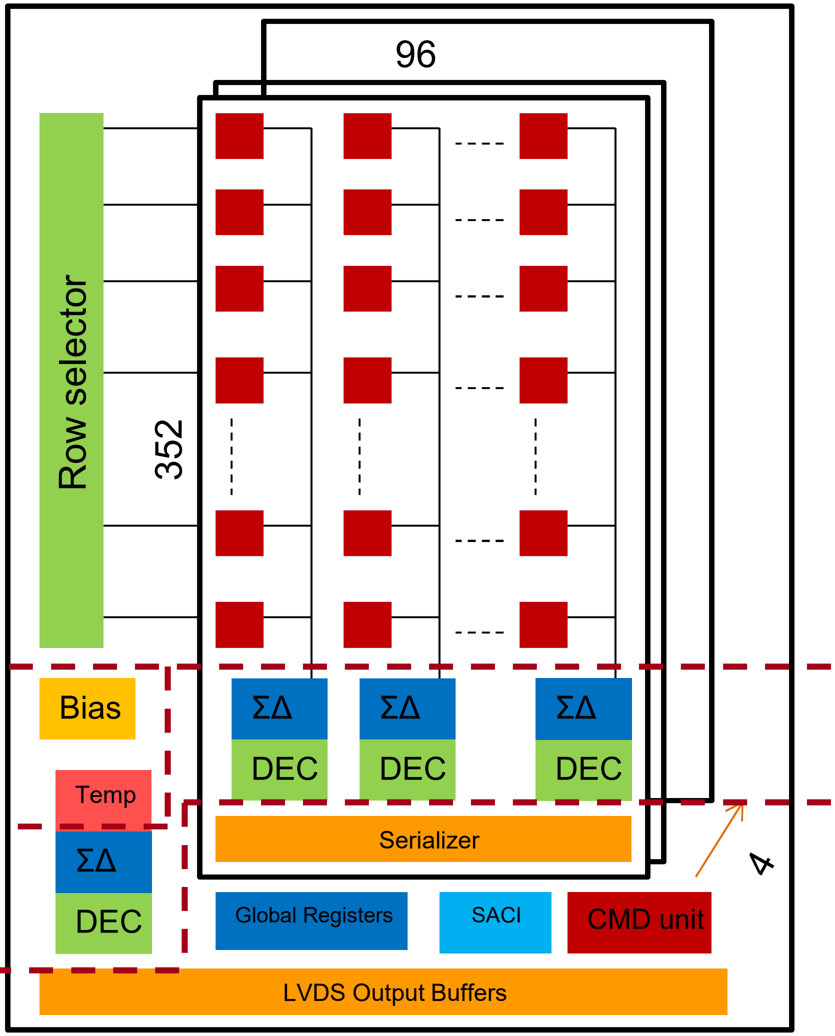
Pixel Matrix: fully analog.
Different designs for each detector variants

Balcony (ePix platform):

Analog BE:
- Bias
- Provides Calibration and Monitoring support

Mixed Signal BE:
- Performs Analog to Digital Conversion

Digital BE:
- Controls Configuration
- Controls Acquisition and Readout
- Serialize digital data



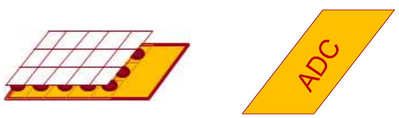
ePix(A) intermediate step – status of the project

To mitigate risks and to bridge the gap of the development time and intermediate version of ePix using external ADC

ePix design phases:

ePix (P) - minimum area matrix prototypes with analog balcony

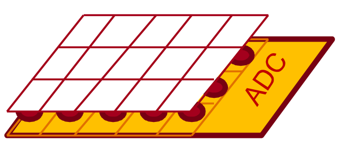
ePix100p designed, fabricated tested
ePix10kp designed, fabricated tested



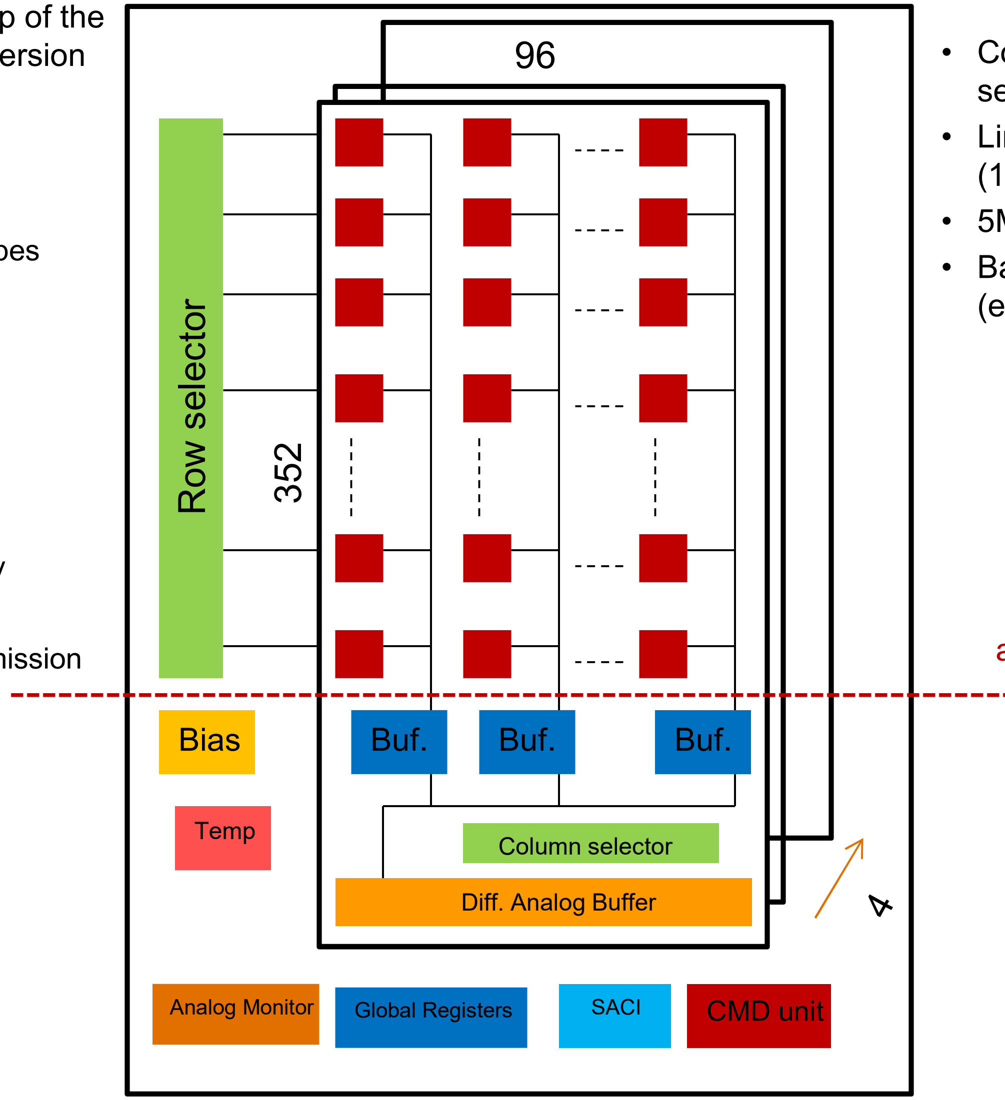
ePix (A) – final size with analog balcony

ePix100a designed, fabricated tested
ePix10ka designed and ready for submission

ePix (F) - full matrix with digital balcony

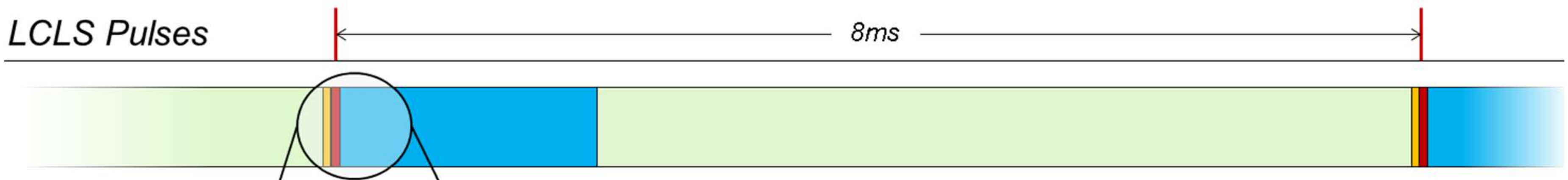


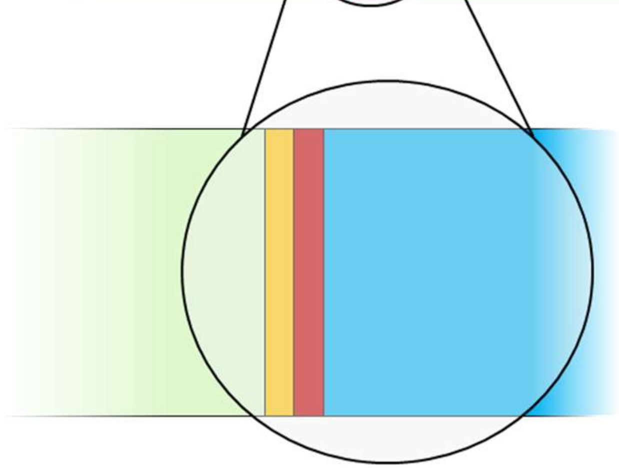
Digital balcony in design



- Columns are read sequentially
- Limited read-out speed (120-240Hz)
- 5MHz clock required
- Back-end noise limited (ePix100a)

ePix phases of operation





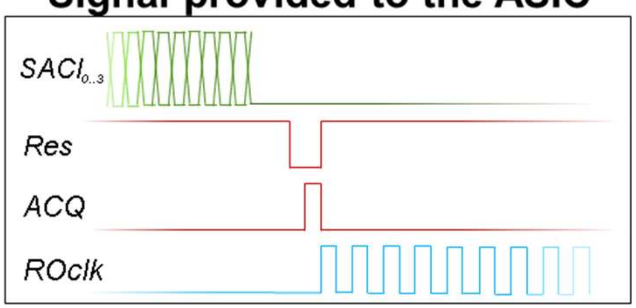
Idle/Configuration phase: non vital resources kept in power saving mode

Wake up phase: all resources get ready to run

Acquisition phase: analog processing in pixels active, no digital activity (balcony in power saving mode)

Readout phase: matrix readout A/D conversion, data serialization and transmission (non vital pixel analog blocks in power saving mode)

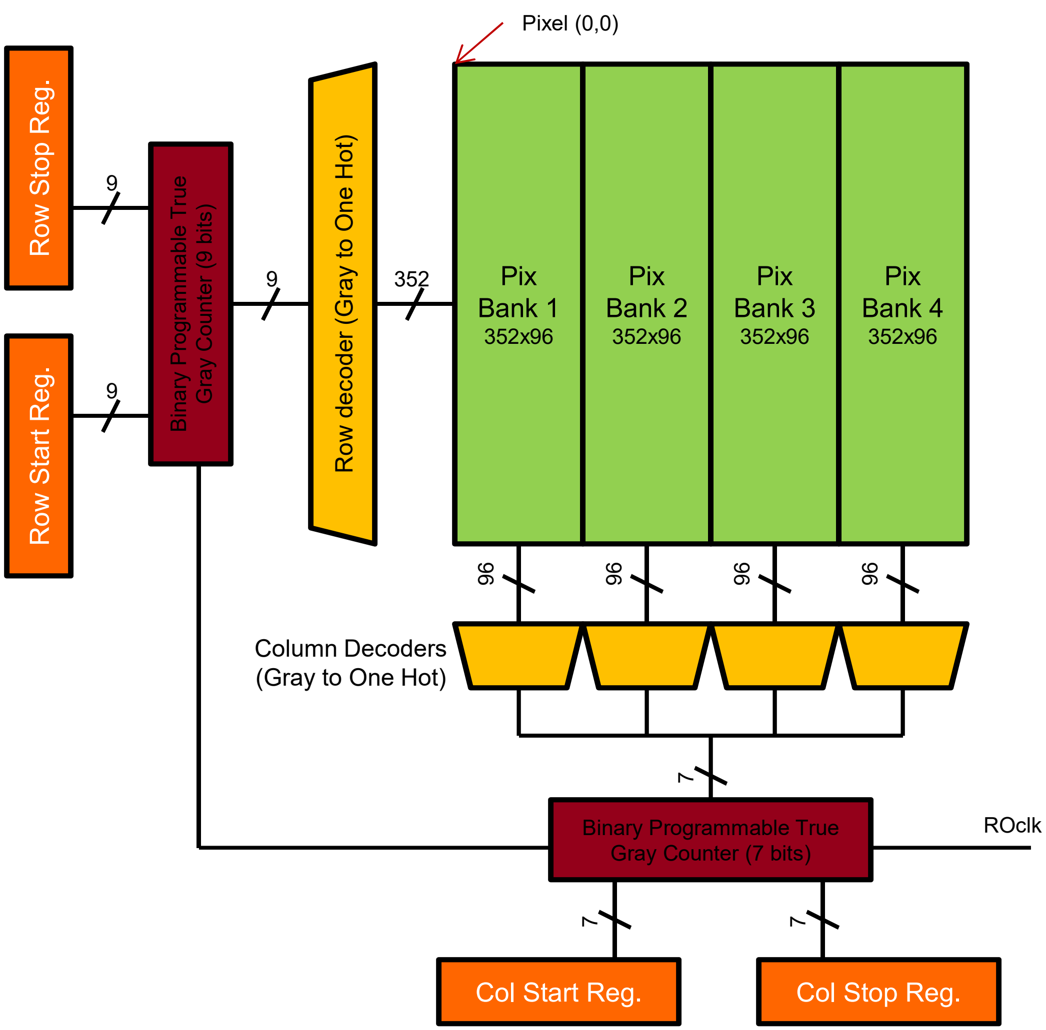
Signal provided to the ASIC



During Configuration only 4 digital signals are used.

During Acquisition and Read Out only 3 digital signals are used.

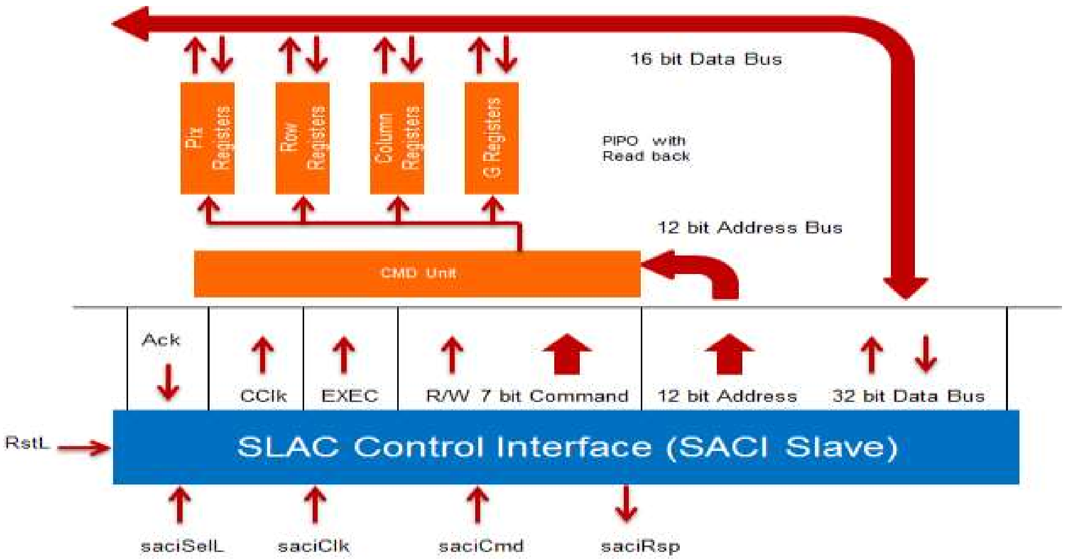
ePix pixel matrix access protocol



Pixel Matrix with Random Access

- In configuration phase a command unit pushes addresses into the counters providing access to the pixels. Single rows or columns can also be accessed in parallel as well as the full matrix
- In acquisition phase the row counter (both in the ver. A) scan the matrix in a windows defined by the addresses stored in the Rows and Columns start and stop registers

SLAC ASIC Control Interface (SACI)



Master/Slave Serial Interface

4 Signals

- 3 shared: saciClk, saciCmd, saciRsp
- 1 dedicated select line per slave: saciSelL

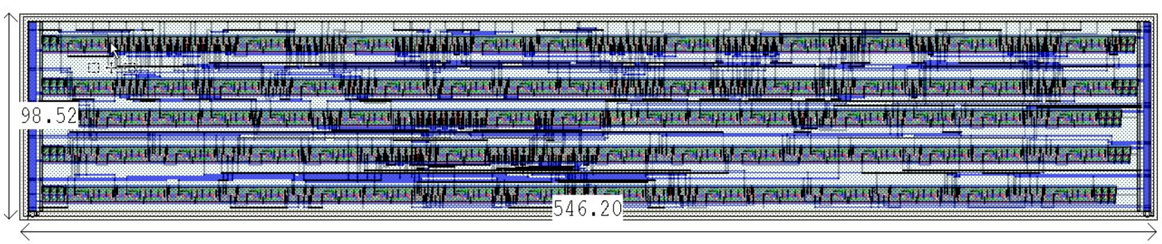
Allows multiple slaves on same SACI bus. (Similar to SPI.)

Motivation

- Need simple serial interface to ASICs for configuring registers and sending commands.

Standard Options Not a Great Fit

- SPI: No backpressure. No way for ASIC to signal that it is done with a command or ready for new data. Requires polling.
- I2C: Backpressure possible through clock stretching, but complex protocol and implementation.



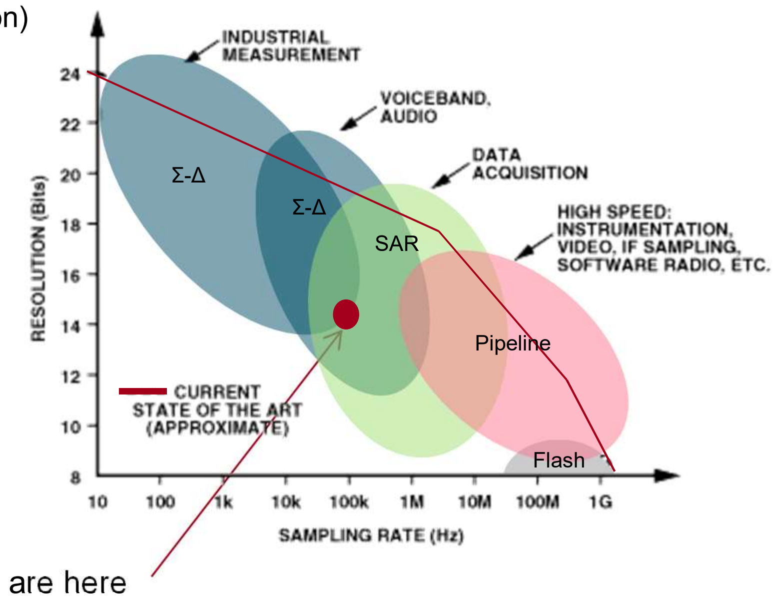
- 320 Standard Cells
- 98.52 µm x 540.20 µm

Why sigma delta?

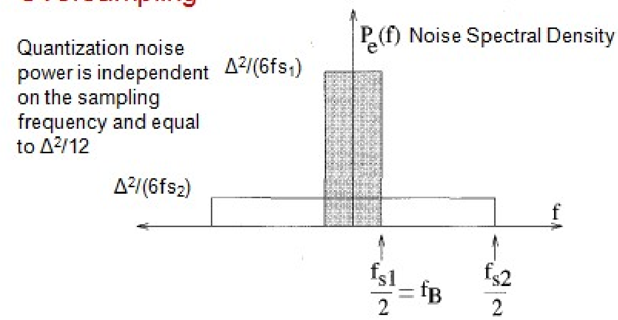
Optimal ADC architecture is a compromise among sampling rate, resolution, digital multiplexing, serialization rate and development time

Sigma-delta present several advantages:

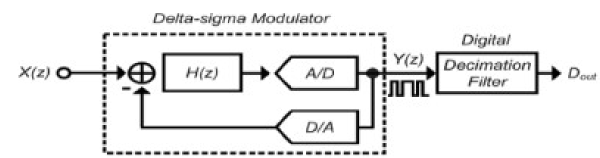
- They are compatible with frame rates of 500-1kHz required by the application
- Allow trading resolution for clock speed (oversampling ratio). Different pixel variants may require different resolutions
- They provide noise shaping
- Have a pseudo-random nature which reduces cross-talk effects between channels
- Require low precision analog blocks and have simple implementation (small area)
- Have potential for upgrades in more advanced technologies (heterogeneous integration)

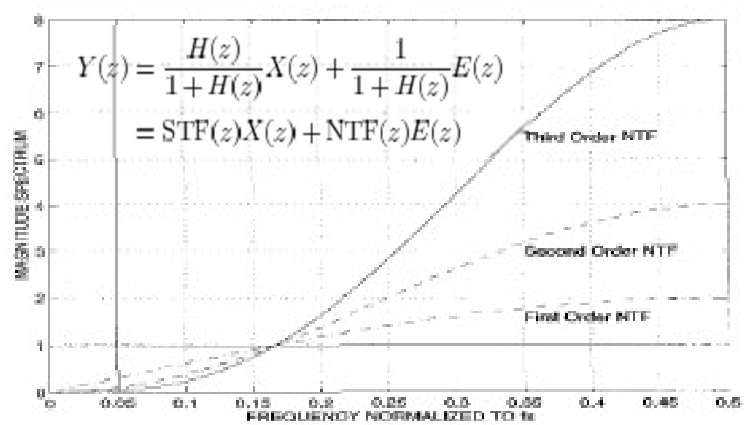


Oversampling



Noise Shaping





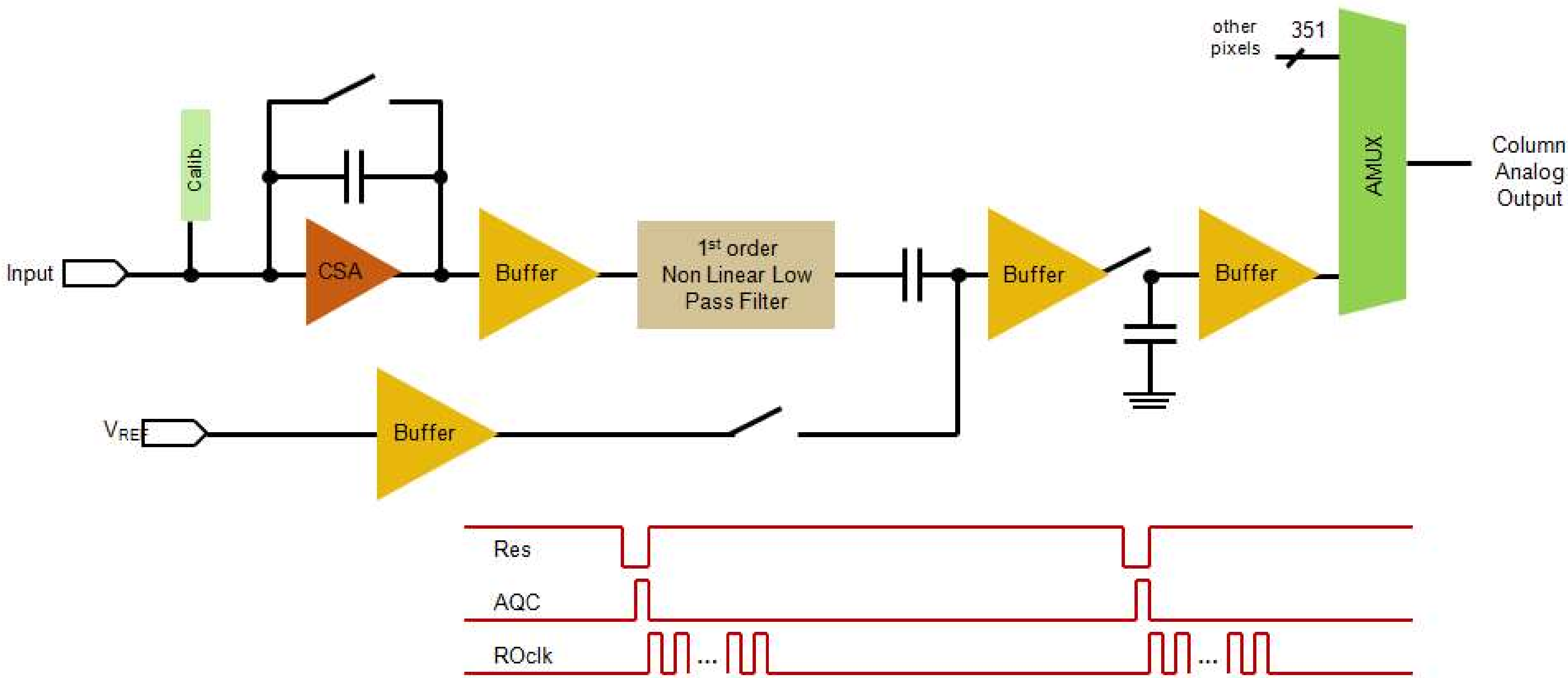
ePix calibration, compensation and monitoring

"Any detector is only as good as it's calibration" *S. Gruner*

- Gain calibration (per pixel)
  - charge can be injected in each single pixel or group of pixels. A 10-bit DAC can set the amount of injected charge in constant or automatic scan mode.
- Frame common mode tracking (In frame)
  - at the end of each frame the baseline and the max charge values are digitized on each column. This feature provides the possibility to track baseline shifts.
- Temperature tracking and compensation
  - a temperature variations compensation scheme is present.
- Analog and Digital monitors
  - critical internal nodes can be monitor during debugging and to check the correct functioning during operation

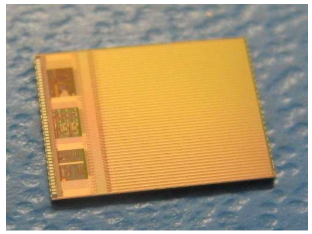
ePix100 pixel architecture

Signal Sampling Phase: Res is Low, AQC goes Low

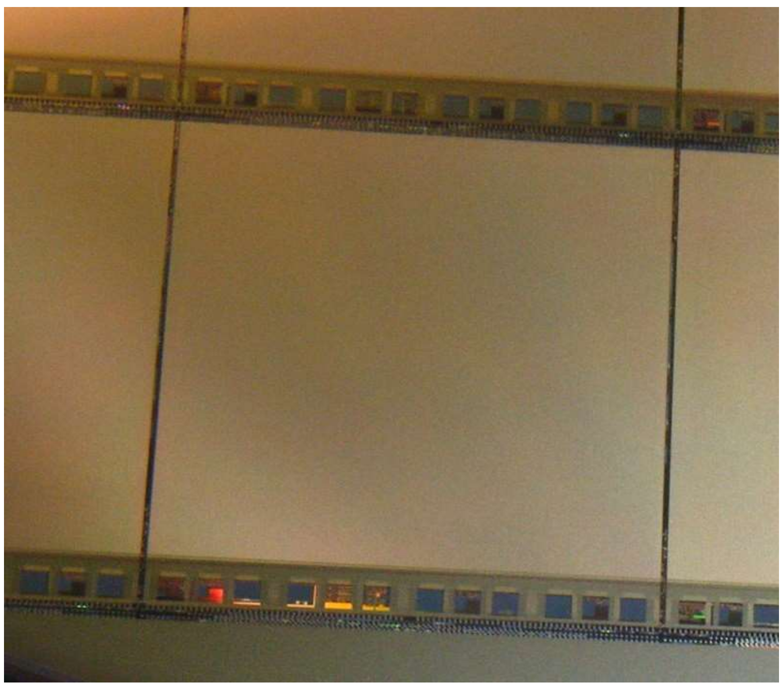


ePix100a prototype

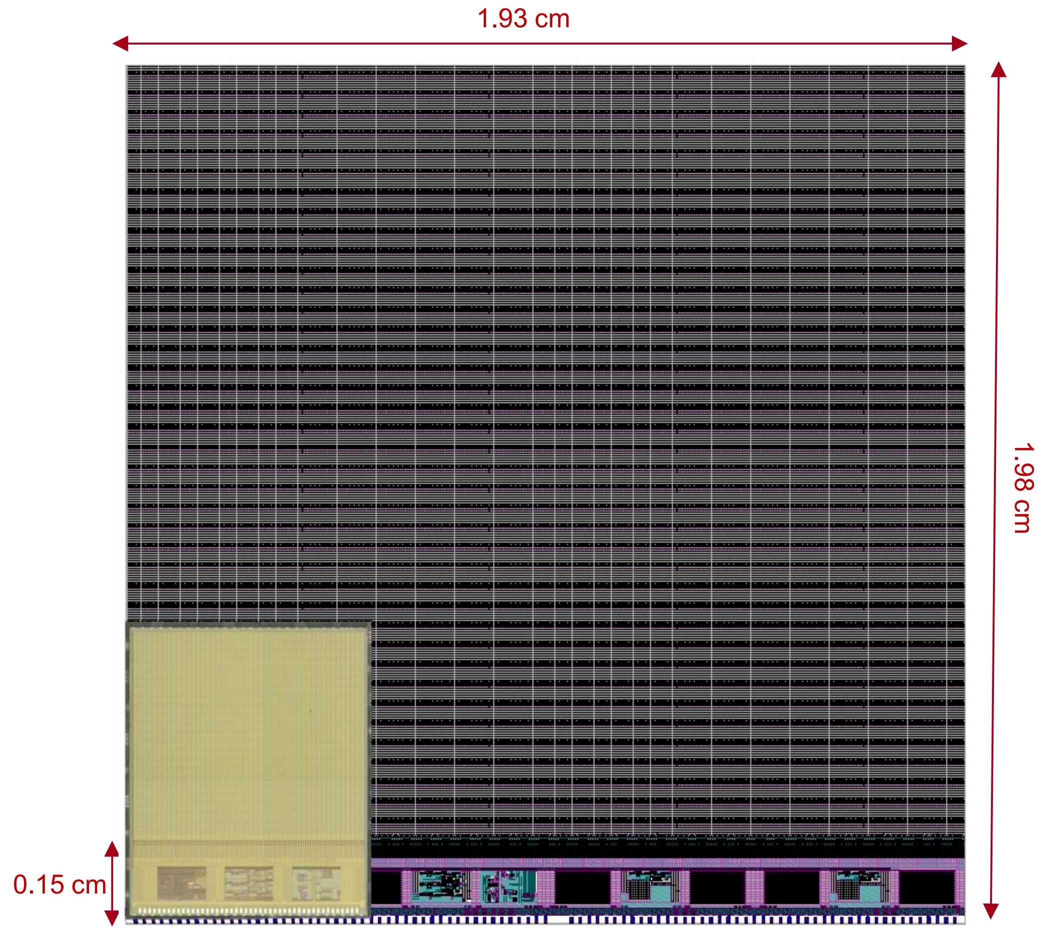
Presented last year
ePix100p prototype 96x96 pixels



ePix100a full reticle 352x384 pixels

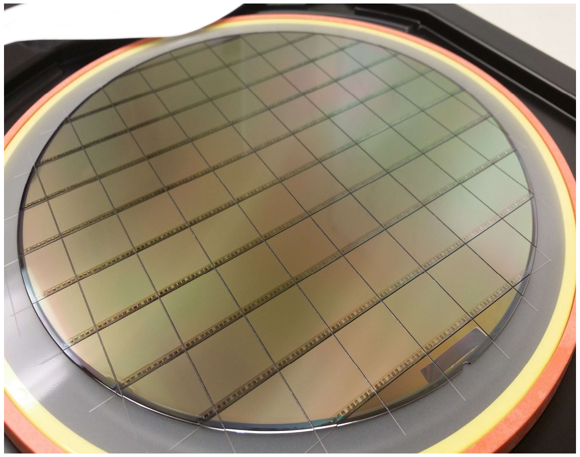


The layout of ePix100a



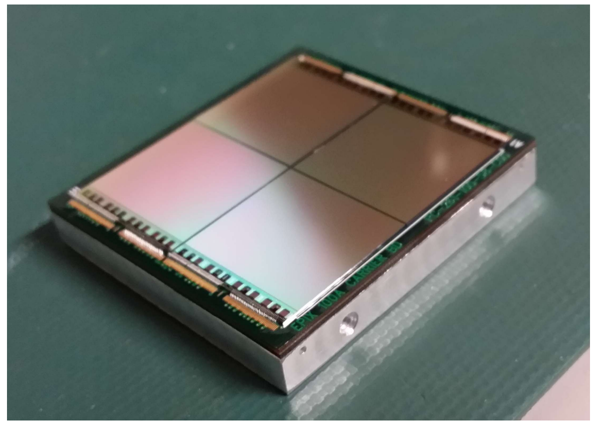
ePix100a pixel layout 50µm x 50µm

ePix100a prototype 352x384 pixels

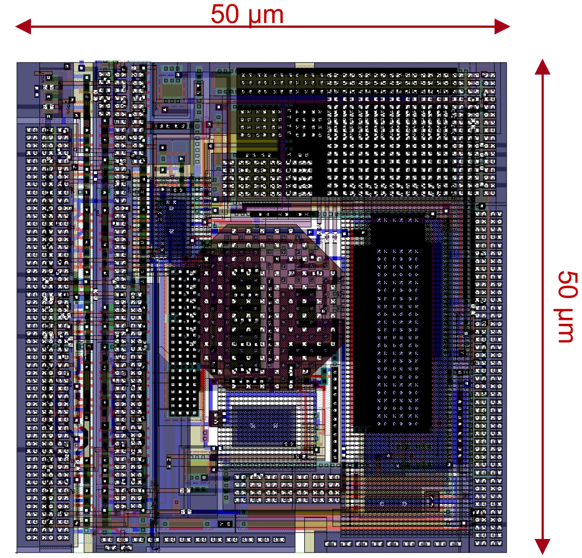


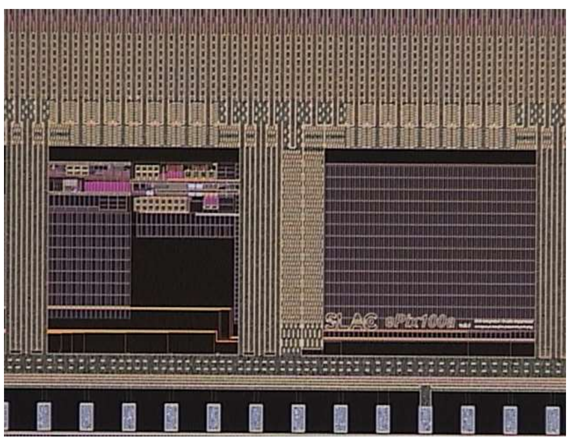
ePix100a wafer

~ 28 million transistors

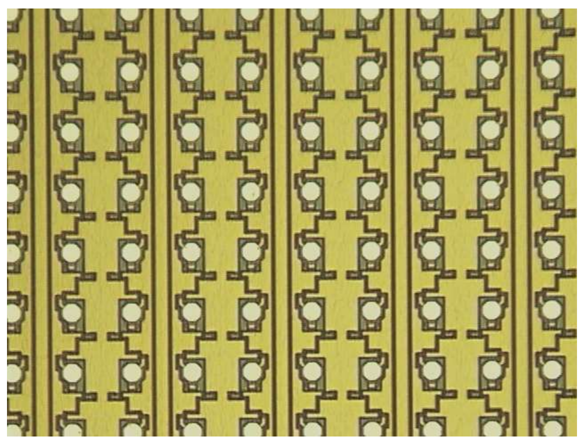


ePix100a 2x2 assembly

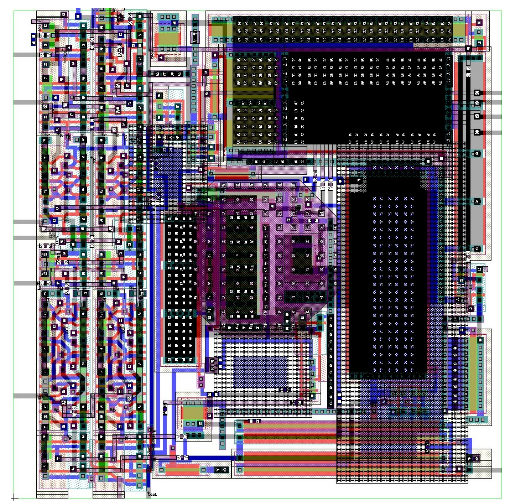




ePix100a balcony close up

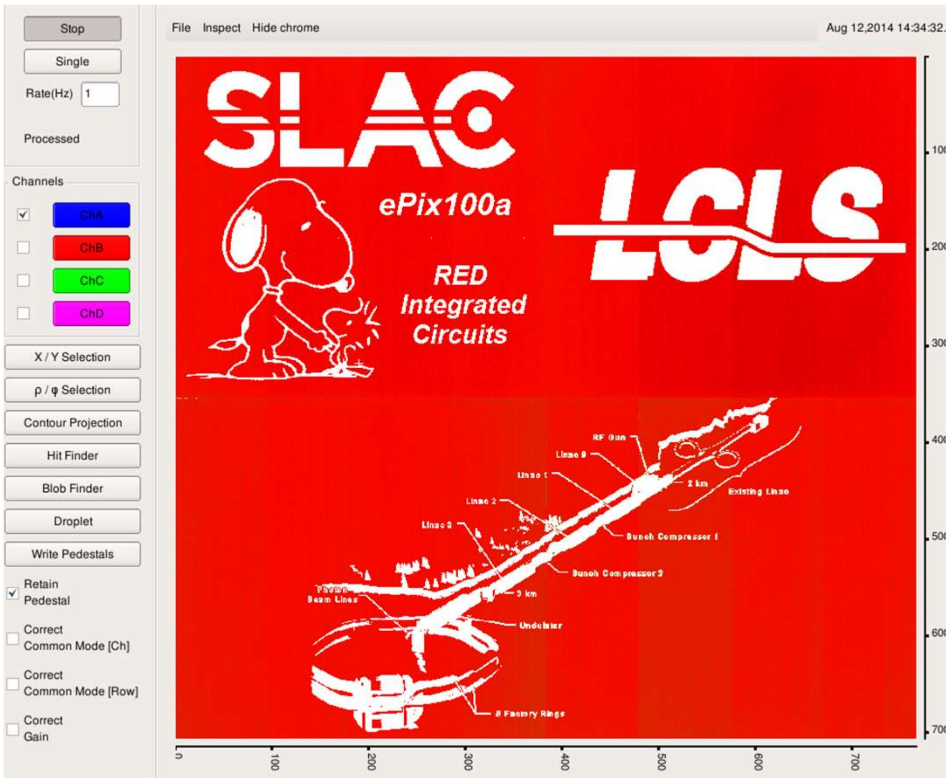


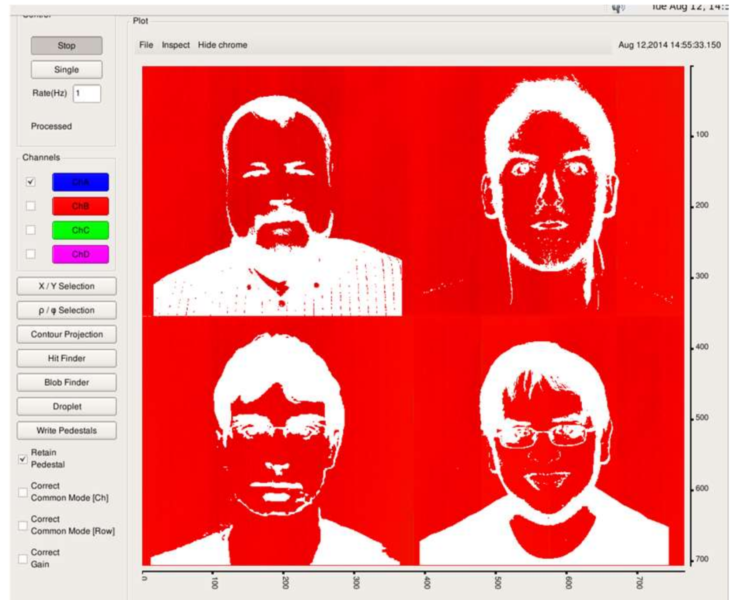
ePix100a pixel close up



ePix100a pixel layout

ePix100 prototype: functional test

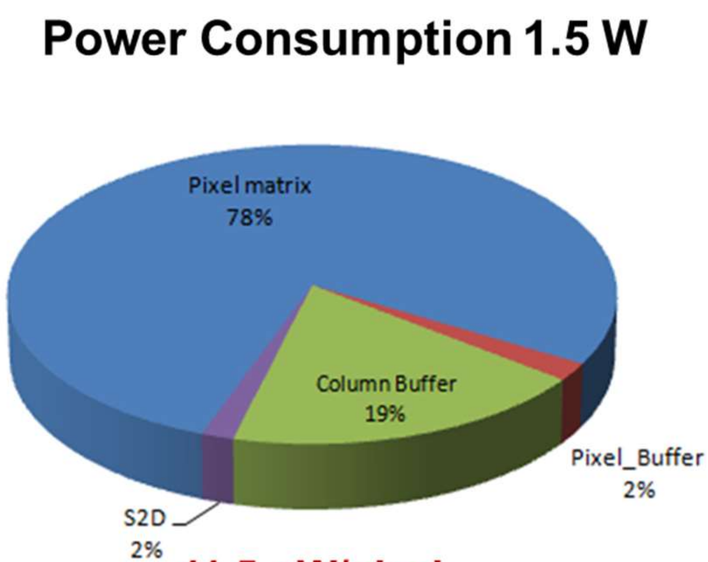




ePix100a with some pixel injected using the automatic scan mode based on the internal pulser. The pulser injects in every frame an increased amount of charge in the selected pixels up to the full scale (100Ph @8keV).
The interesting aspect of these pictures is that all functionalities of the ASIC are used demonstrating the device is fully working.

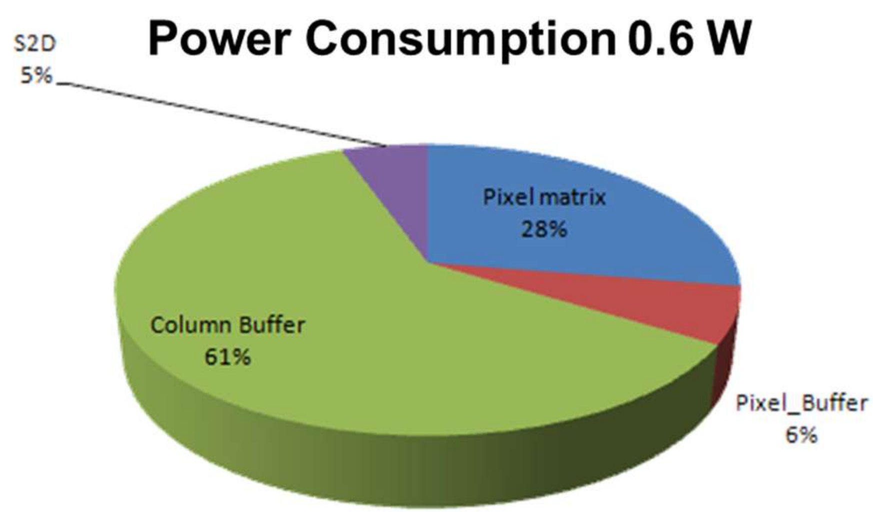
ePix100a measured power consumption

DC mode



11.5 µW/pixel

Power pulsed mode

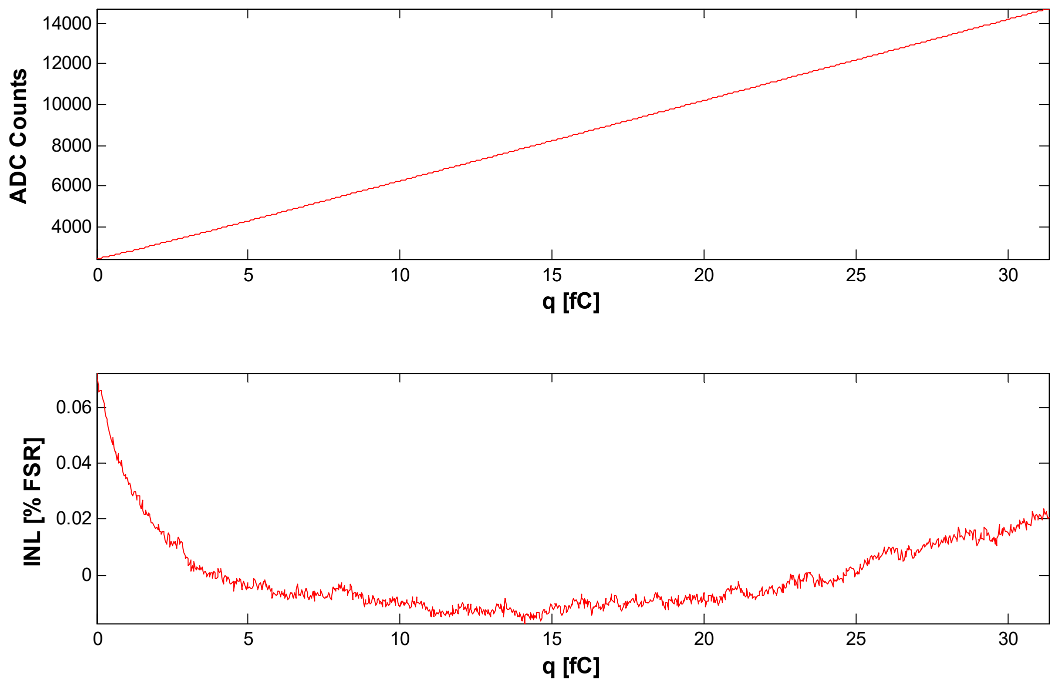


5 µW/pixel

@ 120Hz and with a the optimum integration time of 36µs

Eiger	8.8µW/pixel
Timepix3	14µW/pixel
Medipix3	9µW/pixel
FEI4	10µW/pixel

ePix100a pixel linearity and gain measurements



	Min. Required	Simulated	Measured
Gain	35mV/fC	42mV/fC	38.2mV/fC
Non-Linearity	< 1%	~0.1%	~0.1%

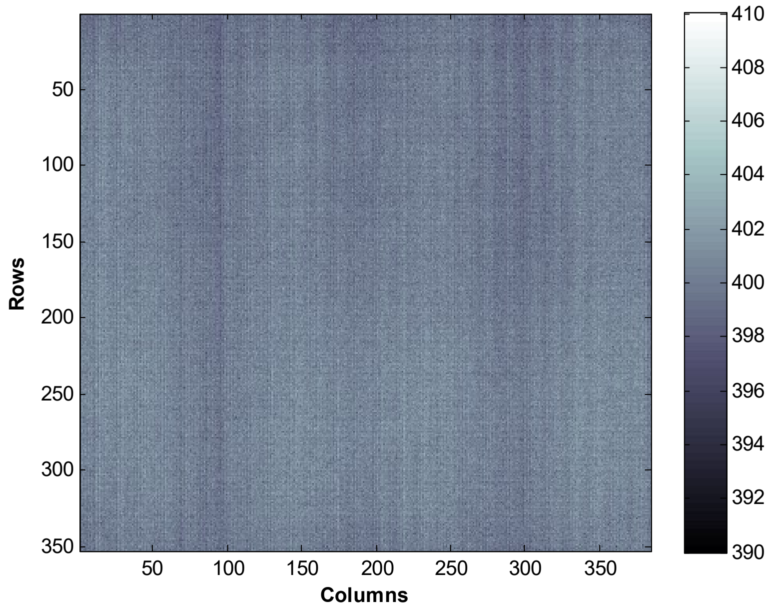
Gain slightly lower than nominal. Compatible with parasitic capacitances around the feedback capacitor:

Nominal Cf = 24fF

Measured equivalent Cf = 26.2fF

ePix100a gain uniformity measurement

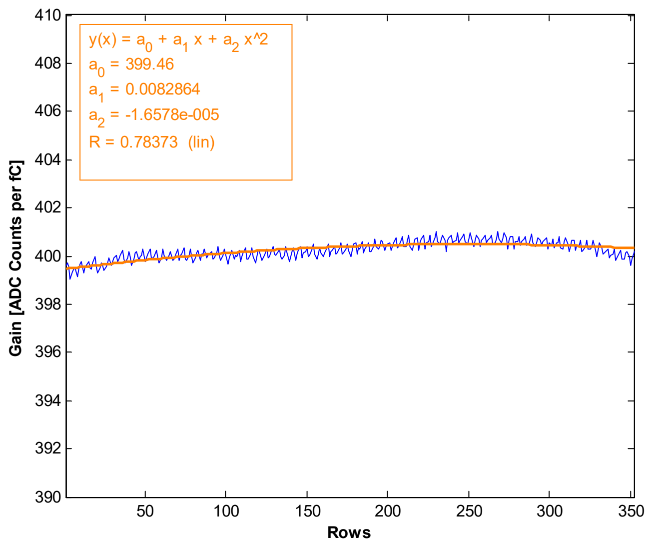
ePix100a gain map

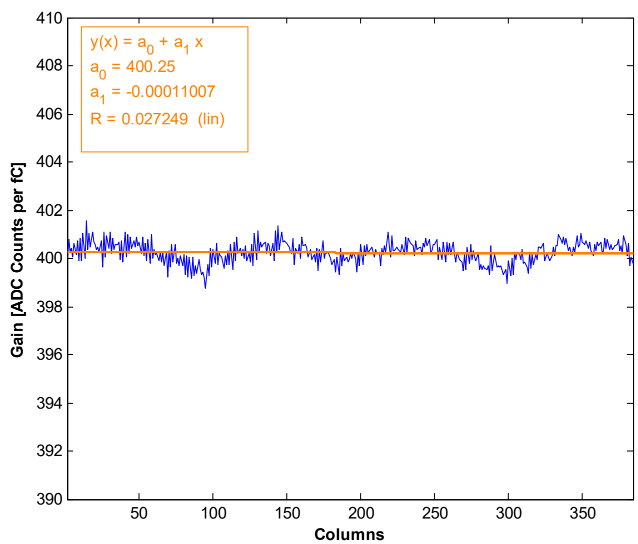


Good Uniformity of gain across the full matrix is achieved:

Flatness across rows < 2count/fC i.e. max 0.5%

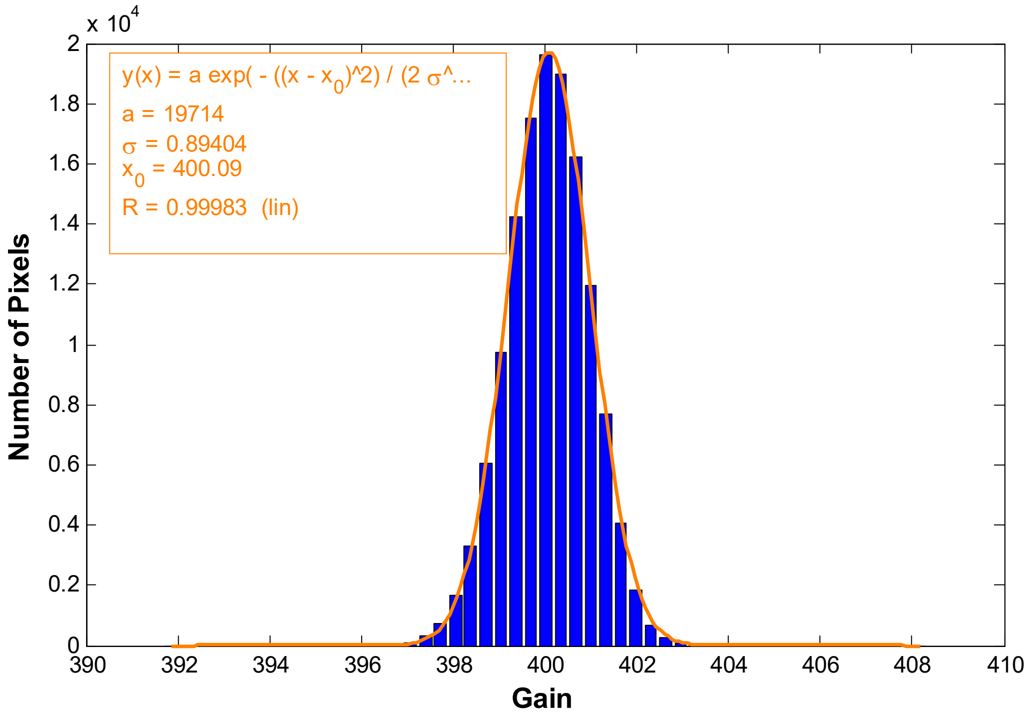
Flatness across columns < 2count/fC i.e. max 0.5%





ePix100a gain uniformity measurement

SLAC

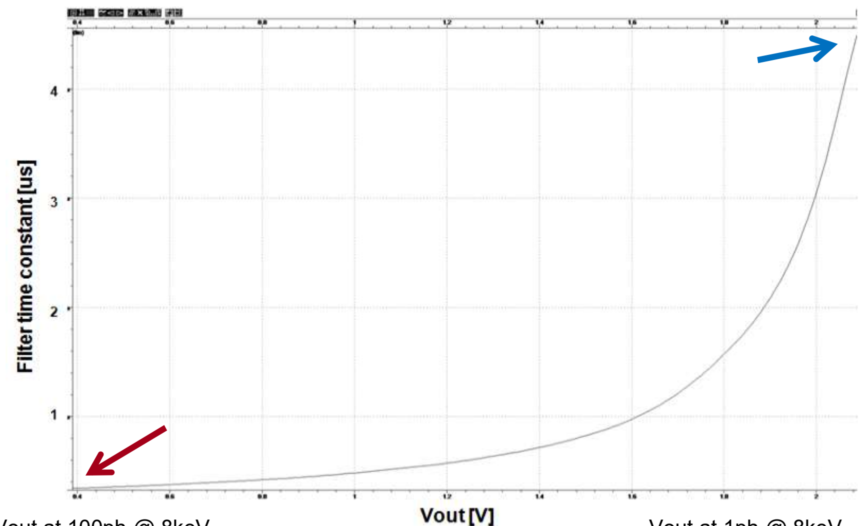


Overall gain distribution and dispersion:

Gain dispersion of 0.9 count/fC is achieved i.e. ~0.2%

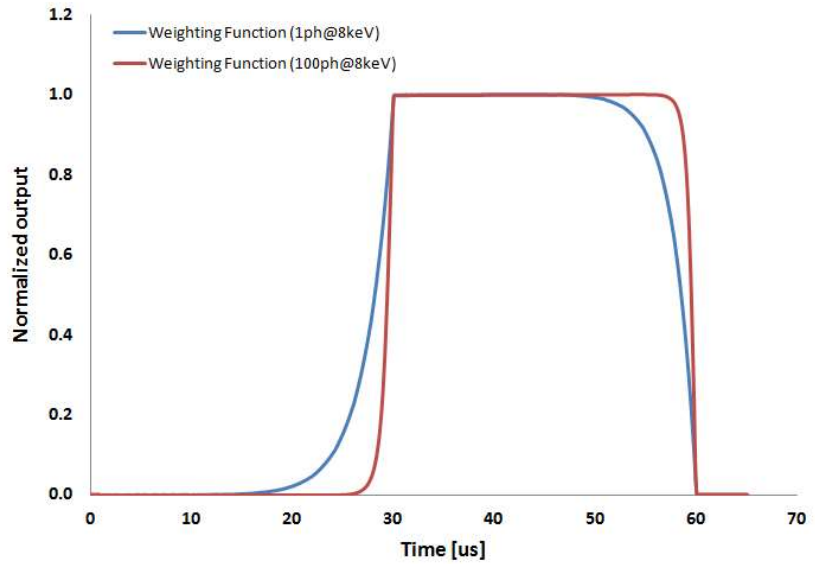
The result is compatible with the typical dispersion of 24fF MIM capacitors and expected gain variations in the pixel analog chain

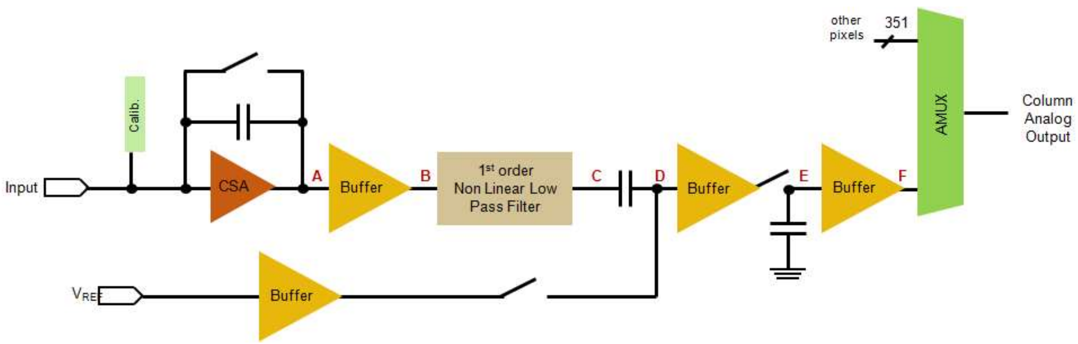
ePix100 filter behavior



Vout at 100ph @ 8keV

Vout at 1ph @ 8keV

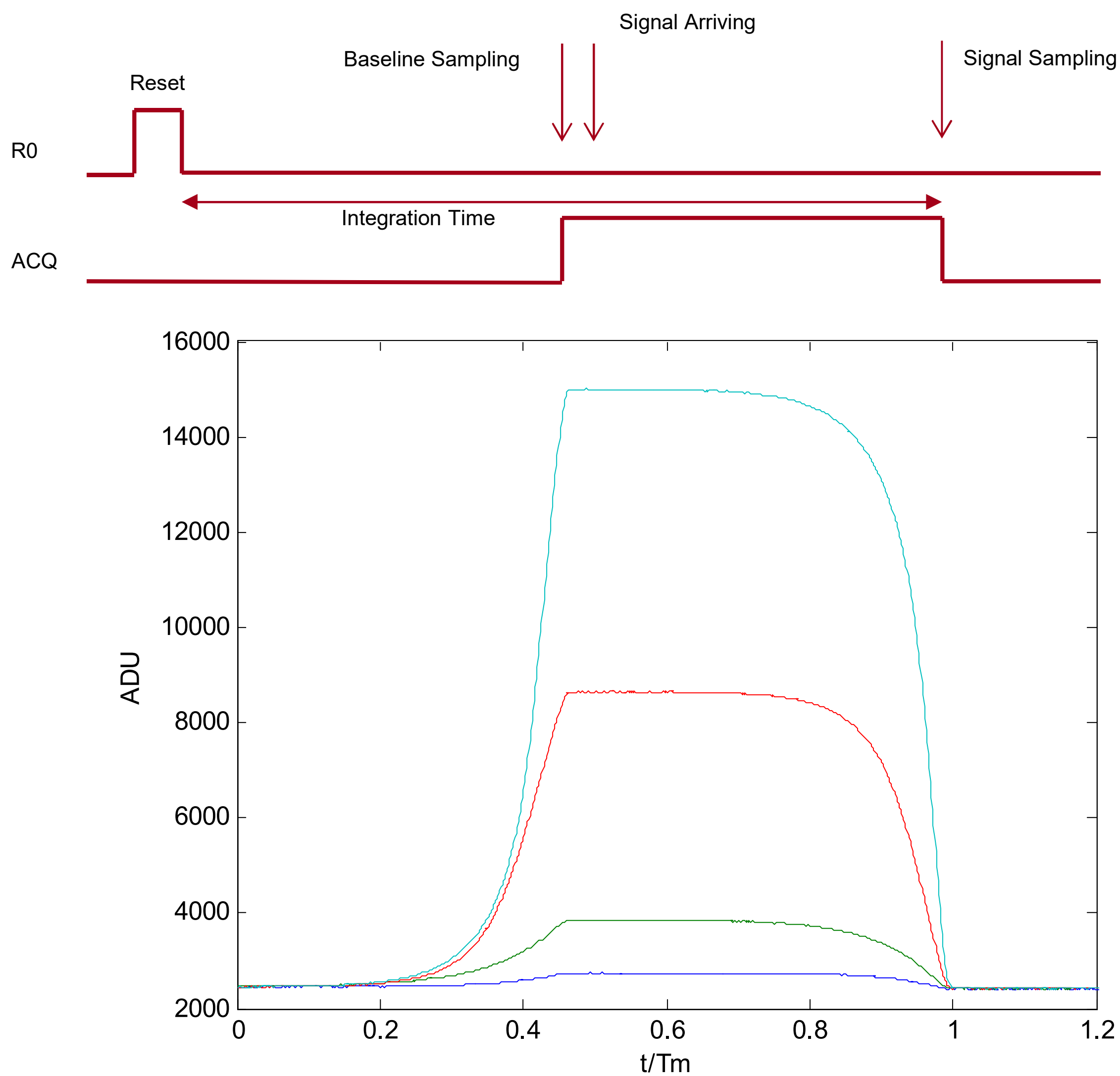




ePix100a noise weighting function

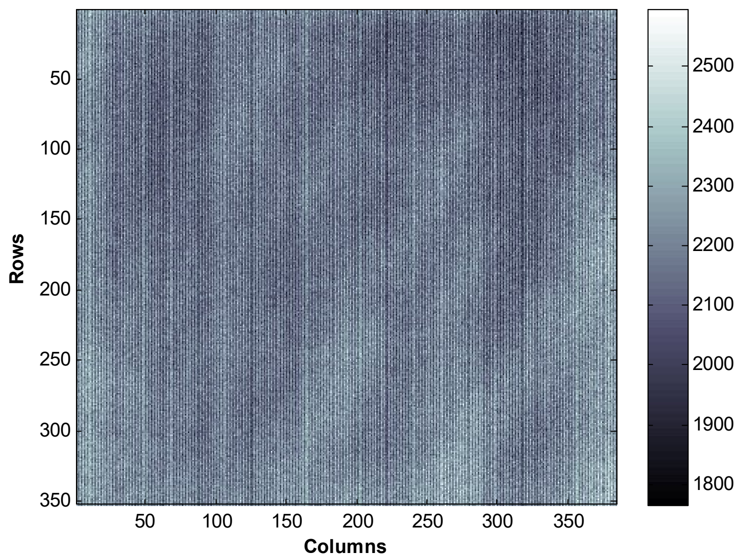
Filter response at different injection levels: The time constant is maximum at minimum signal (equivalent to 1Ph at 8keV) and it decreases with the injection level.

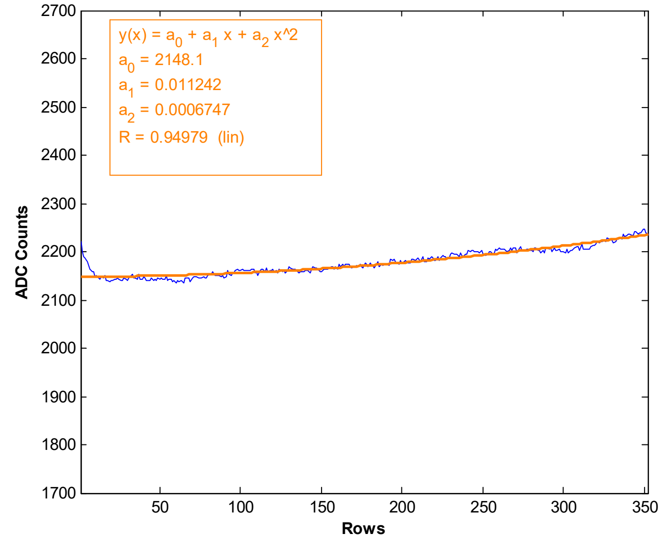
The maximum measured time constant is about 4.5us as expected from simulations

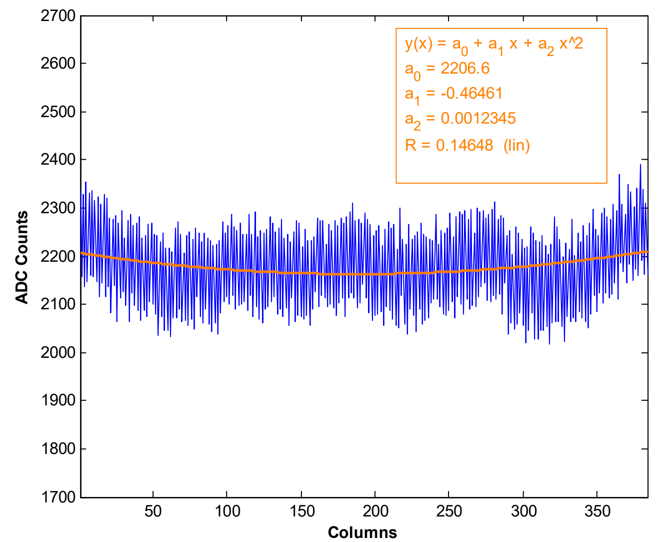


Dark frame uniformity: fixed patterns

ePix100a dark frame (1000 frames averaged)







Fixed pattern noise is visible across columns as expected considering the layout arrangement of the pixels in the matrix (groups of 16 with mirror image every column)

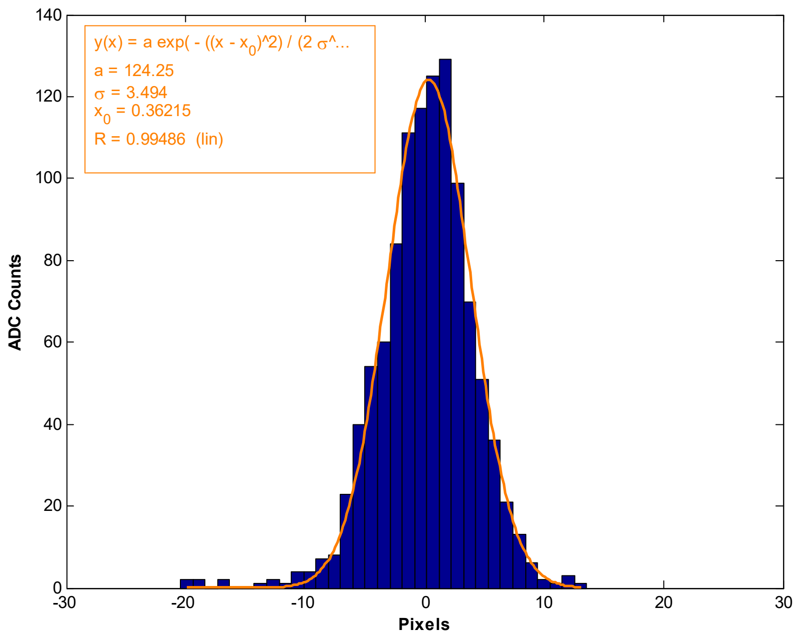
Good flatness of the dark field is achieved:

Flatness across rows < 50 counts i.e. max 2.3%

Flatness across columns < 50 counts i.e. max 2.3%

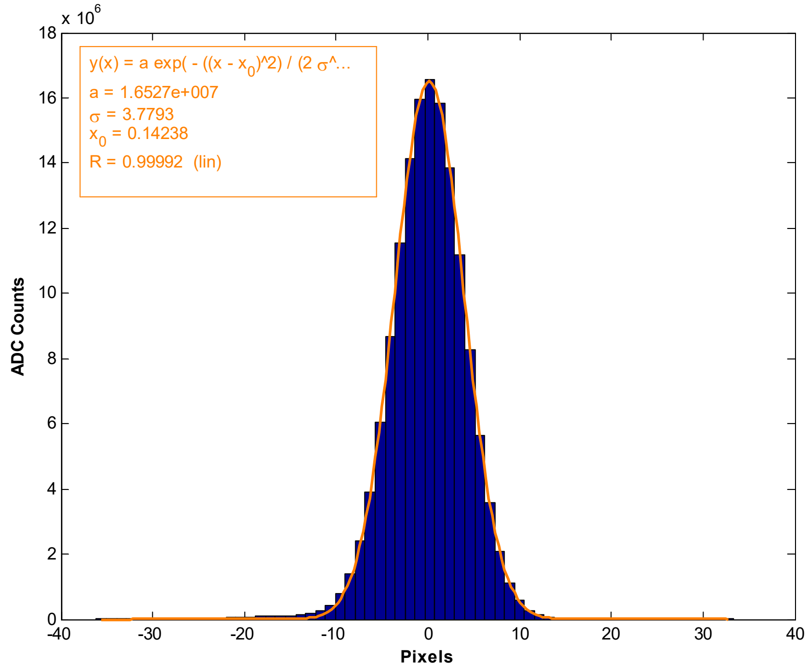
ePix100a noise performance

Best pixel *(or as somebody say "typical" pixel)* noise distribution



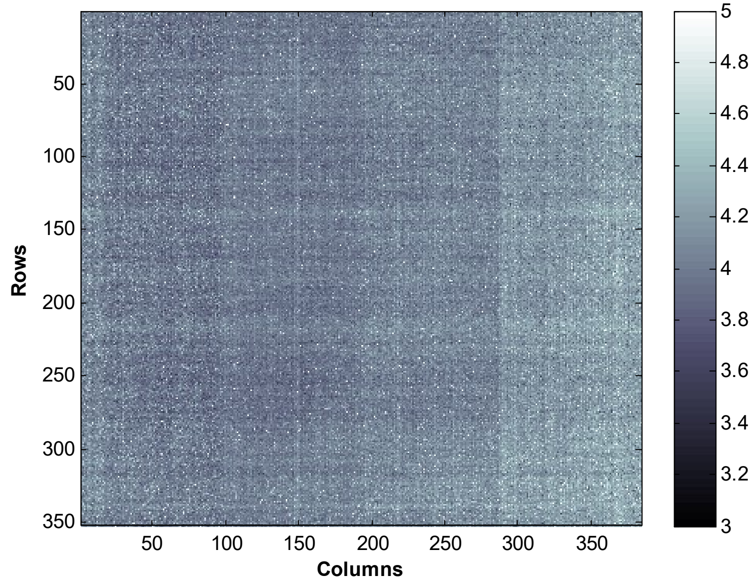
a sigma of 3.8 counts r.m.s. is equivalent to about 55e- r.m.s. i.e. a S/N ratio of 40 for single photon at 8keV

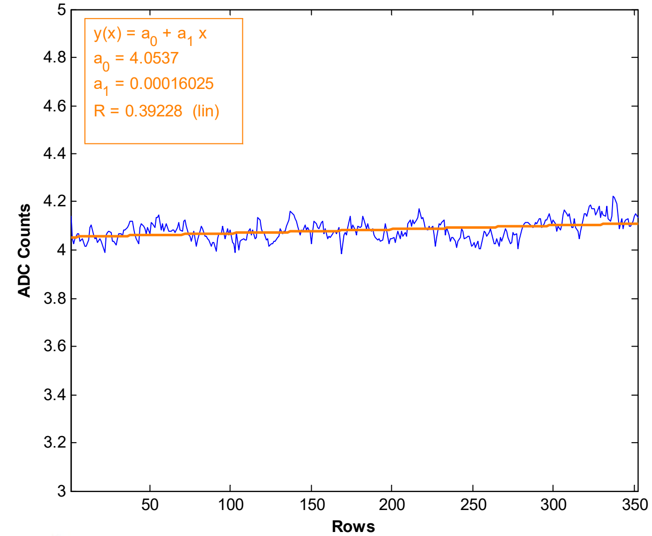
All pixels cumulative noise distribution

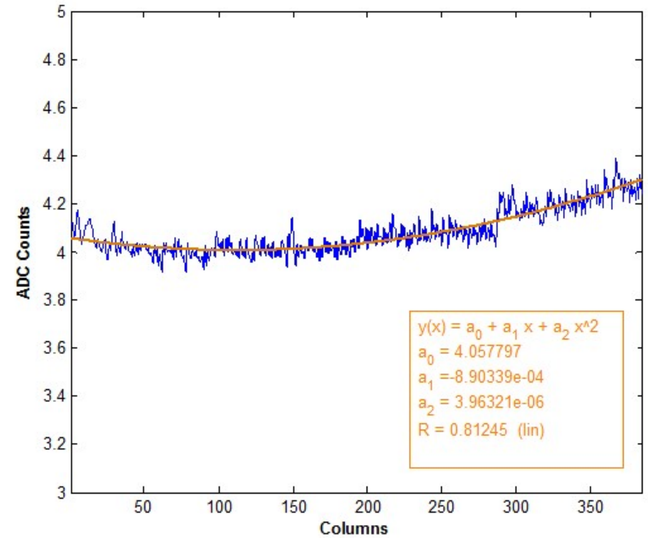


ePix100a noise uniformity

ePix100a noise (dark frame subtracted)







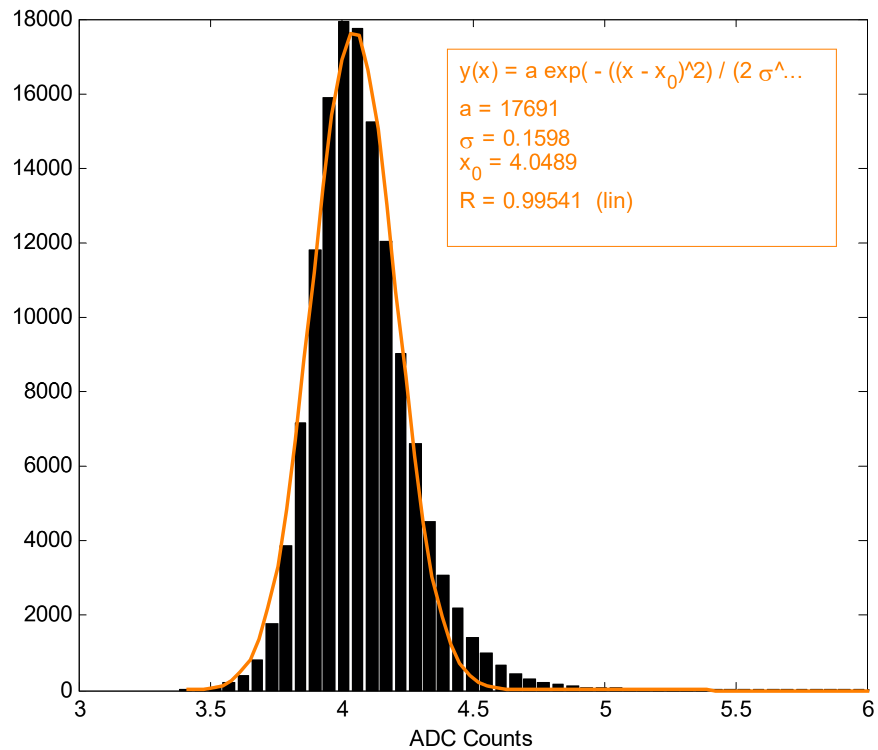
Good noise uniformity across the full matrix is achieved:

Flatness across rows < 0.1 count i.e. max 2.5%

Flatness across columns < 0.2 count i.e. max 5%

ePix100a noise uniformity

Distribution of the pixel noise (r.m.s.) across the matrix

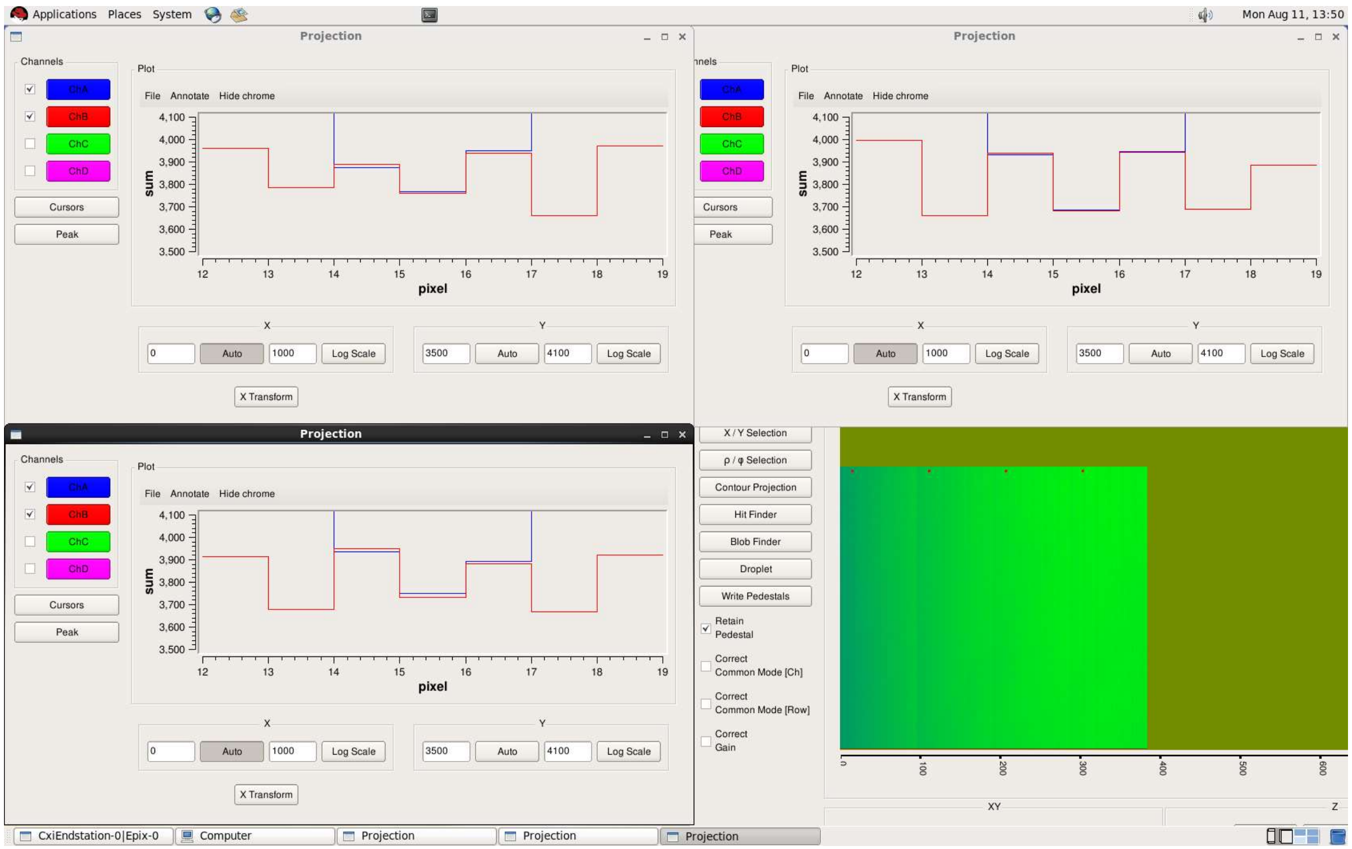


Noise dispersion among pixels is on the order of 1.6%

The distribution show a non perfectly Gaussian behavior. Although the dispersion is negligible the behavior of the pixel in the tail is under study

ePix100a crosstalk measurements

SLAC

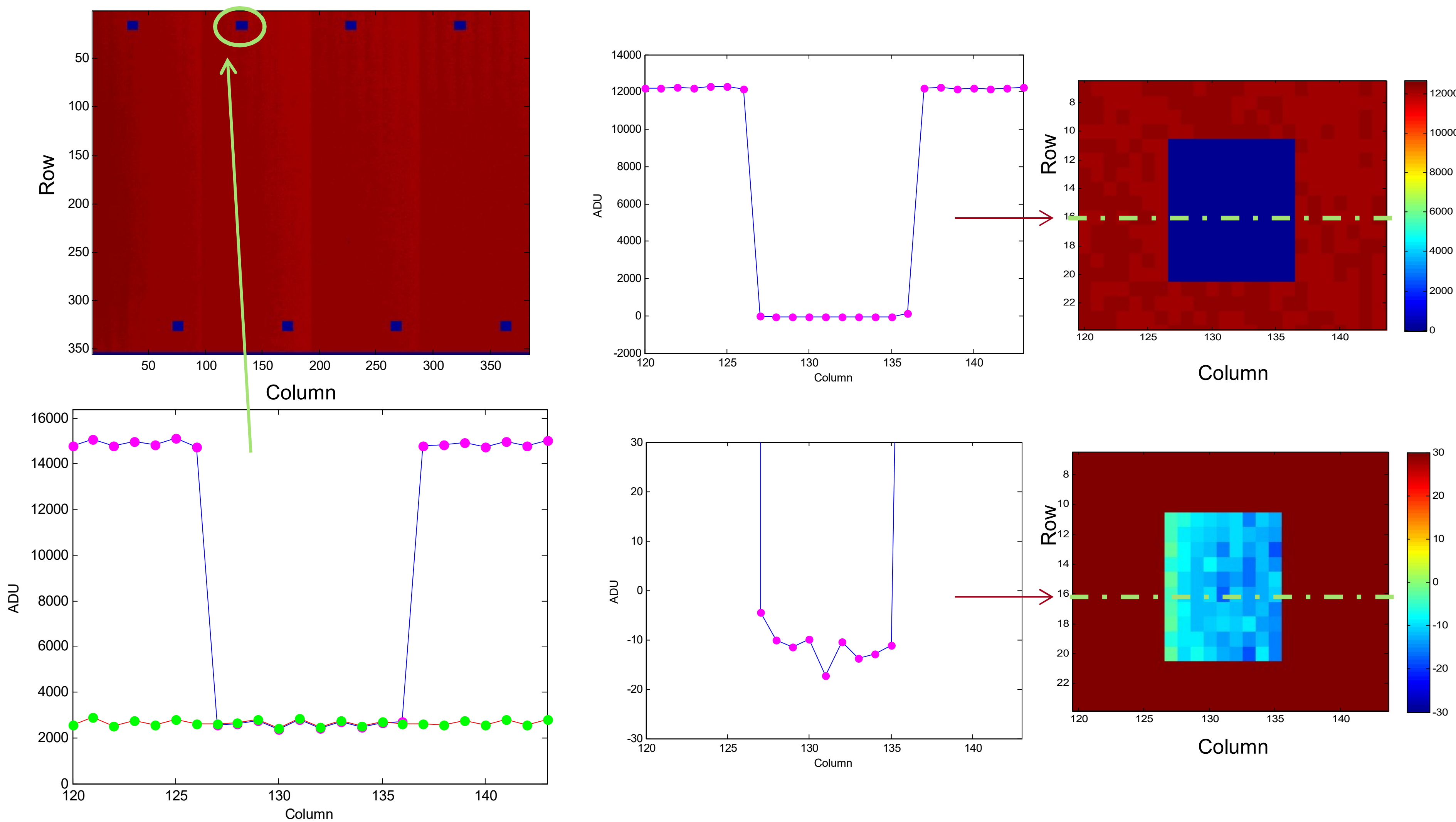


Study of the behavior of a 3x3 not-pulsed pixels section when the rest of the matrix is pulsed with max signal

Negligible crosstalk has been observed, at the level of the noise.

Measurement performed at the nominal integration time of 36us

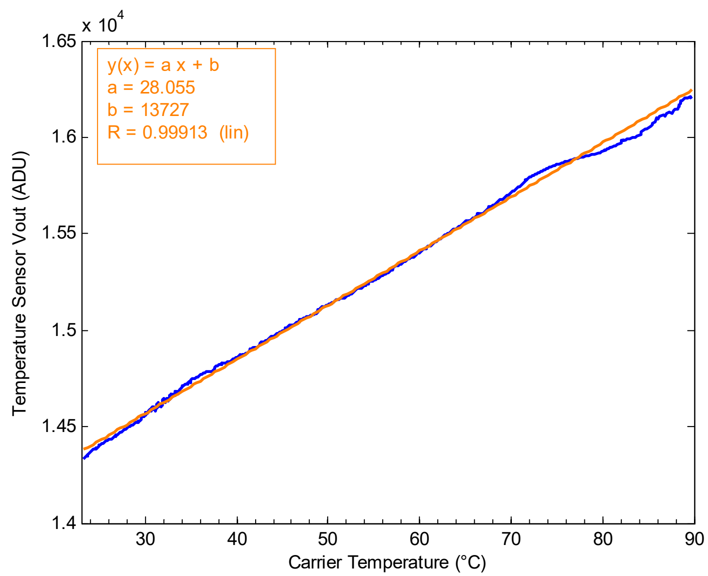
ePix100a crosstalk measurements



ePix100p temperature behavior (see K. Nishimura's talk for the 100a results)

SLAC

on-chip temperature sensor

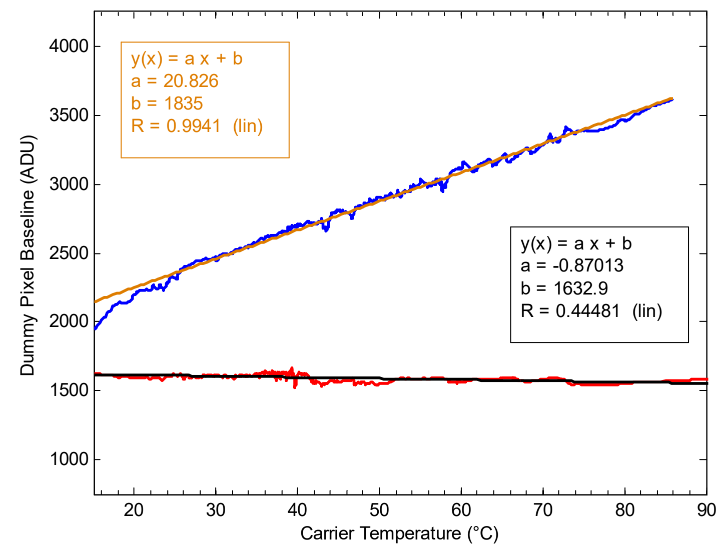


T_{ePix} (°C) = 0.0356*Tempsens(ADU)-489.28

Temperature sensor characteristic measured in comparison with a thermistor mounted on the ASIC side.

Measurement is affected by instability of the temperature and by the difference of thermal capacity of the two devices.
Accurate measurements will be repeated using a environmental chamber

temperature compensation circuitry



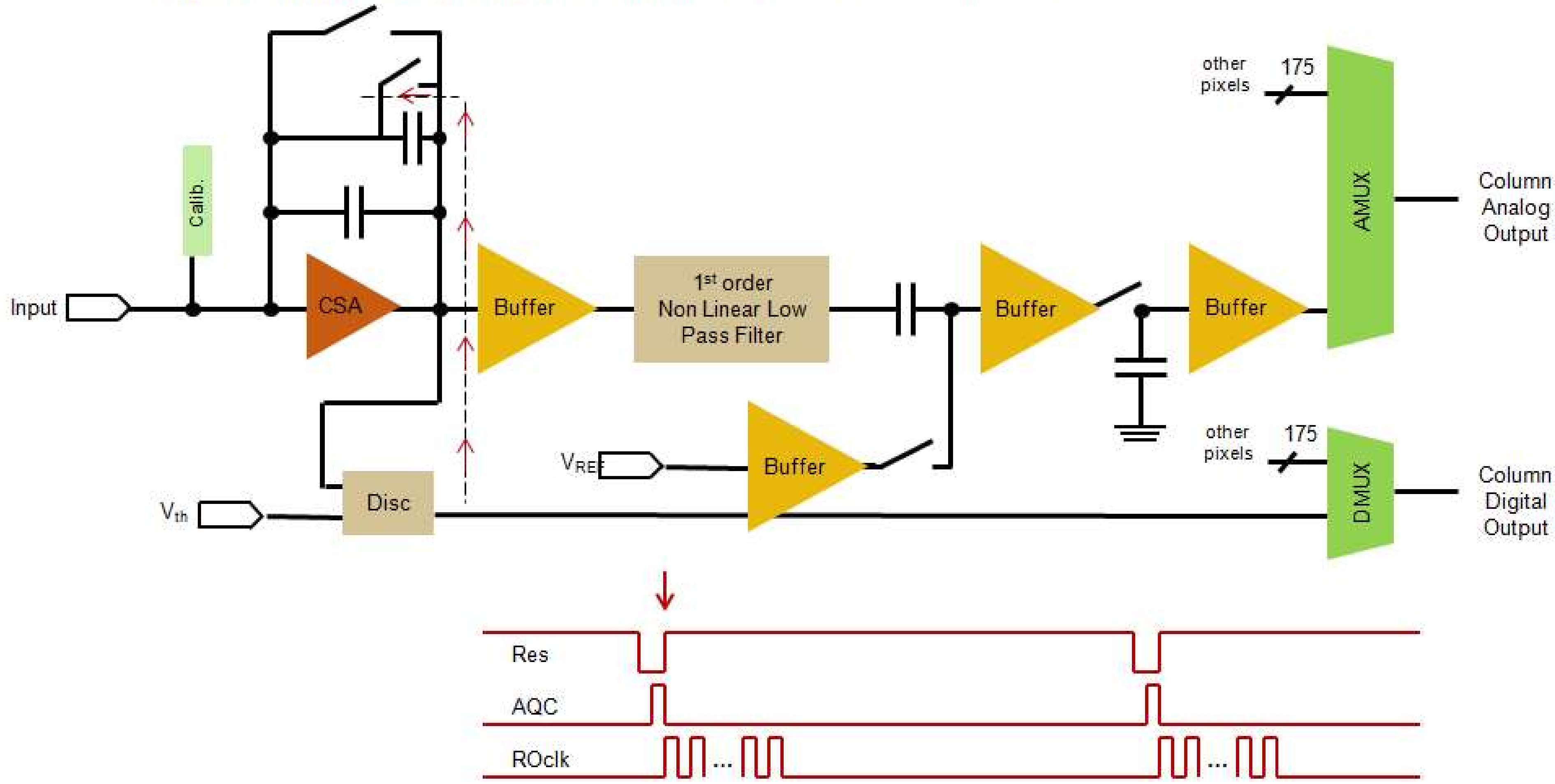
TC_{ePix} (uncompensated) = 20.8 ADU/°C

TC_{ePix} (compensated) = -0.9 ADU/°C

After proper calibration a TC between +- 0.2 ADU/°C is expected

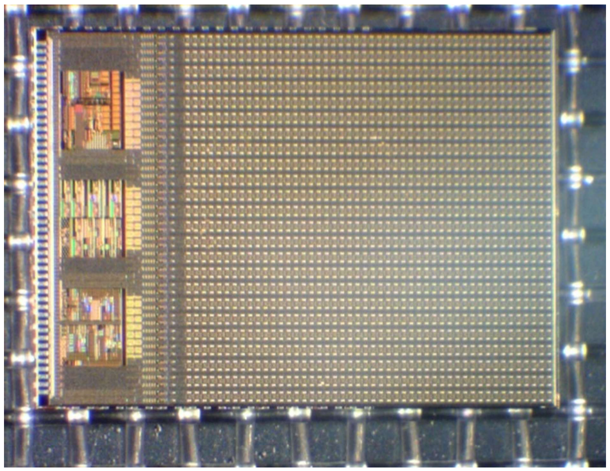
ePix10k pixel architecture

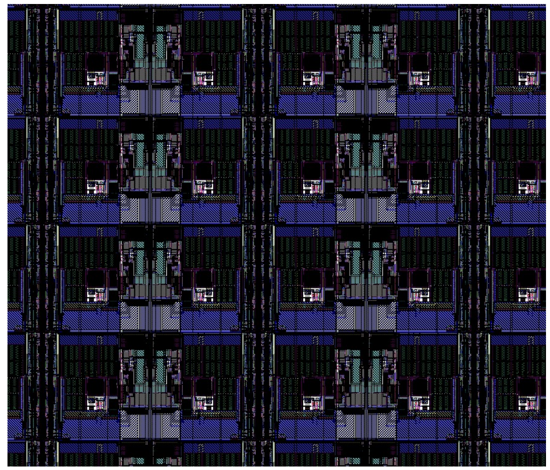
Signal Sampling Phase (signal larger than 100ph at 8keV): : Res is Low, AQC goes Low



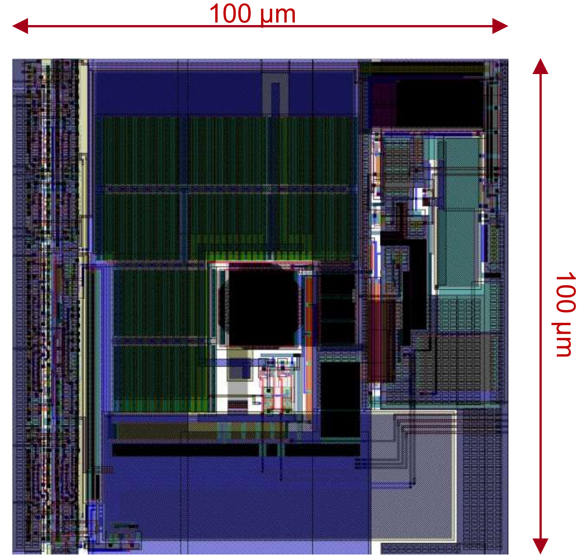
ePix10kp pixel layout 100µm x 100µm

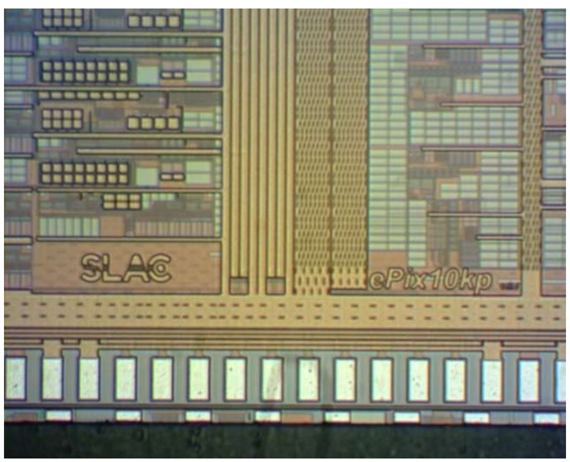
ePix10k prototype 48x48 pixels



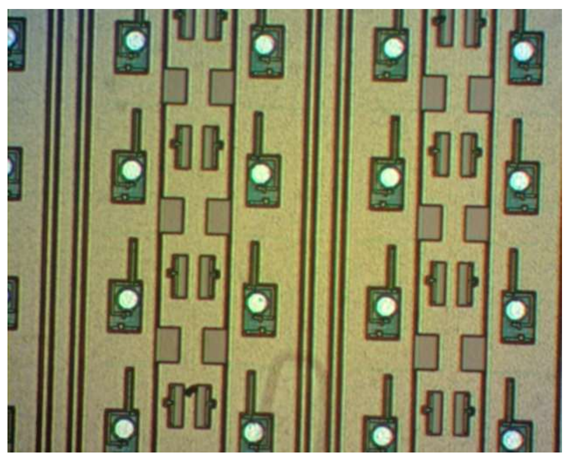


~ 20 million transistors

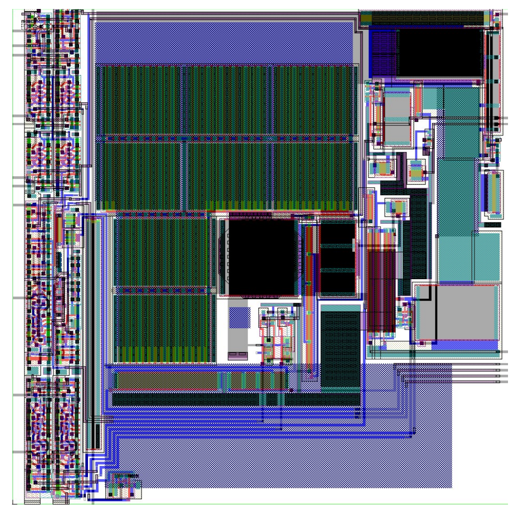




ePix10kp balcony close up

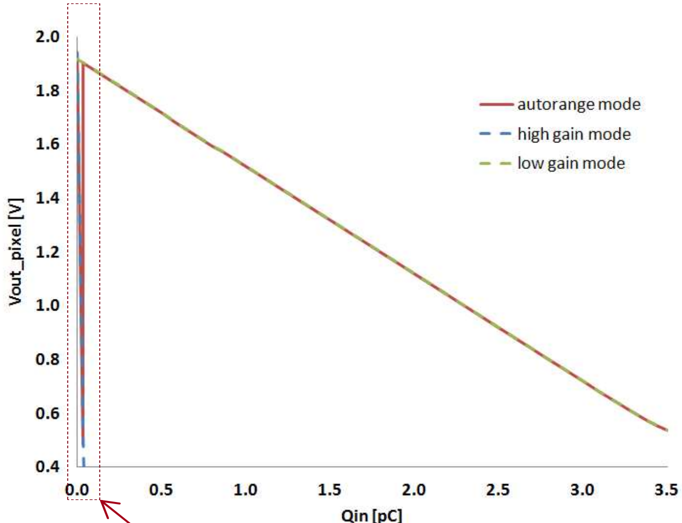


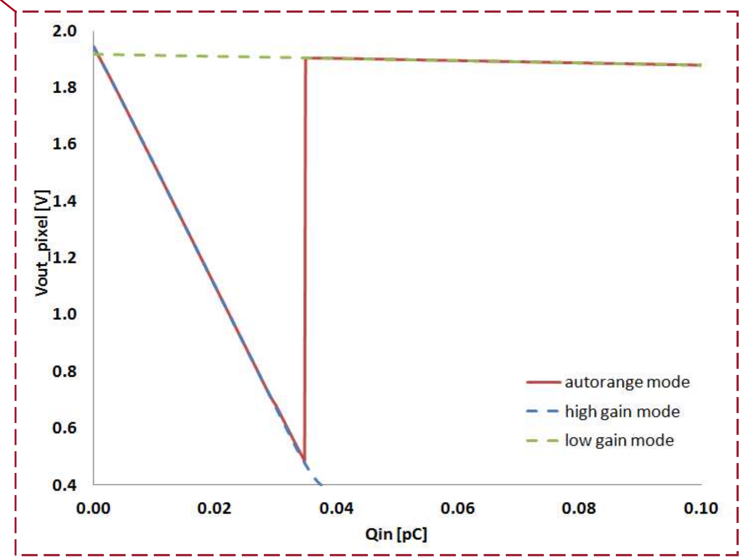
ePix10kp pixel close up



ePix10kp pixel layout

ePix10k expected pixel response - linearity



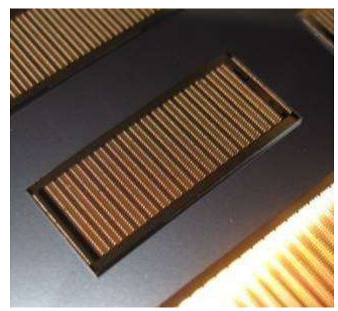


3 Modes of operation:

- High Gain = 42mV/fC or 6.5µV/e^-
- Low Gain = 398mV/pC or 64nV/e^-
- Auto-ranging

Non-Linearity < 0.05%

KPiX SLAC;
similar implementation successfully used in HEP:



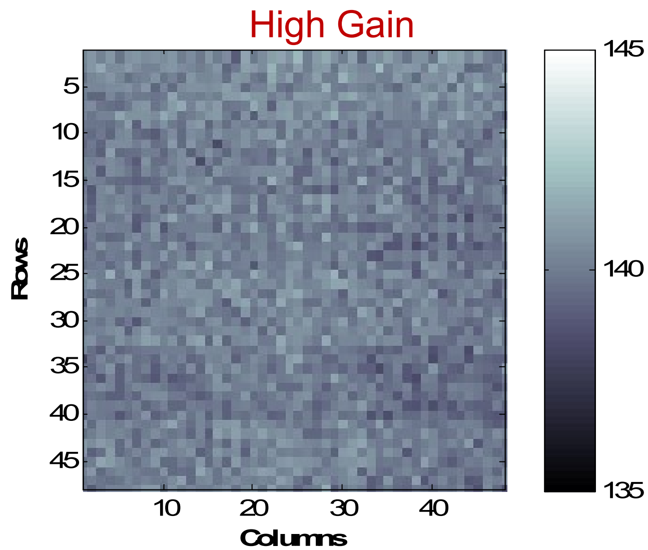
- 1024 pixels
- Auto-ranging (multiple gains),
- Multiple sampling per train,
- Power pulsing

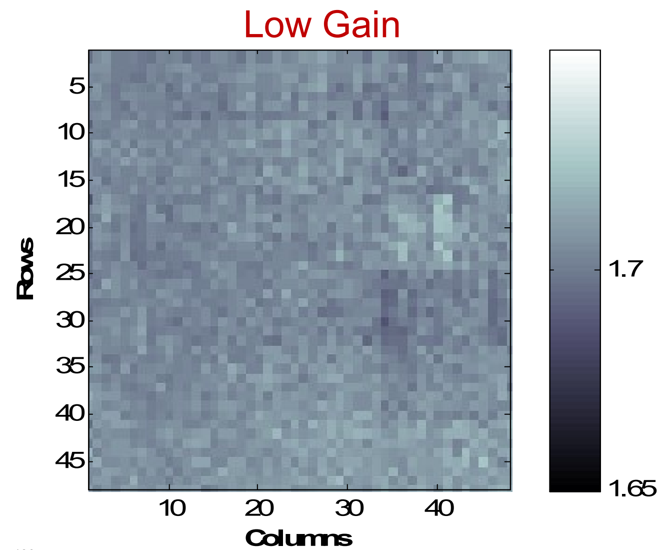
D. Freytag et al., *IEEE Nucl. Sci. Symp. Conf. Rec. (2008) 3447*

ePix10k gain uniformity measurement

ePix10kp gain maps:

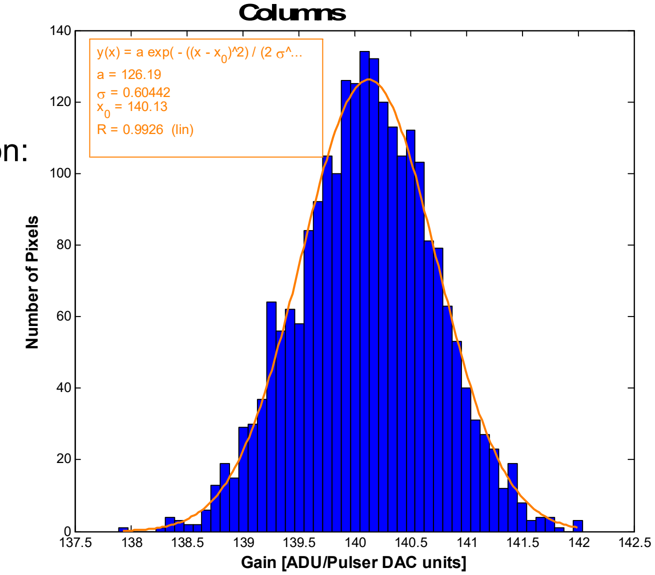
Good Uniformity of gain across the full matrix is achieved in both High Gain and Low Gain

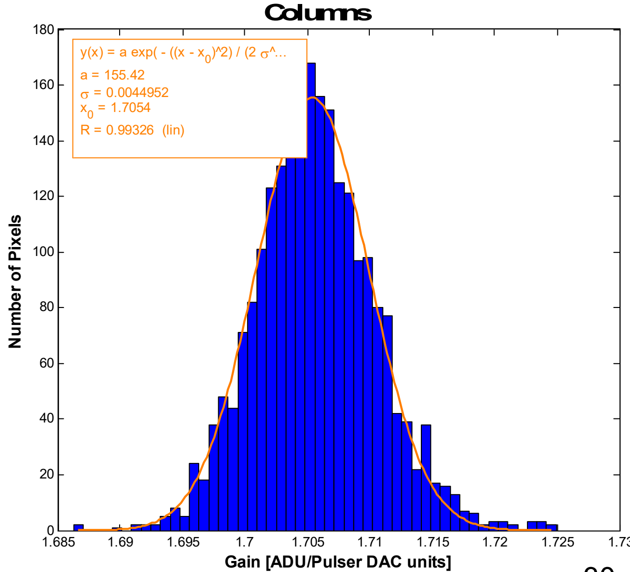




Overall gain distribution and dispersion:

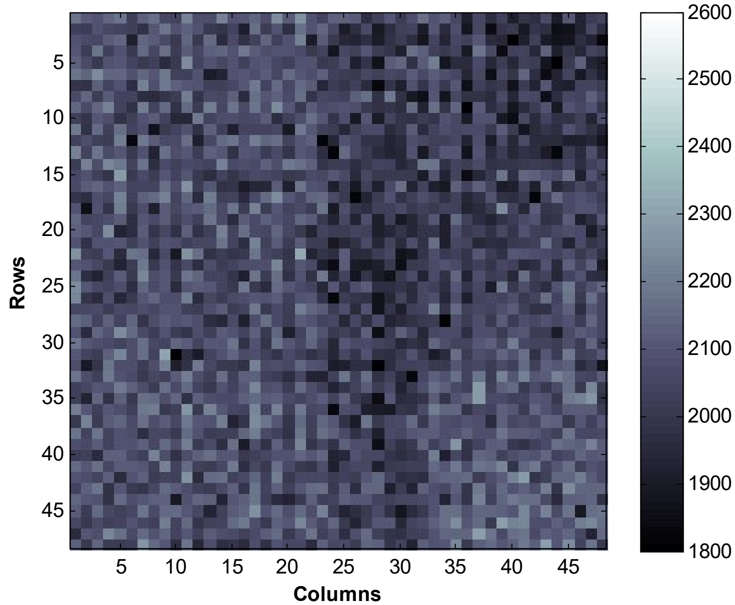
A gain dispersion of ~0.4% in High Gain and of ~ 0.3% in Low Gain have been achieved





Dark frame uniformity: fixed patterns

ePix10kp darkframe (1000 frames averaged)



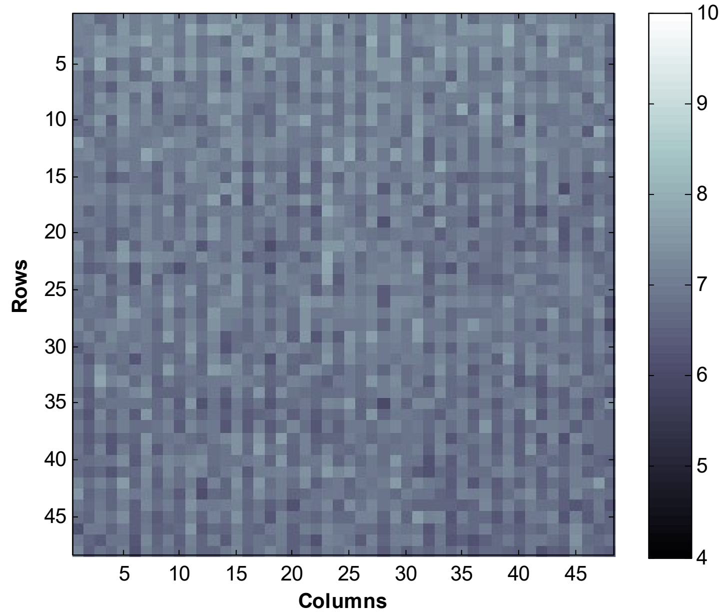
Fixed pattern noise is visible across columns as expected considering the layout arrangement of the pixels in the matrix (groups of 16 with mirror image every column)

Good flatness of the dark field is achieved:

Flatness across rows < 80 counts i.e. max 0.4%

Flatness across columns < 120 counts i.e. max 0.6%

ePix10kp noise (darkframe subtracted)

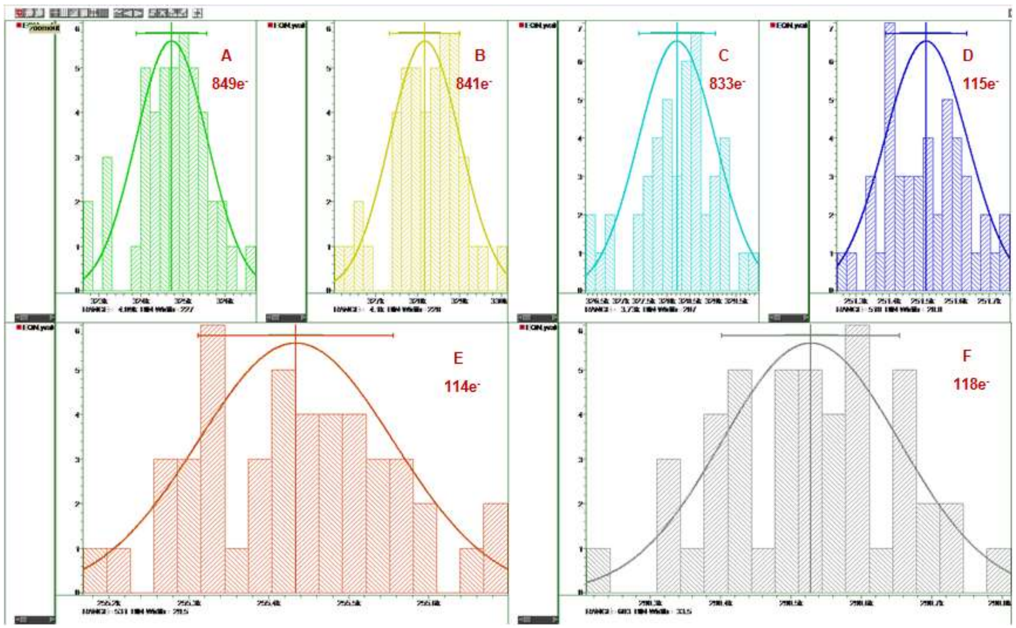


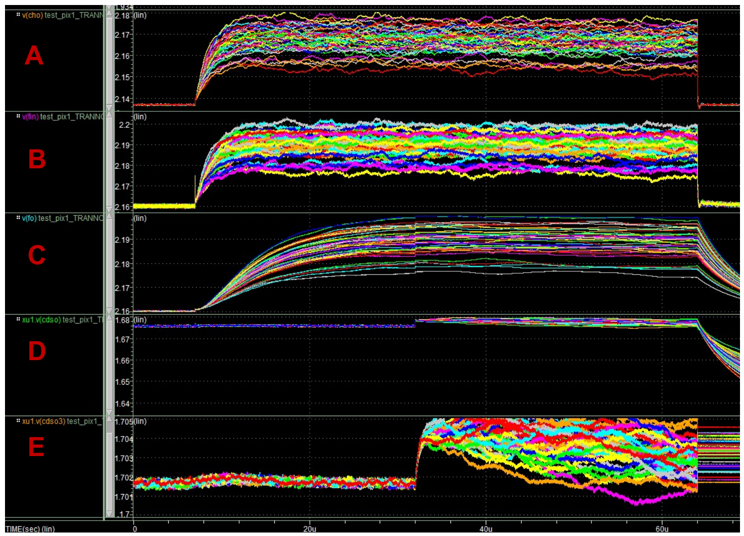
Good noise uniformity across the full matrix is achieved:

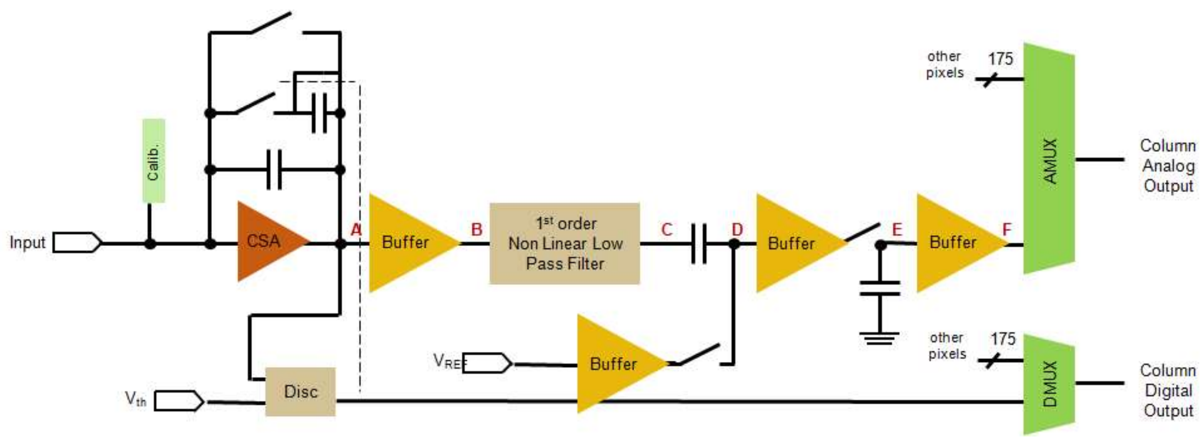
Flatness across rows < 0.4 count i.e. max 6%

Flatness across columns < 0.2 count i.e. max 3%

ePix10k noise simulations



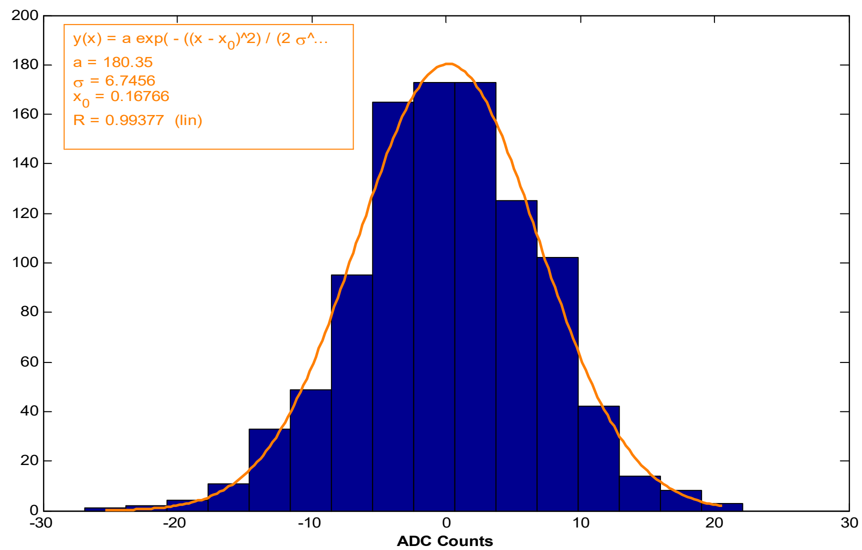




ePix10k noise performance

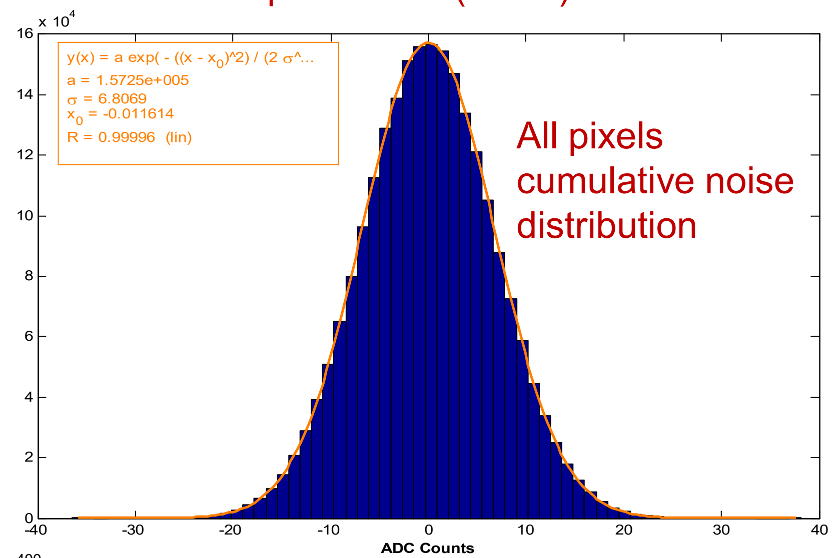
SLAC

Single pixel noise distribution

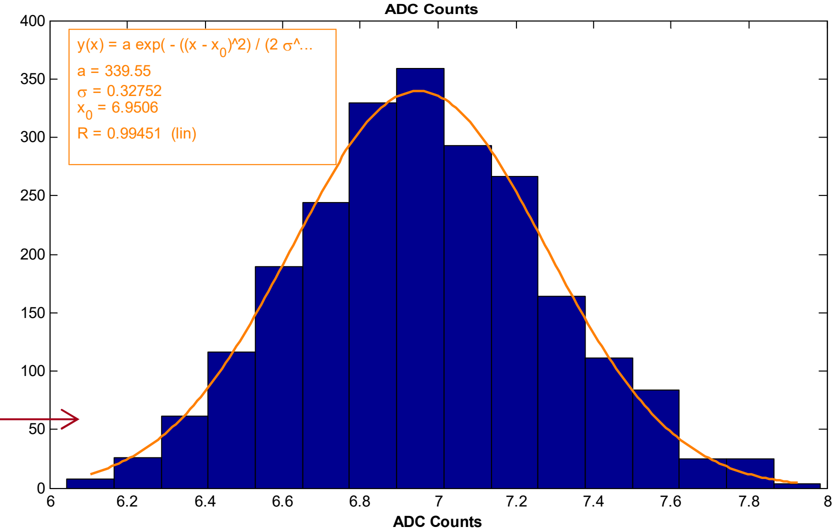


a sigma of 6.7 counts r.m.s. is equivalent to about 120e- r.m.s. i.e. a S/N ratio of 18 for single photon at 8keV

Distribution of the pixel noise (r.m.s.) across the matrix



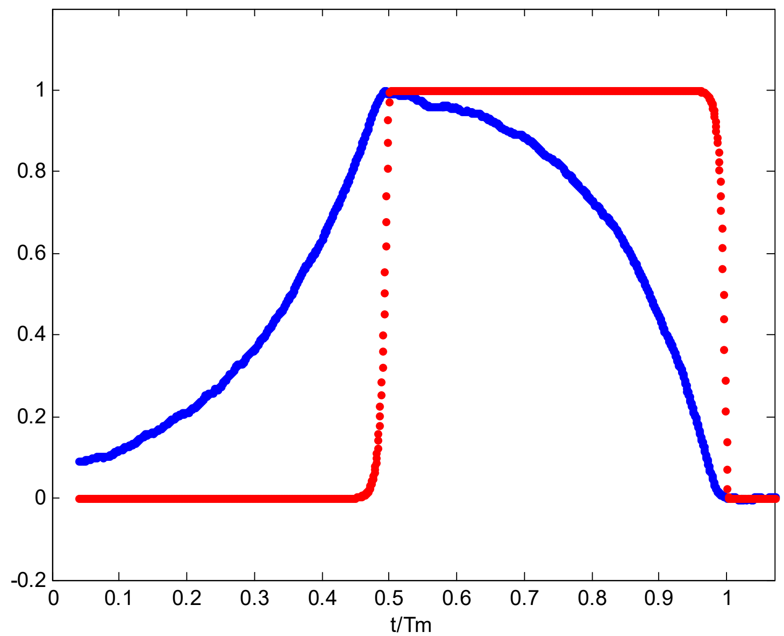
All pixels cumulative noise distribution



Noise dispersion among pixels is on the order of 5%

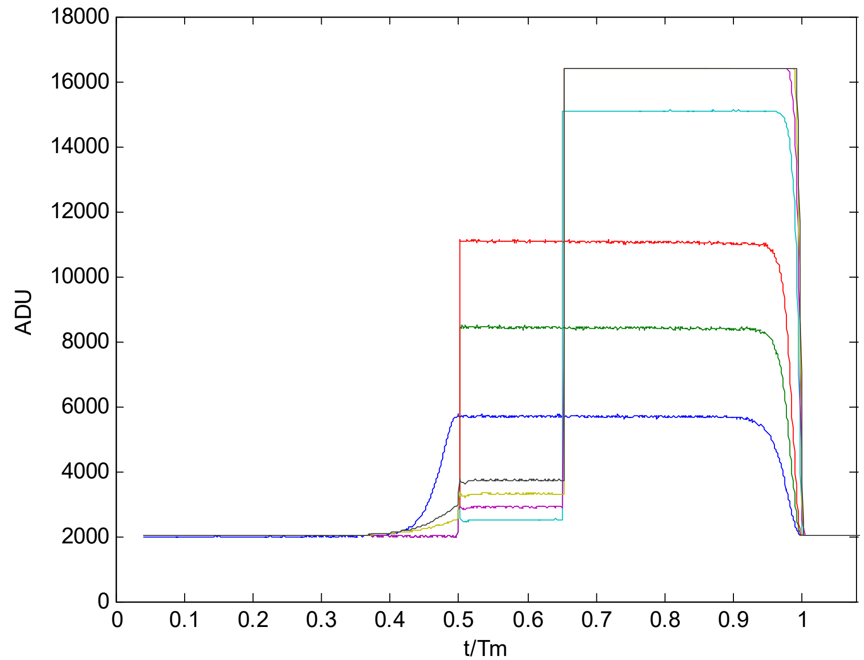
ePix10k weighting functions

Weighting functions in high gain mode



For a small signal the filter has a long time constant and the function is quasi-trapezoidal

Weighting functions in auto-range mode



Passed the range switching the weighting function has a reduced amplitude. The effect of gating the comparator firing can be seen in the top right part.

CDS effects on auto-ranging – ePix approach

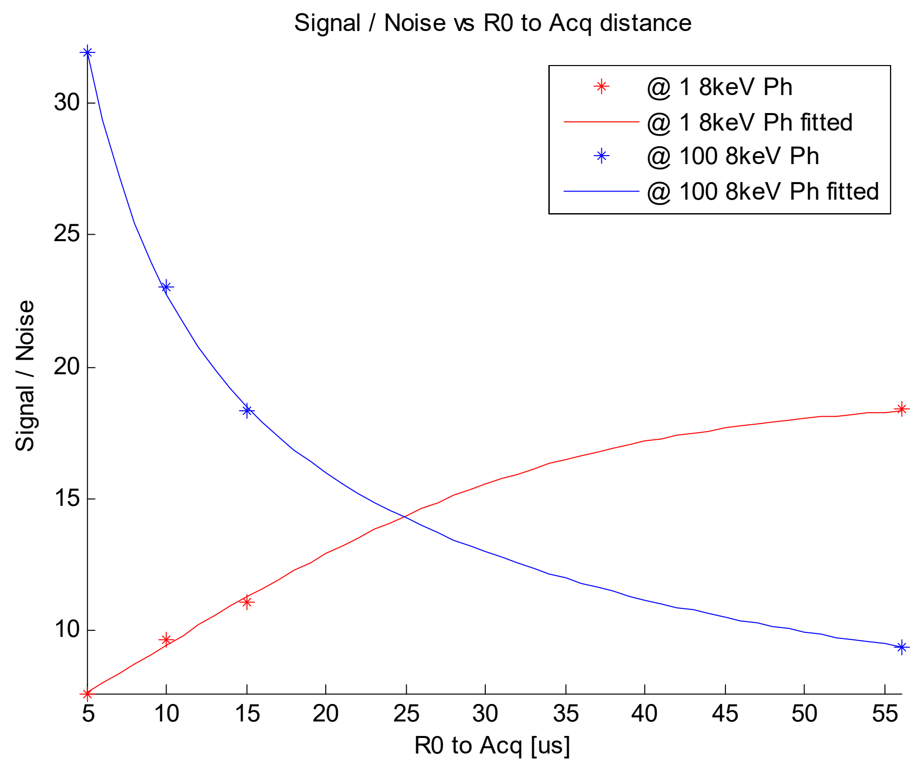
In auto-ranging if a signal triggers the comparator, the CDS will subtract a baseline weighted with a larger gain, resulting in an excess noise in the second range.

Solutions:

- read the 2 samples separately and subtract only if the signal is in the first range
- don't use CDS at all
- or the ePix approach

Because the intervals of time reserved to sample the baseline and the signal are continuously adjustable in ePix; the CDS timings can be unbalanced resulting in a filtered version of the baseline sample with an effective lower gain. This is equivalent of reducing the efficiency of the CDS and increasing the S/N ratio at the switching point.

Trade off between S/N ratio at the switching point and at the minimum signal in ePix10k auto-range mode



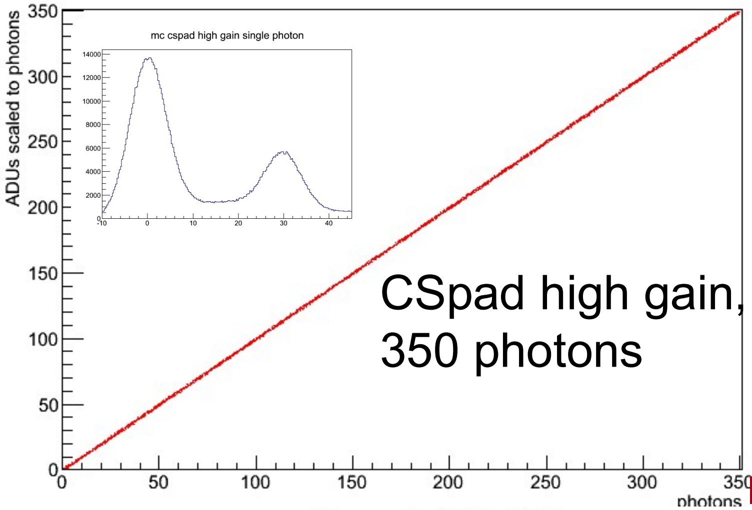
There is an optimal point at which the S/N is larger than 14 (150e- in the first range) in both ranges

Cspad 2 fixed gains -> ePix10k autoranging

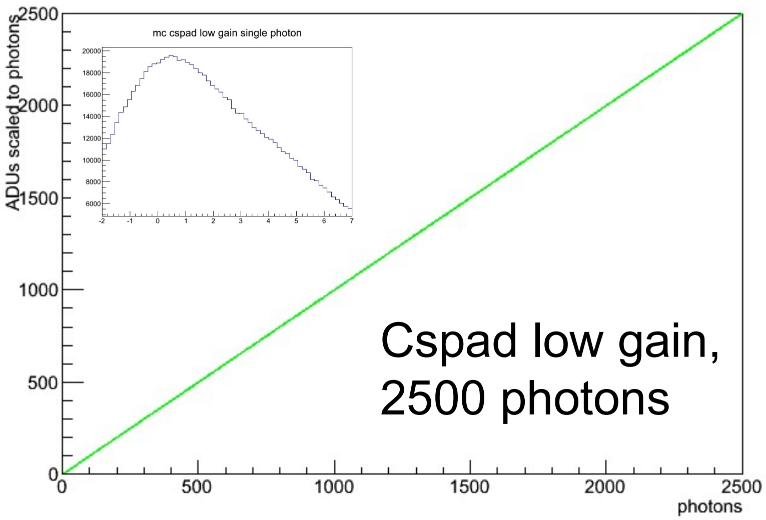
P. Hart

SLAC

cspad high gain (about 8 S/N)

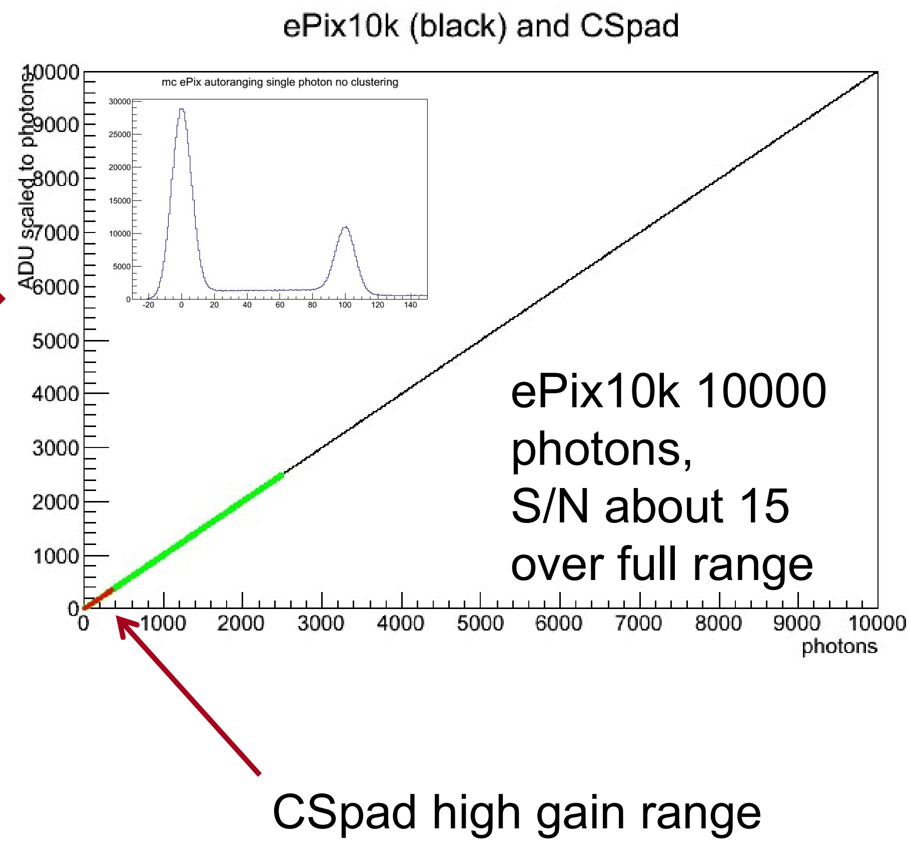


cspad low gain (3ish S/N)



Insets show pedestal and single photon distribution

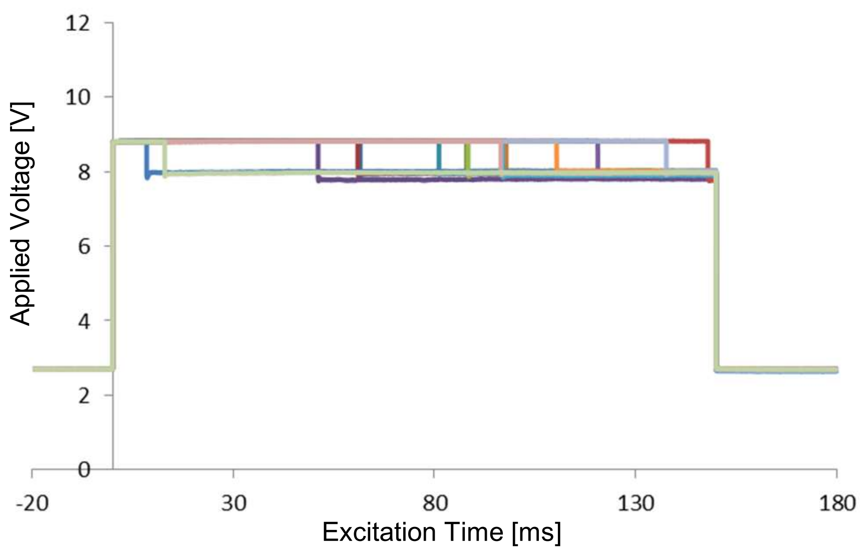
ePix10k (black) and CSpad



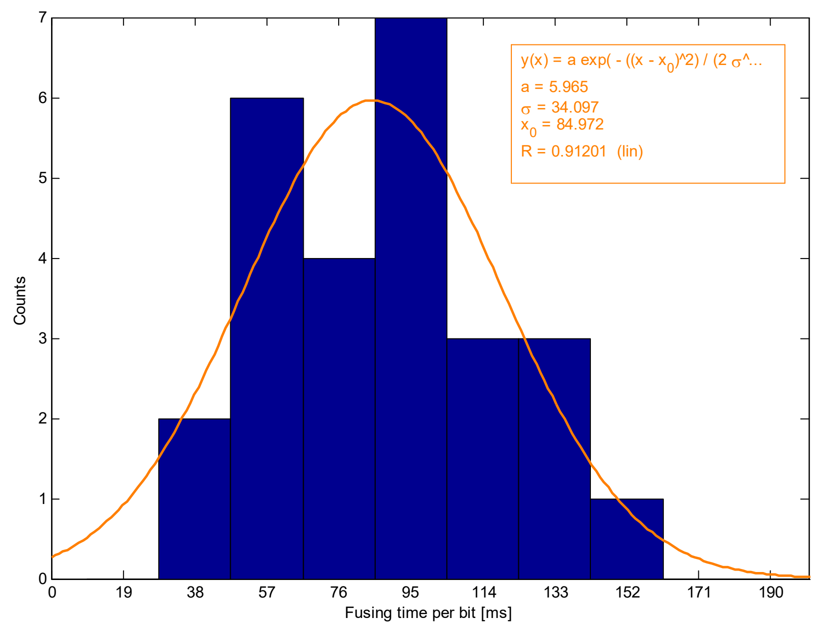
Chip ID (tested in ePix10kp and included in ePix100a)

A custom anti-fuse based register allows the possibility to write a 16bit ID to identify each chip. An additional 16 bit register contains an hard code Identifier of the ASIC model and version.

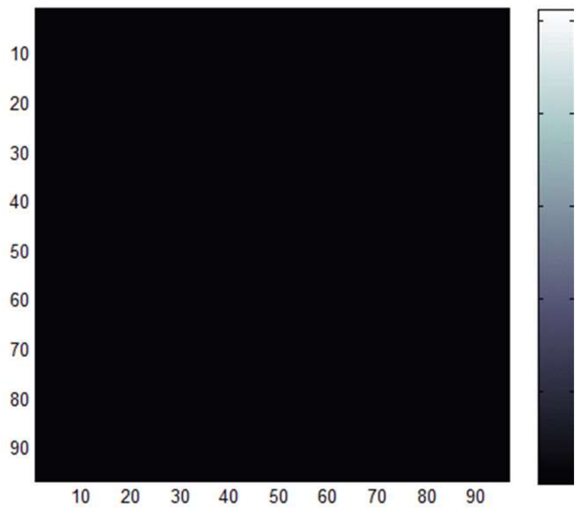
Optimized excitation required for anti-fuse burning



Distribution of a bit fusing time



Summary



ePix100p with some pixel injected using the automatic scan mode based on the internal pulser. The pulser injects in every frame an increased amount of charge in the selected pixels up to the full scale (100Ph @8keV).
The interesting aspect of this movie is that all functionalities of the ASIC are used.

- SLAC is working on a new generation of hybrid pixel detectors for photon science based on a modular platform approach that:
  - facilitates integration, scalability, versatility
  - mitigates risks
  - reduces development time and costs

- ePix is a class of front-end ASICs for integrating hybrid photon detectors
  - Based on a column parallel readout architecture with sigma delta ADCs
  - Fully analog pixel matrix with filtering optimized for different areas of application
    - **ePix-100** is optimized for **ultra low noise** applications. It has pixels of 50µmx50µm size arranged in a 352x384 matrix. A resolution of ~50e^- r.m.s. and a signal range of 35fC (100 photons at 8keV) has been achieved. In its final version it will be able to sustain a frame rate of 1kHz.
    - **ePix-10k** is optimized for **high dynamic range** applications. It has pixels of 100µmx100µm size arranged in a 176x192 matrix. A resolution of less than 120e^- r.m.s. and a signal range of 3.5pC (10k photons at 8keV) has been achieved. In its final version it will be able to sustain a frame rate of 1kHz.

- Tests on the ePix100 and ePix10k prototypes and the ePix100a have demonstrated the approach is sound.
  - In particular the platform has been proven to behave as required, together with the power distribution system (100a), allowing to proceed also with the submission of the full size variant ePix10ka.