Configuration Registers

	Address																	Address (cmd = 6 for Start Register cmd=1 for Stop Registers)					Address				
	1	2	3MSB	3LSB	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
BIT 0	CompTH_DAC 0	Pixel Dummy	Pulser 8	Pulser 0	DM1 0	Pulser_DAC 0	DM1en	VREF_DAC 0	TPS_tcomp	TPS_GR 0	PP_OCB_S2D	Preamp 0	S2D_tcomp	tc 0	TPS_tcDAC 0	S2D0_tcDAC 0	test_BE	Row Start (9bits)	Row Stop (9bits)	Column Start (7bits)	Column Stop (7bits)	CHIP ID (16 bits)	S2D1_GR 0	S2D3_GR 0	S2D1_tcDAC 0	S2D2_tcDAC 0	S2D3_tcDAC 0
1	CompTH_DAC 1		Pulser 9	Pulser 1	DM1 1	Pulser_DAC 1	DM2en	VREF_DAC 1	TPS_MUX 0	TPS_GR 1	OCB 0	Preamp 1	Filter_DAC 0	tc 1	TPS_tcDAC 1	S2D0_tcDAC 1	is_en						S2D1_GR 1	S2D3_GR 1	S2D1_tcDAC 1	S2D2_tcDAC 1	S2D3_tcDAC 1
2	CompTH_DAC 2		Pbit	Pulser 2	DM1 2	Pulser_DAC 2	emph_bd 0	VREF_DAC 2	TPS_MUX 1	TPS_GR 2	OCB 1	Preamp 2	Filter_DAC 1	S2D 0	TPS_DAC 0	S2D0_DAC 0	DelEXEC						S2D1_GR 2	S2D3_GR 2	S2D1_DAC 0	S2D2_DAC 0	S2D3_DAC 0
3	CompTH_DAC 3		atest	Pulser 3	DM1 3	Monost_Pulser 0	emph_bd 1	VREF_DAC 3	TPS_MUX 2	TPS_GR 3	OCB 2	Pixel_CB 0	Filter_DAC 2	S2D 1	TPS_DAC 1	S2D0_DAC 1	DelCCKreg						S2D1_GR 3	S2D3_GR 3	S2D1_DAC 1	S2D2_DAC 1	S2D3_DAC 1
4	CompTH_DAC 4		test	Pulser 4	DM2 0	Monost_Pulser 1	emph_bd 2	VREF_DAC 4	TPS_MUX 3	S2D0_GR 0	Monost 0	Pixel_CB 1	Filter_DAC 3	S2D 2	TPS_DAC 2	S2D0_DAC 2	RO_rst_en						S2D2_GR 0	trbit	S2D1_DAC 2	S2D2_DAC 2	S2D3_DAC 2
5	CompTH_DAC 5		Sab_test	Pulser 5	DM2 1	Monost_Pulser 2	emph_bc 0	VREF_DAC 5	RO_Monost 0	S2D0_GR 1	Monost 1	Pixel_CB 2	Filter_DAC 4	S2D_DAC_Bias 0	TPS_DAC 3	S2D0_DAC 3	SLVDSbit						S2D2_GR 1		S2D1_DAC 3	S2D2_DAC 3	S2D3_DAC 3
6	CompEn 0		Hrtest	Pulser 6	DM2 2	CompEn 1	emph_bc 1	VrefLow 0	RO_Monost 1	S2D0_GR 2	Monost 2	Vld1_b 0	Filter_DAC 5	S2D_DAC_Bias 1	TPS_DAC 4	S2D0_DAC 4	FELmode						S2D2_GR 2		S2D1_DAC 4	S2D2_DAC 4	S2D3_DAC 4
7	PulserSync		PulserR	Pulser 7	DM2 3	CompEn 2	emph_bc 2	VrefLow 1	RO_Monost 2	S2D0_GR 3	fastPP_enable	Vld1_b 1	testLVDTransmitter	S2D_DAC_Bias 2	TPS_DAC 5	S2D0_DAC 5	CompEnOn			Not Available			S2D2_GR 3		S2D1_DAC 5	S2D2_DAC 5	S2D3_DAC 5
Default Value	42			0	16	3	0	22	97	51	183	68	67	108	88	89	0										

	Number of Bits	Dec Value	Bin Value	Function		Allocated?
tc	2	0	00	*BGR temperature Compensation Bits*	BE_ANALOG	TRUE
TPS_DAC	6	22	010110	*TestPoint System Input Common Mode*		TRUE
TPS_GR	4	3	0011	*TestPoint System Output Dynamic Range*		TRUE
TPS_MUX	4	0	0000	*TestPoint System Input Selector*		TRUE
TPS_tcomp	1	1	1	*TestPoint System temperature Compensation On/Off*		TRUE
TPS_tcDAC	2	0	00	*TestPoint System temperature Compensation Gain*		TRUE
RO_Monost	3	3	011	*Programmable Read Out Delay*		TRUE
S2D	3	3	011	*Output Driver Driving Capabilities and Stability*		TRUE
S2D_DAC	6	22	010110	*Output Driver Input Common Mode*		FALSE
S2D_GR	4	3	0011	*Output Driver Output Dynamic Range*		FALSE
S2D_tcDAC	2	1	01	*Output Driver temperature Compensation Gain*		FALSE
S2D_tcomp	1	1	1	*Output Driver temperature Compensation On/Off*		TRUE
S2D_DAC_Bias	3	3	011	*Output Driver Input Common Mode*		TRUE
Pulser_DAC	3	3	011	*Test Pulser Current*		TRUE
PP_OCB_S2D	1	1	1	*Balcony On/Off (1 is On)*		TRUE
OCB	3	3	011	*Balcony Driver Current*		TRUE
Monost	3	3	011	*Fast Power Pulsing Speed*		TRUE
Filter_DAC	6	33	100001	*Pixel Filter Level (Default 1V)*		TRUE
VREF_DAC	6	22	010110	*Baseline DAC (Default 1.65V)*		TRUE
Preamp	3	4	100	*Preamplifier Current*		TRUE
Pixel_CB	3	4	100	*Pixel Output Buffer Current*		TRUE
fastPP_enable	1	1	1	*Fast Power Pulsing Enable*		TRUE
CompTH_DAC	6	42	101010	*Comparator Threshold DAC*		TRUE
Vld1_b	2	1	01	*Pixel Buffer Current*		TRUE
Vref_low	2	0	00			FALSE
CompEn	3	0	000	*Comparator Enable Delay in FEL Mode Off*		TRUE
Pulser	10	0	0000000000	*Test Pulser Level*	BE_DIGITAL	TRUE
test	1	0	0	*test mode*		TRUE
atest	1	0	0	*Automatic test mode On/Off (0 is off)*		TRUE
Pbit	1	0		*Pulser Counter Direction*		TRUE
HRtest	1	0	0	*High Resolution Mode Test*		TRUE
Sab_test	1	0	0	*test mode with Dark Frame*		TRUE
is_en	1	0	0	*Interleaved ReadOut Enable*		TRUE
Monost_Pulser	3	0		*Pulser vs Pixel ON delay*		TRUE
DM1	4	0	0000	*Digital Monitor Mux 1*		TRUE
DM2	4	1	0001	*Digital Monitor Mux 2*		TRUE
DelEXEC	1	0	0	*EXEC Delay ENABLE*		TRUE
DelCCKreg	1	0	0	*CCKreg Delay ENABLE*		TRUE
estLVDTransmitte	1	0	0	*if 1 High Speed LVDS transmitter under test*		TRUE
test_BE	1	0	0	*test BackEnd*	Matrix	TRUE
FELmode	1	1	1	*FEL mode vs Syncrothron Mode (ACQ and CompEnable Signal are modified)*		TRUE
CompEnOn	1	?	#VALUE!	*Comparators enable mode On/Off*		TRUE
trbit	1	?	#VALUE!	*Transition bit*		TRUE
DM1en	1	0	0	*Digital Monitor 1 Enable*	PADS	TRUE
DM2en	1	0	0	*Digital Monitor 2 Enable*		TRUE
emph_bd	3	0	000	*emphasis bit delay*		TRUE
emph_bc	3	0	000	*emphasis bit current*		TRUE
TOTAL	125					
Available	0					

Bit map: (from Angelo)

ga	g	
0	0	Auto range
0	1	Auto Range Test
1	0	low gain
1	1	high gain

Digital

Mux		Description
0	clk	clk
1	exec	exec
2	ro_rst	ro_rst
3	ack	
4	is_en	
5	ROWclk	
6	ADDR0	ADDR_buff0
7	ADDR1	ADDR_buff1
8	ADDR2	ADDR_buff2
9	ADDR3	ADDR_buff3
10	ADDR4	ADDR_buff4
11	CMD0	cmd_buff_0
12	CMD1	cmd_buff_1
13	CMD2	cmd_buff_2
14	CMD3	cmd_buff_3
15	config	

Digital

Mux		Description
0	clk	
1	exec	
2	ro_rst	
3	ack	
4	is_en	
5	PixelDummyDout	
6	DB0	
7	DB1	
8	DB2	
9	DB3	
10	DB4	
11	DB5	
12	DB6	
13	DB7	
14	ADDRmat	
15	config	

Analog

Mux			Description
0	in	ok	???
1	fin	ok	???
2	fo	ok	???
3	abus	ok	???
4	cdso3	ok	???
5	bgr_2V	ok	*bgr voltage (should be equal to 2V)*
6	bgr_2vd	ok	*bgr variable voltage*
7	vx_comp	ok	*Output Driver DAC Reference (the temperature variation on this will decide the temperature compensation bits)*
8	vcmi	ok	*Output Driver Reference*
9	Pix_Vref	ok	*Baseline Control Voltage to the Pixel*
10	VtestBE	ok	*BE Calibration Voltage*
11	Pix_Vctrl	ok	*Filter Voltage*
12	testline	ok	*Pulser Output*
13	PTAT		
14	Vguard		
15			