Instrumentation for Accelerator Based sub-GeV DM Searches

Cameron Bravo (SLAC)

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

LDMX

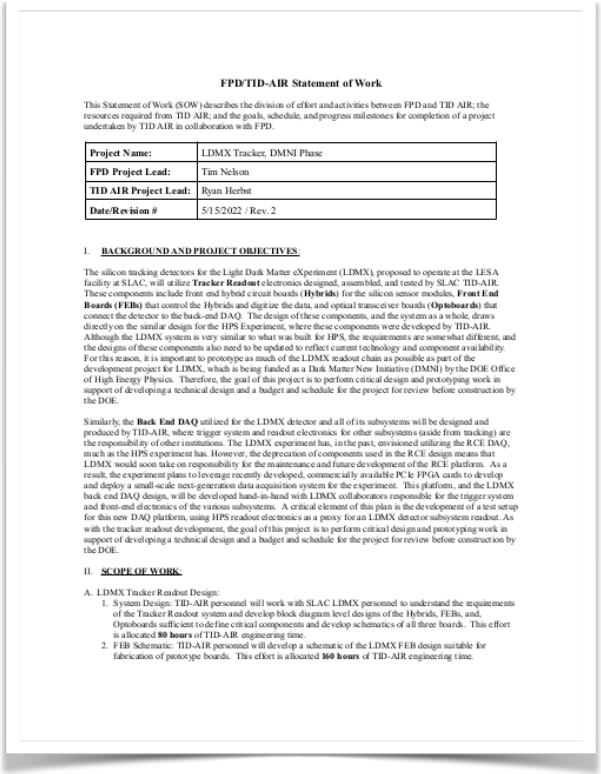
There is an SOW for this work, last revised 5/22

Tracker readout design

- Front End Board (FEB)
  - schematic
  - layout
  - prototyping
  - testing
- Readout hybrids
  - schematic to define board size (based on HPS)

Back end DAQ design/development

- System Design
- Bittware PCIe DAQ development
  - FPGA development
  - Testing with Tracker FEBs



FPD/TID-AIR Statement of Work

This Statement of Work (SOW) describes the division of effort and activities between FPD and TID AIR; the resources required from TID AIR; and the goals, schedule, and progress milestones for completion of a project undertaken by TID AIR in collaboration with FPD.

Project Name:	LDMX Tracker, DMNI Phase
FPD Project Lead:	Tim Nelson
TID AIR Project Lead:	Ryan Herbst
Date/Revision #	5/15/2022 / Rev. 2

I. **BACKGROUND AND PROJECT OBJECTIVES:**

The silicon tracking detectors for the Light Dark Matter eXperiment (LDMX), proposed to operate at the LESA facility at SLAC, will utilize **Tracker Readout** electronics designed, assembled, and tested by SLAC TID-AIR. These components include front end hybrid circuit boards (**Hybrids**) for the silicon sensor modules, **Front End Boards (FEBs)** that control the Hybrids and digitize the data, and optical transceiver boards (**Optoboards**) that connect the detector to the back-end DAQ. The design of these components, and the system as a whole, draws directly on the similar design for the HPS Experiment, where these components were developed by TID-AIR. Although the LDMX system is very similar to what was built for HPS, the requirements are somewhat different, and the designs of these components also need to be updated to reflect current technology and component availability. For this reason, it is important to prototype as much of the LDMX readout chain as possible as part of the development project for LDMX, which is being funded as a Dark Matter New Initiative (DMNI) by the DOE Office of High Energy Physics. Therefore, the goal of this project is to perform critical design and prototyping work in support of developing a technical design and a budget and schedule for the project for review before construction by the DOE.

Similarly, the **Back End DAQ** utilized for the LDMX detector and all of its subsystems will be designed and produced by TID-AIR, where trigger system and readout electronics (or other subsystems (aside from tracking) are the responsibility of other institutions. The LDMX experiment has, in the past, envisioned utilizing the RCE DAQ, much as the HPS experiment has. However, the deprecation of components used in the RCE design means that LDMX would soon take on responsibility for the maintenance and future development of the RCE platform. As a result, the experiment plans to leverage recently developed, commercially available PCIe FPGA cards to develop and deploy a small-scale next-generation data acquisition system for the experiment. This platform, and the LDMX back end DAQ design, will be developed hand-in-hand with LDMX collaborators responsible for the trigger system and front-end electronics of the various subsystems. A critical element of this plan is the development of a test setup for this new DAQ platform, using HPS readout electronics as a proxy for an LDMX detector subsystem readout. As with the tracker readout development, the goal of this project is to perform critical design and prototyping work in support of developing a technical design and a budget and schedule for the project for review before construction by the DOE.

II. **SCOPE OF WORK:**

A. LDMX Tracker Readout Design:

1. System Design: TID-AIR personnel will work with SLAC LDMX personnel to understand the requirements of the Tracker Readout system and develop block diagram level designs of the Hybrids, FEBs, and, Optoboards sufficient to define critical components and develop schematics of all three boards. This effort is allocated **80 hours** of TID-AIR engineering time.
2. FEB Schematic: TID-AIR personnel will develop a schematic of the LDMX FEB design suitable for fabrication of prototype boards. This effort is allocated **360 hours** of TID-AIR engineering time.

SOW called for completion before end of FY22. More funding added in FY23 and expected in FY24. Important to keep on track for DOE reviews.

Thanks to Tim for this slide

2

HPS

SLAC

Routine updates and respins of previous designs (need to write an SOW)

- Front End Board (FEB)
  - schematic revisions (minor)
  - layout revisions (minor)
  - turnkey production of 20 boards (parts in hand)
  - testing
- Flange Boards
  - schematic revision (old transceivers discontinued)
  - layout revision
  - production of 10 boards
- Readout hybrids
  - respin of existing design (~20 boards) to build more detector modules

With next HPS run in 2025, this has not been urgent, so have prioritized LDMX work. However, the funds have been sitting idle and have been vulnerable to poaching. Need to get going.

Thanks to Tim for this slide

Readout Chips for Si Strip Trackers

- Limited quantities available of radiation hard front end chips for reading out Si strip sensors
  - APV25 production line at IBM decommissioned (0.25 um)
  - VFAT3 pad layout not ideal for Si strip senors
  - ABC130 uses opposite polarity wrt sensors we have
- None of these chips have all the features that would be “ideal” for our types of experiments
  - Analog readout for charge interpolation
  - Buffer depth to enable LHC Run3 scale trigger latency
  - Fixed latency binary data for track triggering
- Hard to justify new ASIC just for us, we make the scraps work