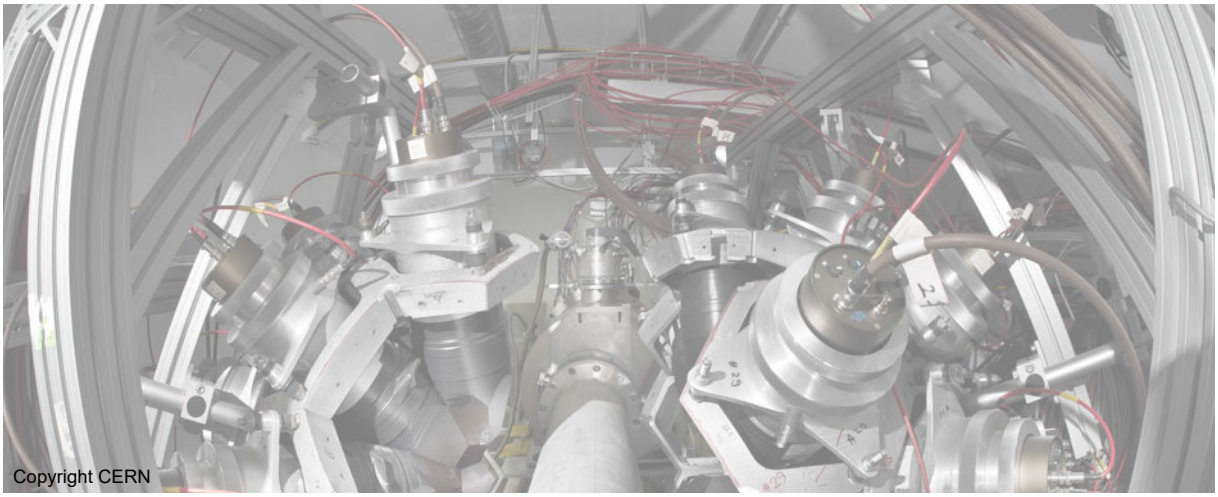
ADQ14 Datasheet

ADQ14 is a high-performance 14-bit data acquisition platform which offer complete and versatile solutions for advanced measurements.It comes with a generous set of hardware, firmware, and software features which help simplify integration. Every aspect of the measurement process from the detector, real-time signal processing, data visualization, and more are included. Selected features include:

- *Flexible choice of sampling rate, channel count, and multi-board synchronization*
- *Advanced programmable analog front-end supporting high input bandwidth*
- *Open FPGA for real-time DSP and stand-alone application-specific firmware*
- *Up to 3.2 GByte/s data transfer rate and optional peer-to-peer streaming to GPU*
- *Wide selection of form factors helps simplify integration*



Teledyne Signal Processing Devices Sweden AB | Teknikringen 6, SE-583 30 Linköping, Sweden | www.spdevices.com
Regional sales offices | www.spdevices.com/contact

ADQ14 Datasheet

Features

- Up to 4 analog channels
- Up to 2 GSPS sample rate per channel
- 14 bits vertical resolution
- DC-coupled with up to 1.2 GHz analog BW
- AC-coupled with up to 1.2 GHz analog BW
- Programmable DC-offset
- Internal and external clock reference
- Internal and external clock generator
- Clock reference output
- Internal and external trigger
- Trigger output
- Multi-channel synchronization
- Time-stamp for real-time operation
- 2 GBytes data memory
- Up to 3 GBytes/s data transfer to PC
- Data interfaces
  PXIe / PCIe / USB3.0 / MTCA.4 / 10 GbE

ADQ14 Development Kit

- Open FPGA for custom applications
- Real-time signal processing

Applications

- RADAR
- LIDAR
- Wireless communication
- High-speed data recording
- Test and measurement
- Ultrasonic ranging
- Time-of-flight scientific instruments
- Swept-Source OCT
- Thomson scattering

Advantages

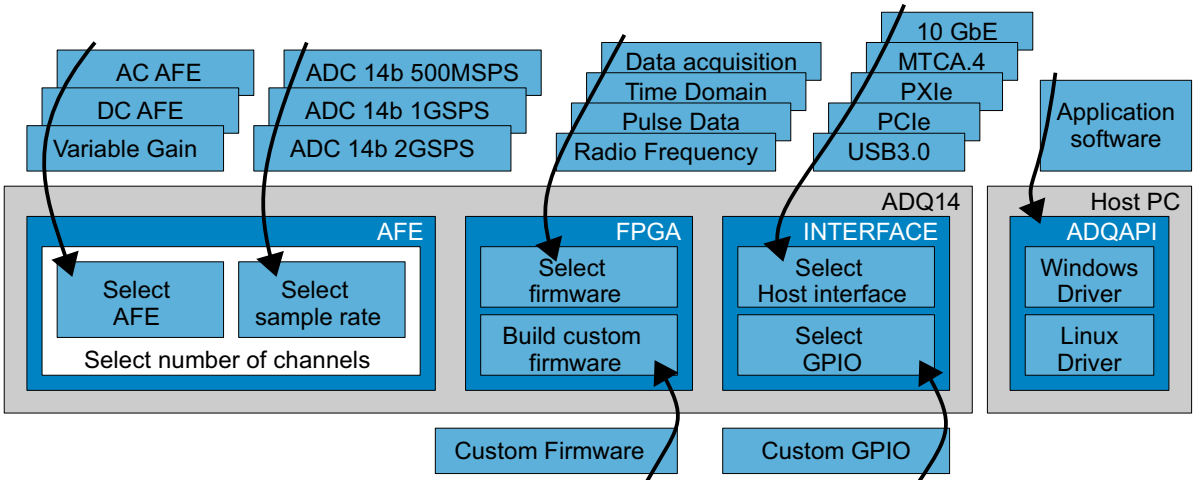
- Multiple form factor options helps optimize systems partitioning.
- Analog front-ends that support a wide range of detectors and allows for re-use and streamlined cost-efficient maintenance.
- Real-time FPGA custom processing enables compact system design.
- Teledyne SP Devices' design service is available for fast integration to reduce time-to-market.

Flexible digitizer solution for the complete signal chain

ADQ14 supports the entire signal chain, from the detector to the application integration.

The wide-band high dynamic range analog front-en offers options for a variety of advanced detectors.

Due to the vast amounts of data produced the processing support is key and thereforeADQ14 includes several layers of signal processing support. The open FPGA and application-specific firmware enables real-time integration and very compact system design. The peer-to-peer streaming combines the signal processing strengths of a GPU with the versatile acquisition capabilities of the ADQ14. The software development kit is available both for Windows and Linux and a number of host interface options are available to simplify the systems integration.



1 Selection guide

There are several options for ADQ14. This guide will help you through the selection of options. Follow the procedure listed to find the best product for the current application. Each of the items in the list are described further in this document. The table below to shows which combinations that are available.

1. Select AC- or DC-coupled front-end. This will give the model ADQ14AC or ADQ14DC.
2. Select the number of channels and the sample rate; –2A, –2C, –1X, –4A, –4C or –2X.
3. Select host interface form factor; –USB, –PXIE, –PCIE, –SSPCIE, –MTCA or –10GBE.
4. Select one or several of the firmware packages; –FWDAQ, –FWATD, –FWPD, –FWSDR.
5. Select feature enhancement option; –GPIO, –VG or –OCT.
6. Add ADQ14 Development Kit for custom real-time signal processing in the FPGA.
7. Select warranty period –W5Y.

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Key parameters												
Number of channels	2	2	1	4	4	2	2	2	1	4	4	2
Sample rate / channel [GSPS]	0.5	1	2	0.5	1	2	0.5	1	2	0.5	1	2
Analog front-end (Factory installed)												
AC-Coupling	✓	✓	✓	✓	✓	✓						
DC-Coupling							✓	✓	✓	✓	✓	✓
50 Ω input impedance	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Variable DC-offset [1]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Variable input range [2] [3] –VG							✓	✓	✓	✓	✓	✓
Over-voltage protection [4]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Anti-aliasing filter							✓	✓	✓	✓	✓	✓
Firmware (Field upgrade supported)												
ADQ14 Development Kit [5]	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Acquisition [6] –FWDAQ	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Adv. time domain –FWATD	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Pulse data –FWPD		✓	✓		✓	✓		✓	✓		✓	✓
Radio Systems –FWSDR		✓			✓	✓		✓			✓	✓
Host interface form factor (Factory installed)												
USB3 [7] –USB	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCIe –PCIE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCIe –SSPCIE												✓
PXIe –PXIE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
M-TCA.4 [3] [8] –MTCA											✓	✓
10 GbE UDP p-p [7] –10GBE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
12 pins GPIO [2] [8] –GPIO	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
OCT front panel [9] –OCT												✓
Warranty extension												
Warranty 5 years [10] [11] –W5Y	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

1. Software controlled setting
2. The –GPIO option is included with the variable gain option, –VG.
3. The –VG option is not available for –MTCA nor –SSPCIE form factor.
4. Software controlled on or off.
5. The ADQ14 Development Kit is available for –FWDAQ, –FWPD, –FWSDR.
6. Included with the ADQ14.
7. Select power supply for US market or power supply for EU market.
8. The –GPIO option is available as standard on the –MTCA form factor.
9. Available for –SSPCIE form factor only.
10. Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. This option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.
11. Warranty extension must be ordered before included 3 years warranty is expired.

2 Technical data

All values are typical unless otherwise noticed.

Table 1: General Parameters

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Key parameters												
Channels	2	2	1	4	4	2	2	2	1	4	4	2
Sample rate / channel [GSPS]	0.5	1	2	0.5	1	2	0.5	1	2	0.5	1	2
Resolution [bits]	14						14					
Data memory[1] [GByte]	2						2					
Power												
Power supply [V]	12						12					
Power dissipation [W]	36	36	36	42	42	42	39	39	39	48	48	48

1. The data memory is shared between data (2 bytes per sample) and record headers.

Table 2: Analog input

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Analog inputs												
Coupling	AC						DC					
Input Impedance AC [Ω]	50						50					
Input Impedance DC [Ω]	100k						50					
Input range [V_{pp}]	1.9						0.5	0.5	1	0.5	0.5	1
Bandwidth lower –3 dB [Hz]	80	80	100	80	80	100	DC					
Bandwidth upper –1 dB [MHz]	900	900	800	900	900	800	180	500	900	180	500	900
Bandwidth upper –3 dB [MHz]	1200	1200	1000	1200	1200	1000	250	700	1200	250	700	1200
Connector	SMA						SMA					
Variable DC-offset range [V]	±0.95						±0.25		±0.5	±0.25		±0.5
Variable DC-offset steps	31						31					
Variable gain –VG option												
Input range 0.2 Vpp	–						✓	✓	–	✓	✓	–
Input range 0.5, 1, 2, 5 Vpp	–						✓	✓	✓	✓	✓	✓
Bandwidth –1 dB –VG[1] [MHz]	–						180	400	700	180	400	700
Bandwidth –1 dB –VG[2] [MHz]	–						180	300	450	180	300	450
Bandwidth –3 dB –VG[1] [MHz]	–						250	500	900	250	500	900
Bandwidth –3 dB –VG[2] [MHz]	–						250	400	700	250	400	700
Variable DC-offset range[3]	–						Full scale					
Variable DC-offset steps	–						31					

1. Ranges 0.2 Vpp 0.5 Vpp.
2. Ranges 1 Vpp, 2 Vpp and 5 Vpp.
3. The variable DC-offset covers the full range of each respective range setting. For example, the 1 Vpp range has a DC-offset setting covering ±0.5 V.

Table 3: Over-voltage protection

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Overvoltage protection												
Max input voltage [V]	–						±4					
Max input current [mA]	±100						–		–		–	
–VG range 0.2 V_{pp} [V]	–						±1.25		–		±1.25	
–VG range 0.5 V_{pp} [V]	–						±4					
–VG range 1 V_{pp} [V]	–						±4					
–VG range 2 V_{pp} [V]	–						±4					
–VG range 5 V_{pp} [V]	–						±5					

Table 4: Dynamic performance

MODEL	ADQ14AC[1] (TBC)						ADQ14DC[1]					
OPTION	–2A	–2C	–1X[2]	–4A	–4C	–2X[2]	–2A	–2C	–1X[2]	–4A	–4C	–2X[2]
Analog performance with overvoltage protection activated												
SNR [dB]	64	64	64	64	64	64	62	60	58	62	60	58
SNDR [dB]	59	59	59	59	59	59	62	60	58	62	60	58
SFDR [dBc]	61	61	61	61	61	61	75	75	75	75	75	75
ENOB [bits]	9.6	9.6	9.6	9.6	9.6	9.6	10	9.7	9.3	10	9.7	9.3
Analog performance without overvoltage protection												
SNR [dB]	64	64	64	64	64	64	–					
SNDR [dB]	63	63	63	63	63	63	–					
SFDR [dBc]	69	69	69	69	69	69	–					
ENOB [bits]	10.2	10.2	10.2	10.2	10.2	10.2	–					
Analog performance –VG option range 0.5 1 2 5 Vpp												
ENOB [bits]	–						10	9.7	9.3	10	9.7	9.3
SFDR [dBc]	–						75	75	75	75	75	75
Analog performance –VG option range 0.2 Vpp												
ENOB [bits]	–						9.4	9.1	–	9.4	9.1	–
SFDR [dBc]	–						75	75	–	75	75	–

1. At 71 MHz -1dBFS input signal.
2. Dynamic performance ignoring interleaving tones. Interleaving tones are removed by ADX. ADX is included in the –FWSDR firmware option.

Table 5: Clock

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Internal Clock Reference												
Frequency [MHz]	10						10					
Accuracy [ppm]	± 3 ± 1/year						± 3 ± 1/year					
External clock reference input												
Frequency (min – max) [MHz]	10 MHz ± 5 ppm						10 MHz ± 5 ppm					
Signal level (min – max) [Vpp]	0.5 – 3.3						0.5 – 3.3					
Impedance AC [Ω]	50						50					
Impedance AC (high[1]) [Ω]	200						200					
Impedance DC [Ω]	10 k						10 k					
Connector	SMA						SMA					
PXIe clock reference[2]												
PXIe clock [MHz]	100						100					
PXIe sync[3] [MHz]	10						10					
Clock reference output												
Frequency [MHz]	Set by selected clock reference						Set by selected clock reference					
Signal level [Vpp]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance AC [Ω]	50						50					
Impedance DC [Ω]	10 k						10 k					
Duty cycle	50% ± 5%						50% ± 5%					
Connector	SMA						SMA					
External clock source												
Frequency [GHz]	1						1					

1. Software-controlled high-impedance setting for large fan-out situations.
2. Available on ADQ14 with option –PXIE in a chassis that supports PXIe.
3. Jitter of PXIe sync is reduced by PXIe clock in the ADQ14.

Table 6: Trigger

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
External trigger input												
Trigger frequency (max) [MHz]	>1						>1					
Signal level (min – max) [V]	–0.5 to 3.3						–0.5 to 3.3					
Threshold[1] [V]	Programmable						Programmable					
Sensitivity [mV]	200						200					
Time resolution [ps]	125						125					
Excess jitter[2] [ps]	25						25					
Impedance DC [Ω]	50						50					
Impedance DC (high[3]) [Ω]	>500						>500					
GPIO data rate[4] [MHz]	125						125					
Connector	SMA						SMA					
Trigger output												
PRF (max) [MHz]	100						100					
Signal level output low max [V]	0.1						0.1					
Signal level output high min [V]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance DC [Ω]	50						50					
GPIO data rate[4] [Mbit/s]	100						100					
Connector	Shared with trigger input						Shared with trigger input					

1. Set threshold to match requested electrical standard when operated as GPIO input.
2. The trigger is synchronous to the sampling and can be resolved with sub-sample precision. The excess jitter is jitter added to the trigger signal inside the ADQ14.
3. Software-controlled high-impedance setting for large fan-out situations.
4. When used as GPIO.

Table 7: Multi-Unit Synchronization

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
External sync input												
PRF (max) [MHz]	>1						>1					
Signal level input low max [V]	0.8						0.8					
Signal level input high min [V]	2						2					
Impedance DC [Ω]	50						50					
Impedance DC (high[1]) [Ω]	>500						>500					
GPIO data rate [Mbit/s]	100						100					
Connector (–PCIE)	MCX inside PC chassis						MCX inside PC chassis					
Connector (other form factor)	SMA shared with Sync out						SMA shared with Sync out					
Sync output												
PRF (max) [MHz]	>1						>1					
Signal level output low max [V]	0.1						0.1					
Signal level output high min [V]	1.2 (into 50 Ω load)						1.2 (into 50 Ω load)					
Impedance DC [Ω]	50						50					
GPIO data rate [MHz]	100						100					
Connector (–PCIE)	MCX inside PC chassis						MCX inside PC chassis					
Connector (other form factor)	SMA shared with Sync input						SMA shared with Sync input					

1. Software-controlled high-impedance setting for large fan-out situations.

Table 8: GPIO: included in option –GPIO, option –VG and on form factor –MTCA.

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Number of GPIO signals	12						12					
Signal level input high min [V]	0.8						0.8					
Signal level input low max [V]	2						2					
Input impedance [Ω]	10k						10k					
Signal level output low max [V]	0.1 (no load)						0.1 (no load)					
Signal level output high min [V]	3.1 (no load)						3.1 (no load)					
Output impedance [Ω]	90						90					
Max data rate [Mbit/s per pin]	100						100					
GPIO power out [V]	3.3						3.3					
GPIO power out [mA]	100						100					
Connector	Hirose ST60-24P(50)											
Cable	See ordering information											

Table 9: Environment

INTERFACE TO HOST PC	USB3.0	PCI EXPRESS		PXI EXPRESS	MTCA.4	10GBE
OPTION	–USB	–PCIE	–SSPCIE	–PXIE	–MTCA	–10GBE
Data rate						
Communication standard	USB3.0	Gen2 by 8 lanes		Gen2 by 8 lanes	Gen2 by 4	10GbE
Data rate sustained [1] [MByte/s]	200	3200		3200	1600	1000
Mechanical						
Box size [mm^3]	191 x108 x 62	–		–	–	231.7 x 108 x 62
Weight [g]	750	–		–	–	
Bus width mechanical [lanes]	–	16[2]		–	–	–
Board width (ADQ14AC) [slot]	–	2	–	1 slot 4TE	–	–
Board width (ADQ14DC) [slot]	–	2	1	2 slot 8TE	Double width	–
Board length [mm]	–	short	237	160	160	–
Board height	–	–	–	3U	Mid size	–
Electrical						
Power supply	External[3]	6-pin ATX power		From chassis	From chassis	External[3]
Bus width electrical [lanes]	–	8		8	4	
Temperature range						
Operation [°C]	0 to 45	0 to 45 [4]		0 to 45 [5]	0 to 45	0 to 45
Compliances						
CE	✓	✓		✓	✓	✓
RoHS2	✓	✓		✓	✓	✓
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c)					

1. This is depending on the capacity of the complete system including the host computer.
2. The wide contact is required to support the weight of the board.
3. Use only the power supply which is included in the delivery of ADQ14–USB.
4. This is the temperature in to the fan of the ADQ14.
5. High fan setting required if available on the chassis.

Table 10: Firmware options: functions overview

MODEL OPTION	ADQ14AC ANDADQ14DC –FWDAQ	–FWATD	–FWPD	–FWSDR	COMMENT
Signal enhancement IP					
DBS	✓	✓	✓		
ADX				✓	Interleaved models
Trigger modes					
Software trigger	✓	✓		✓	
External trigger	✓	✓	✓	✓	
Common level trigger	✓	✓			All channels trigger on one selected channel
Individual level trigger			✓		Each channel trigger independently
PXIe backplane trigger	✓			✓	DStarB signal. Requires option –PXIE in a chassis with PXIe star trigger support.
Internal trigger	✓	✓		✓	
Trigger output					
Internal trigger	✓	✓	✓	✓	
Trigger event	✓	✓	✓	✓	
Clock					
All clock modes	✓	✓	✓	✓	
Sample skip	✓	✓			A DDC contains a low pass filter combined with sample skip.
Digital Down Converter				✓	
Multi-unit sync	✓	✓	✓	✓	See app note 15-1583
Data acquisition modes					
Streaming with infinite record length	✓			✓	
Streaming with header	✓	✓	✓	✓	
Streaming without header	✓			✓	
Multi-record	✓			✓	

Table 11: Data acquisition parameters for –FWDAQ

MODEL		ADQ14AC AND ADQ14DC					
OPTION		–2A	–2C	–1X	–4A	–4C	–2X
Streaming							
Re-arm time	[ns]	8	8	16	8	8	16
Pre-trigger max	[samples]	16 ki	16 ki	16 ki	16 ki	16 ki	16 ki
Pre-trigger step	[samples]	4	4	8	4	4	8
Trigger delay max	[samples]	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$
Trigger delay step	[samples]	4	4	8	4	4	8
Record length max	[samples]	2 Gi	2 Gi	2 Gi	2 Gi	2 Gi	2 Gi
Record length min	[samples]	8	8	16	8	8	16
Record length step	[samples]	1	1	1	1	1	1
Multi-record[1]							
Re-arm time	[ns]	TBD	TBD	TBD	TBD	TBD	TBD
Pre-trigger max	[samples]	Record length					
Pre-trigger step	[samples]	4	4	8	4	4	8
Trigger delay max	[samples]	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$	$2^{32} - 1$
Trigger delay step	[samples]	4	4	8	4	4	8
Record length max	[samples]	500 Mi	500 Mi	1000 Mi	250 Mi	250 Mi	500 Mi
Record length min	[samples]	TBD	TBD	TBD	TBD	TBD	TBD
Record length step	[samples]	TBD	TBD	TBD	TBD	TBD	TBD

1. Use these parameter for pre-trigger length larger that 16kiSamples. If pre-trigger is shorter than 16kiSamples use the streaming parameters.

Table 12: Software support[1]

MODEL	ADQ14AC						ADQ14DC					
OPTION	–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Operating systems												
Windows 10	✓						✓					
Linux[2]	✓						✓					
Application integration												
Digitzer Studio [3]	Acquisition and analysis GUI						Acquisition and analysis GUI Compatilbe firmware options –FWDAQ, –FWATD and–FWSDR					
MATLAB[4]	API, examples						API, examples					
C/C++	API, examples						API, examples					
.Net (C#, Visual Basic)	API, examples						API, examples					
Python	Example scripts						Example scripts					
LabVIEW	Low level functions and example code						Low level functions and example code					

1. Full performance is only guaranteed using supplied examples in C/C++ programming language.
2. See www.spdevices.com document “15-1494 Digitizer operating system support” for a complete listing.
3. See 20-2381 Digitizer Studio Datasheet for supported hardware options, firmware options and operating systems.
4. Windows only and –FWDAQ only.

3 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The ADQ14–USB and ADQ14–PCIE has a built-in fan to cool the device. ADQ14–PXIE is cooled from the chassis fan. The built-in temperature monitoring unit will protect the ADQ14 from overheating by temporarily shutting down parts of the device in an overheat situation.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

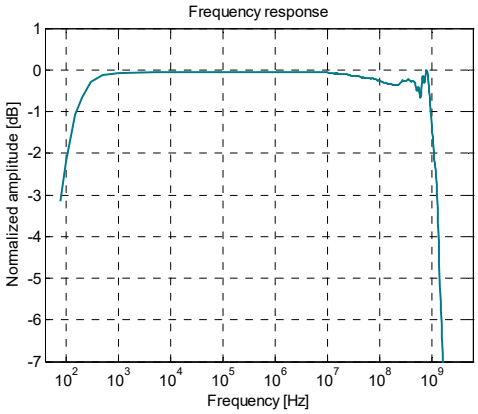
Table 13: Absolute Maximum Ratings

MODEL		ADQ14AC						ADQ14DC					
OPTION		–2A	–2C	–1X	–4A	–4C	–2X	–2A	–2C	–1X	–4A	–4C	–2X
Analog input													
AC (with ovp[1])		See Table 3						See Table 3					
AC w/o ovp f >10 MHz	[Vpp]	5						0.5	0.5	1	0.5	0.5	1
AC w/o ovp f <10 MHz	[Vpp]	2.75						0.5	0.5	1	0.5	0.5	1
DC max[2]	[V]	+7						See Table 3					
DC min[2]	[V]	–3						See Table 3					
External clock reference													
Signal level AC	[Vpp]	5						5					
Signal level DC	[V]	± 5						± 5					
External trigger input													
Signal level to GND min	[V]	–2.3						–2.3					
Signal level to GND max	[V]	+5						+5					
External sync input													
Signal level to GND min	[V]	–0.5						–0.5					
Signal level to GND max	[V]	+3.8						+3.8					
Power supply													
Voltage to GND (min)	[V]	–0.4						–0.4					
Voltage to GND (max)	[V]	14						14					
Temperature													
Operating (min)	[°C]	0						0					
Operating (max)	[°C]	45						45					
Standard GPIO													
Trigger input		See trigger specification Table 6						See trigger specification Table 6					
Sync		See sync specification Table 7						See sync specification Table 7					
GPIO Expansion –GPIO													
Voltage to GND (min)	[V]	–0.5						–0.5					
Voltage to GND (max)[3]	[V]	4.6						4.6					
Max output current / pin	[mA]	33						33					
Max total output current	[mA]	200						200					
Variable gain –VG													
Relay switching cycles		N/A						10^6					

1. Overvoltage protection.
2. The combination of AC and DC level must never exceed DC level limits.
3. A voltage on a GPIO input higher than 3.3 V may change the output voltage on GPIOs which are set to outputs. This may damage external equipment.

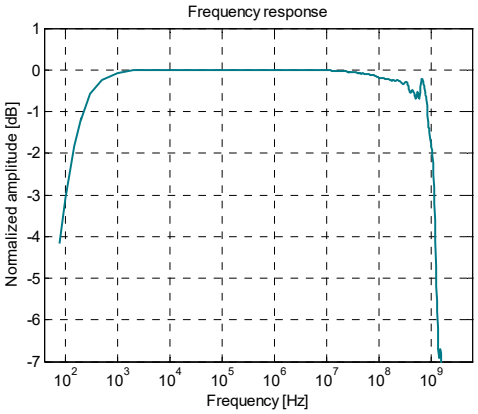
4 Frequency response

All values are typical.



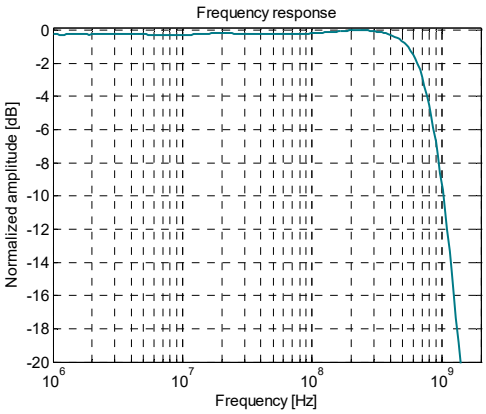
Bandwidth (–3 dB)	1200 MHz
1 dB flatness	900 MHz

Figure 1: ADQ14AC–4C



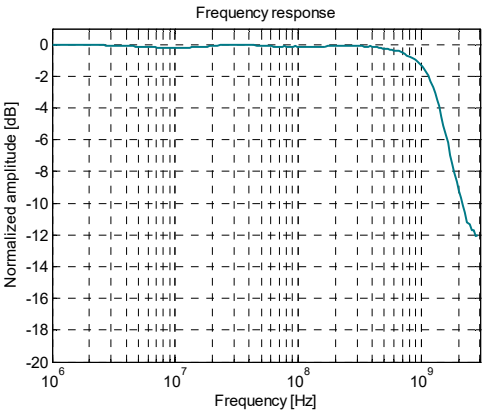
Bandwidth (–3 dB)	1000 MHz
1 dB flatness	800 MHz

Figure 2: ADQ14AC–2X



Bandwidth (–3 dB)	700 MHz
1 dB flatness	500 MHz

Figure 3: ADQ14DC–4C



Bandwidth (–3 dB)	1200 MHz
1 dB flatness	900 MHz

Figure 4: ADQ14DC–2X

5 Spectral performance

All values are typical.

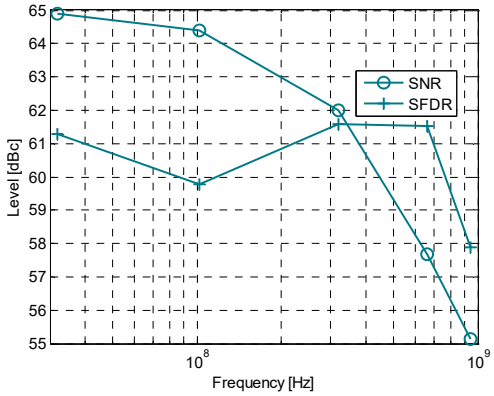


Figure 5: ADQ14AC–4C with overvoltage protection.

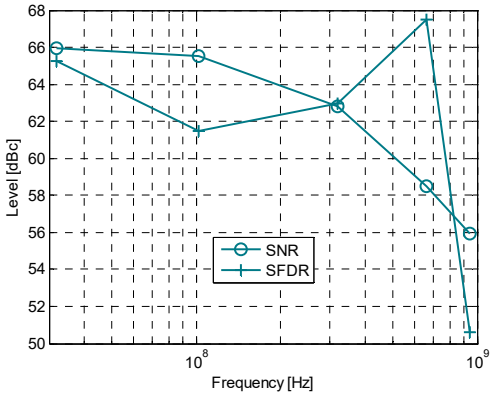


Figure 6: ADQ14AC–2X with overvoltage protection, interleaving spurs excluded.

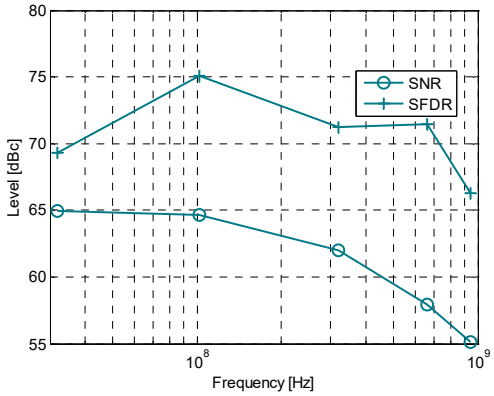


Figure 7: ADQ14AC–4C without overvoltage protection.

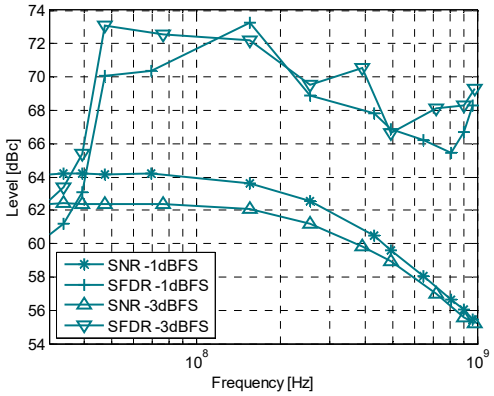


Figure 8: ADQ14AC–2X without overvoltage protection, interleaving spurs excluded.

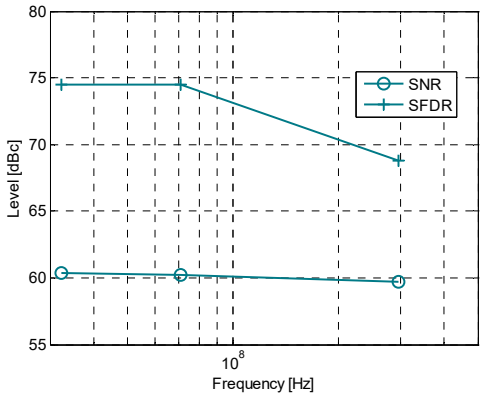


Figure 9: ADQ14DC–4C

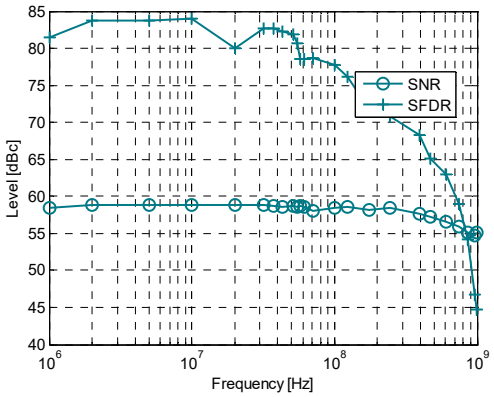


Figure 10: ADQ14DC–2X, interleaving spurs excluded.

6 Frequency domain

All values are typical.

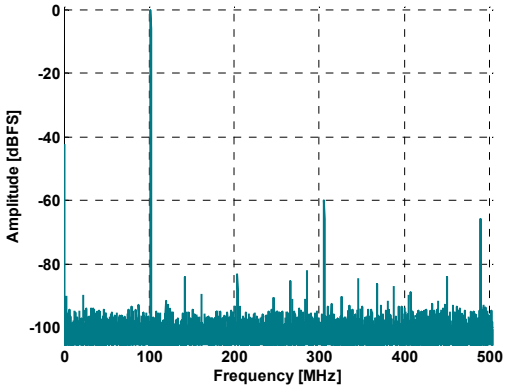


Figure 11: ADQ14AC–4C: 103 MHz with overvoltage protection

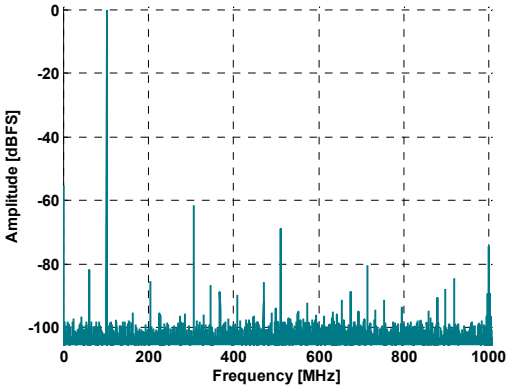


Figure 12: ADQ14AC–2X–FWSDR: 103 MHz with overvoltage protection

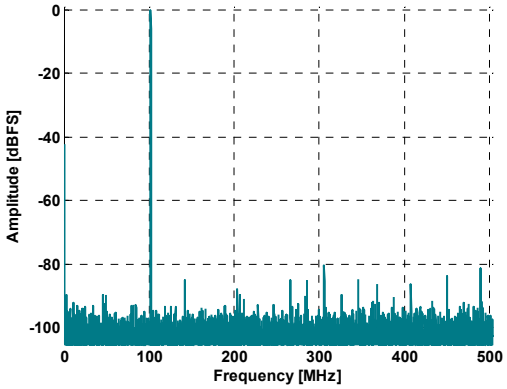


Figure 13: ADQ14AC–4C: 100 MHz without overvoltage protection

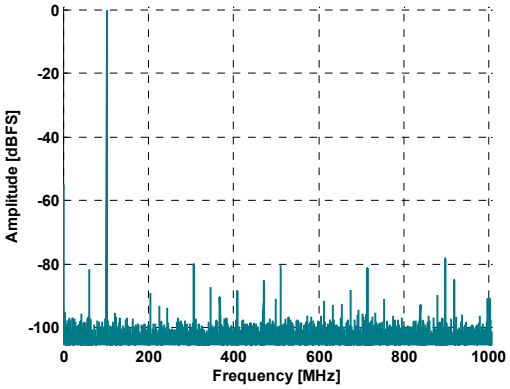


Figure 14: ADQ14AC–2X–FWSDR: 100 MHz without overvoltage protection

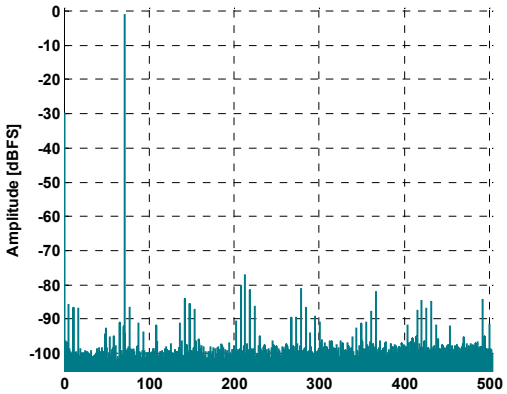


Figure 15: ADQ14DC–4C: 71 MHz

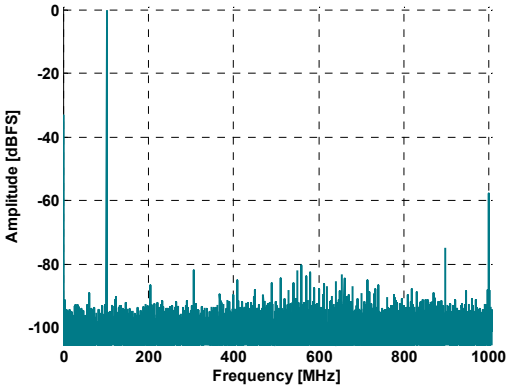


Figure 16: ADQ14DC–2X–FWSDR: 100 MHz

7 Integrating the ADQ14

Figure 17 illustrates how ADQ14 supports the key parts of the system integration.

7.1 Detecting the analog signal

The analog front-end combines high dynamic range with high bandwidth to support the most advanced detectors. The DC-coupled front-end has high sensitivity to simplify the interfacing. Variable gain (option –VG) and DC-offset adds flexibility. The AC-coupled front-end is optimized for linearity at high frequencies, which is required for some applications.

7.2 Timing and synchronization

The clock management and trigger support connects with the infrastructure of the system. The ADQ14 can act as master and generate timing for the entire system and thereby save additional timing cards. It can also receive trigger and clocks from other devices. Synchronization and GPIO signals allow advanced sequencing.

Synchronization might be needed between ADQ14 and other types of equipment. This is supported by the clock and trigger signals.

In a multi-channel system, synchronization between several ADQ14 is needed. The application note 15-1583 “ADQ14 synchronizing several units” shows how to synchronize several ADQ14 units in a large scale installation.

7.3 Real-time signal processing

The data acquisition engine in the FPGA supports several methods for acquiring data and transfer it to the host PC. Since the data rate from the ADC is high, some parts of the application is preferably integrated into the FPGA as to relax the load on the CPU in the host computer. There is a set of application-specific firmware options available to enable efficient real-time signal processing. In addition, the FPGA is opened to the user through the ADQ14 Development Kit for integration of custom algorithms.

7.4 System integration

The interface to the host PC is one important parameter in the system integration. To enable an optimal solution, the ADQ14 offers a wide variety of form factors. Both the mechanical and electrical properties in various standards are important for the result. The mechanical properties enables an optimal placement of the ADQ14 inside the target system and also which type of PC to use. The different electrical properties of the interface determine data transfer rate and noise immunity.

7.5 Building the application

The open ADQAPI is a software package including drivers and software development kit for integrating the ADQ14 into an application. A number of examples and application notes simplifiesy the integration process and shortens the time-to-market.

Partitioning the application between a high level analysis software in the host PC and a low level real-time data analysis in the open FPGA enables high performance applications to run on a cost-efficient PC solution.

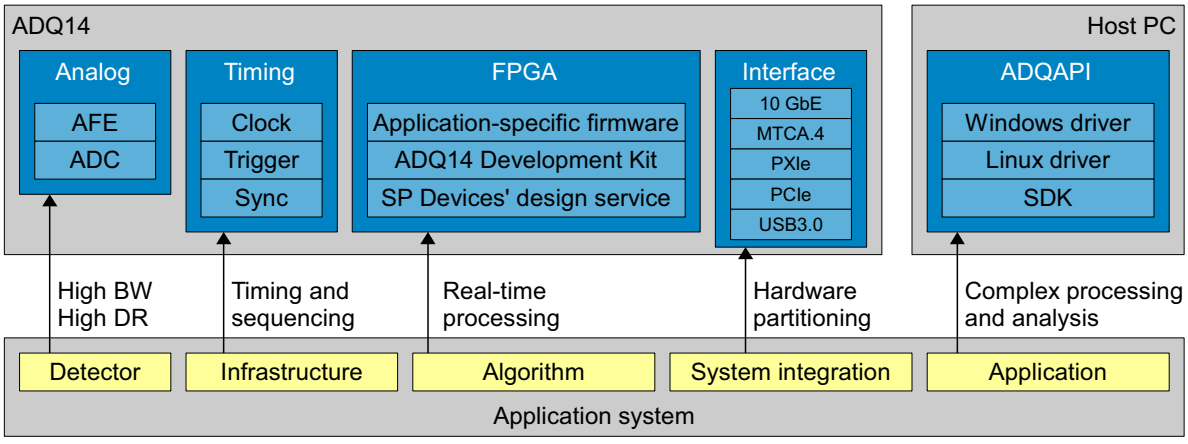


Figure 17: Integrating the ADQ14 into the system.

8 Software tools

8.1 Operating systems

The software package includes drivers for the most common versions of Windows and several Linux distributions.

8.2 Software Development Kit

The ADQ14 digitizer is easily integrated into the application by using the Software Development Kit (SDK). The SDK is included free of charge with the ADQ14. The SDK includes programming examples and reference projects for several platforms. All functions are described in detail in 14-1351 ADQAPI Reference Guide. Please note that full performance is guaranteed for the C/C++ interface only. The SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

8.3 Digitzer Studio GUI for –FWDAQ

The ADQ14 is supplied with the Digitzer Studio software providing quick and easy control of the digitizer, see **Figure 18**. The tool offers both time-domain and frequency-domain analysis. Data can be saved in different file formats for off-line analysis. With Digitzer Studio, the ADQ14 operates as a stand-alone measurement instrument.

Note that the GUI Digitzer Studio only represent a subset of the flexibility of the ADQ14. The full potential of the ADQ14 is reached using the SDK. For more information on Digitzer Studio see 20-2381 Datasheet and 20-2382 User Guide.

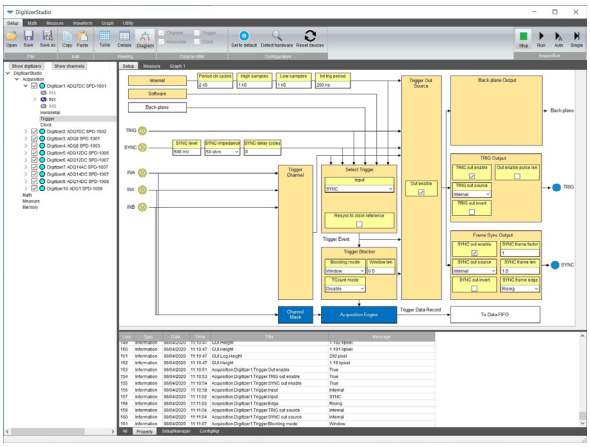


Figure 18: Digitzer Studio.

9 Block diagram

The ADQ14 can be configured in many ways. A detailed block diagram for one of the available configurations is shown in **Figure 19**. The following sections describe the parts of the ADQ14 in detail. Also see the 15-1593 ADQ14 Manual for more details on how to operate the ADQ14.

This datasheet describes functions included in the standard data acquisition firmware package –FWDAQ. Functionality in optional application specific firmware packages is described in their respective datasheets.

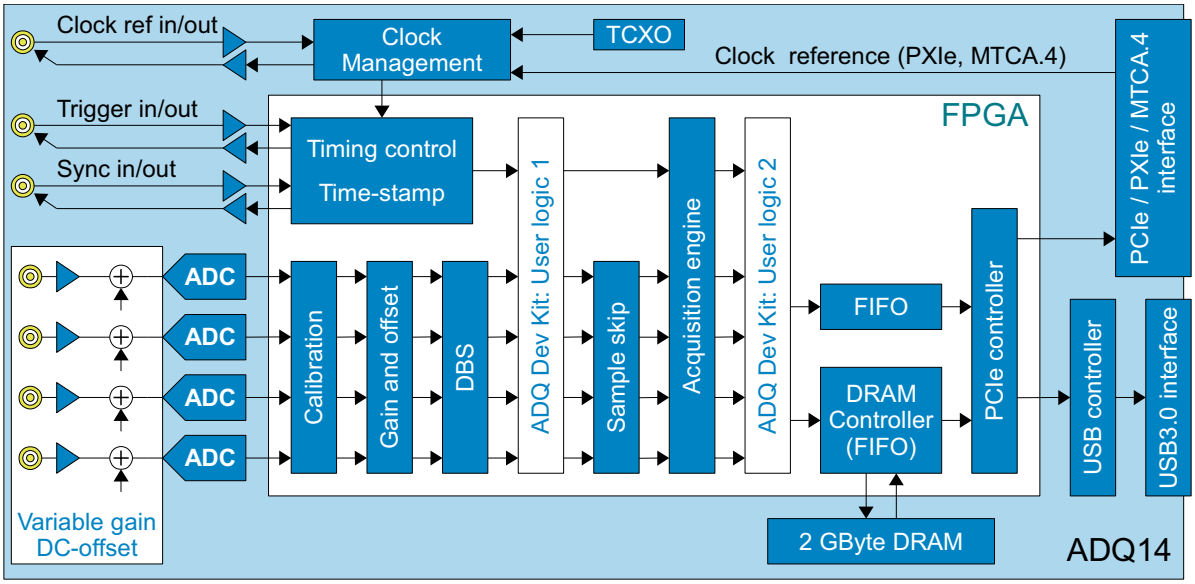
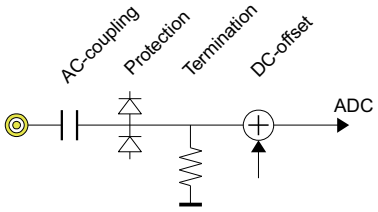


Figure 19: Block diagram for ADQ14DC–4C (quad-channel, DC-coupled).

10 Analog front-end options

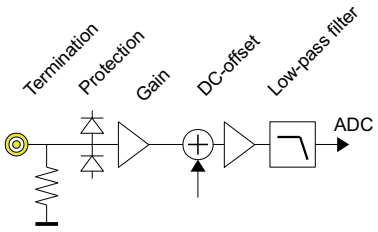


AC-coupling (ADQ14AC)

For RF measurements where linearity at high frequency is important.

The AC-coupled analog front-end contains AC termination and overvoltage protection. The overvoltage protection, can be turned off for higher linearity at high frequencies. This is done with a software command. There is also a software programmable DC-offset. This front-end option is preferred when the application's frequency content is above 300 MHz[1] and the linearity requirements are high. Compared to the DC coupled front end, it has better noise performance over the entire bandwidth.

Note that the AC-coupled AFE is not recommended for signals below 30 MHz[1] when linearity is critical.

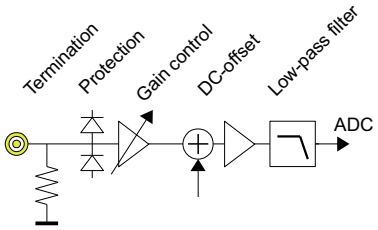


DC-coupling (ADQ14DC)

For pulse data measurements.

The DC-coupled analog front-end contains overvoltage protection and a software programmable DC-offset. Overvoltage protection is crucial in pulse data systems where high voltage detectors are driving the input. It reduces the damage at accidental discharges.

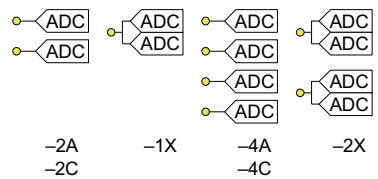
The DC-coupled AFE also has a noise-suppression anti-aliasing filter. When linearity below 300 MHz[1] is important, this is the recommended AFE.



Variable gain option (ADQ14DC–VG)

Enables full flexible usage of the ADQ14DC.

The ADQ14DC can be equipped with software-controlled variable gain. Note that the DC-offset is rail-to-rail regardless of the gain setting.



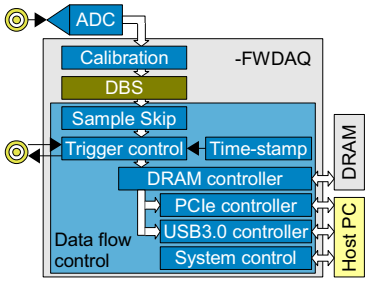
Sample rate and number of channels (–2A, –2C, –1X, –4A, –4C, –2X)

The sample rate and channels combinations are there to meet various measurement situations.

ADQ14 is available with 1, 2 or 4 channels depending on the selected sample rate. The non-interleaved versions sample with 500 MSPS (–2A and –4A) or 1000 MSPS (–2C and –4C). The interleaved versions (–1X and –2X) have a sampling rate of 2000 MSPS. Interleaving performance is enhanced by Teledyne SP Devices' proprietary technologies for interleaving, DBS and ADX[2].

1. Approximate limit.
2. ADX is available in firmware options –FWSDR.

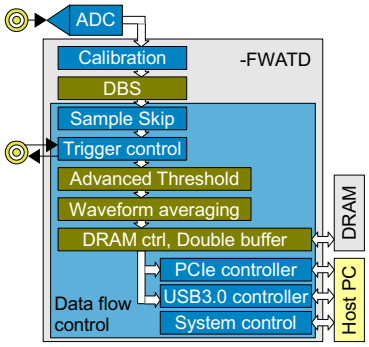
11 Firmware options



Data acquisition firmware (–FWDAQ)

For general purpose high speed data recording.

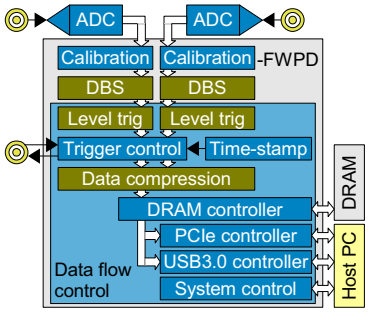
The data acquisition firmware –FWDAQ is the default firmware for ADQ14 and is always included. Supported data acquisition modes are continuous multi-record, and streaming, **Section 12**. The supported trigger modes are external, internal, software and level trigger, as well as internal and external clock reference, **Section 14** and **15**).



Advanced time-domain (–FWATD)

For time-domain analysis of synchronized repetitive events.

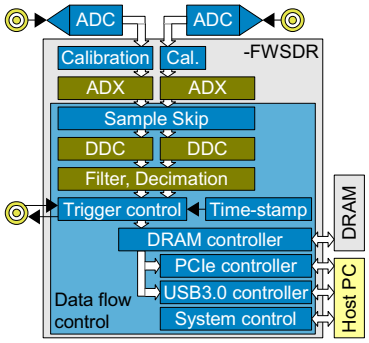
The option –FWATD includes an advanced threshold algorithm for non-linear discrimination of noise. There is also a waveform averaging (WFA) for real-time accumulation of repetitive events, that contributes to improved SNR. The WFA can take waveforms up to 1 MSamples in length. The WFA may also be split into several accumulations of a total length up to 1 MSamples to simplify read-out scheduling. A stable baseline is achieved by the DSB, **Section 19**.



Pulse data (–FWPD)

For capturing random events.

With –FWPD, each channel can be individually event-triggered to capture random events. The trigger levels are user-defined levels or filtered data for adaptive thresholding. To support random event lengths, the record lengths are dynamic. Data compression through zero suppression saves disk space.Thanks to the DRAM bursts of events can be buffered before transferring data to the host PC, **Section 12**. A stable baseline is achieved by the DSB, **Section 19**.



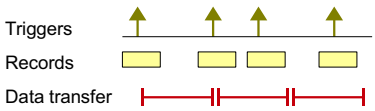
Software defined radio (–FWSDR)

Software defined radio functionality.

The option –FWSDR includes digital down conversion and decimation, **Section 19**. After decimation the data rate is well adapted to streaming to the host PC.

Teledyne SP Devices' proprietary interleaving correction method ADX is included in the time-interleaved models.

12 Data recording



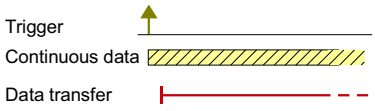
Streaming

Use streaming for maximum throughput.

At each trigger, a record (a set of continuous data) is captured. The record is buffered in the DRAM, which act as a FIFO, and transfered to the host PC. This large 2 GBytes FIFO enables bursts of triggers at very high rate. The large FIFO also guarantee reliable high speed transfer to the PC.

Each record has a header with time-stamp and identifiers for post-processing analysis of the data.

Streaming is described in 20-2465.

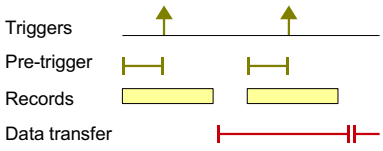


Streaming with infinite record length

Continuous recording of very long events.

The recording is starting at a trigger event and continue until it is terminated by the user. The streaming of infinite record produce a large amount of data and is often combined with a data reduction method in the FPGA. This is, for example, channel masking, DDC and decimation (option –FWSDR), sample skip, or custom implementations using the ADQ14 Development Kit.

Streaming is described in 20-2465.

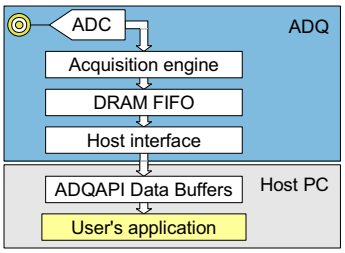


Multi-record

Enables an exceptionally long pre-trigger.

This mode is allows for very long pre-triggers; up to the entire record length. This long pre-trigger can be used for tracking the cause of an event. The parameters for multi-record data acquisition is found in **Table 11**.

For pre-trigger length below 16 kiSamples, us the streaming parameters. For pre-trigger length above 16kiSamples use the multi-record parameters.

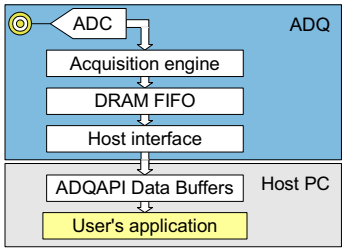


Data FIFO

Guarantees reliable data transfer.

The digitizer has 2 GBytes on-board DRAM, organized as a large FIFO. The FIFO guarantees stable operation over long time at high data rate. The FIFO also enable high trigger burst rate.

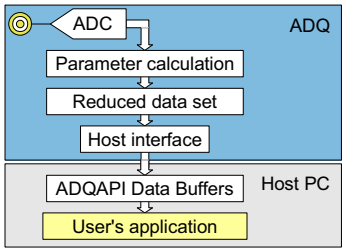
13 Data Transfer



Data transfer –FWDAQ

For maximum throughput.

ADQ14 support for several electrical/mechanical interfaces to meet specific systems design requirements. The software methods for data transfer are unified to work the same for all formats. The API supports efficient multi-threaded handling of data buffers. There is example code for fast integration into the application. The PCIe interface of the standard firmware –FWDAQ is Gen2x8 and supports up to 3.2 GBytes/s, **Table 9**.

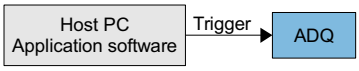


Real-time processing with –FWATD and –FWPD

Real-time processing for optimized data set.

The powerful real-time processing of the pulse detection firmware –FWPD and the averaging firmware –FWATD calculate descriptive parameters form the raw data stream. By transferring only these parameters and not all raw data, the amount of data to be transferred to the host PC is greatly reduced. The concept of calculating key parameters in the FPGA of the ADQ14 is extended further by the open FPGA concept; ADQ14 Development Kit. Since the data rate is reduced, this concept also match USB3.0.

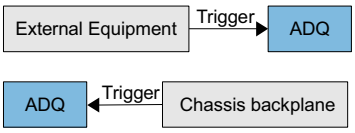
14 Trigger module



Software trigger

User-controlled triggering.

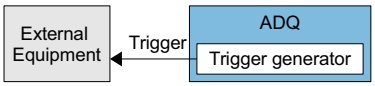
The software trigger is activated from the user's application software. It is used for building oscilloscope applications and for watchdog functions.



External trigger

Synchronizing the acquisition with an experiment.

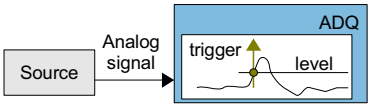
The external trigger is a signal from another unit that activates the acquisition. The external trigger is available on the front panel or in the backplane on PXIe format.



Internal trigger

Internally generated signal for triggering other devices.

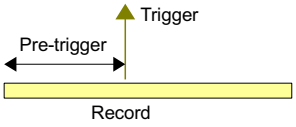
With the internal trigger, the ADQ14 can be the timing master of a large system saving additional timing cards. The internal trigger generate a periodic trigger signal to other hardware units.



Level trigger

Data driven triggering.

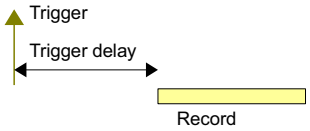
Activity on a data channel will trigger the acquisition. All channels are triggered simultaneously. More advanced level trigger functionality is included in the pulse detection firmware option –FWPD.



Pre-trigger

Capturing data before the trigger.

The pre-trigger buffer allows for capturing data long before the trigger event occurred. This is useful for analyzing the cause of an event.

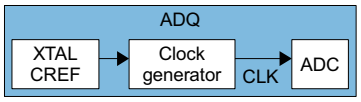


Trigger delay

Capturing data long after the trigger event.

With this function the time span for a measurement can be exceedingly large. By capturing only the event of interest, the amount of data is reduced.

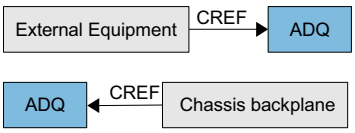
15 Clock module



Internal clock

High precision clock for stand-alone operation.

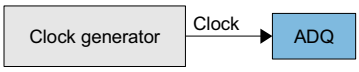
The internal clock is based on an internal high precision reference source. The internal clock enables stand-alone operation.



External clock reference

Synchronize the acquisition to an experiment.

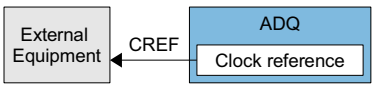
The digitizer can be synchronized with an experiment using the external clock reference. The internal clock generator gets its reference from an external source. There is a connector for this on the front panel. The PXIe and MTCA.4 form factors ca also take the clock reference from the backplane.



External clock

Synchronize the acquisition to an experiment.

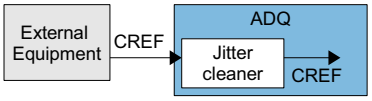
If an external clock is available, the ADQ14 can be clocked directly by that source.



Clock reference output

Synchronize the acquisition to an experiment.

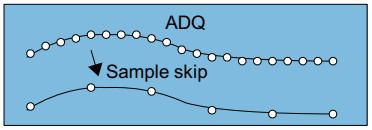
The digitizer can also be synchronized with an experiment using the clock reference output. ADQ14 then acts as clock reference source for the entire system. The clock reference output can e.g. clock another ADQ14. This function together with the trigger generator can replace external timing cards.



Jitter cleaner

For optimized performance with an external clock reference.

Using an external clock reference, the performance can be enhanced by a jitter cleaner. With an external clock reference of 10 MHz, the internal jitter cleaner will optimize the performance.



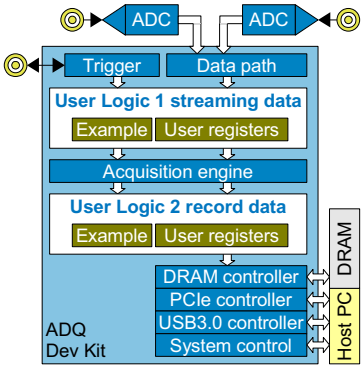
Sample skip[1]

Adapt the sample rate to the situation and optimize the amount of data.

The sample skip function can *adapt the sample rate to the current situation and thus reduce the amount of data.*The ADQ14 can thereby easily adapt to changing conditions.

1. Sample skip can neither be combined with level trigger nor with firmware option –FWPD.

16 Feature enhancement options



Real-time custom signal processing firmware through the ADQ14 Development Kit

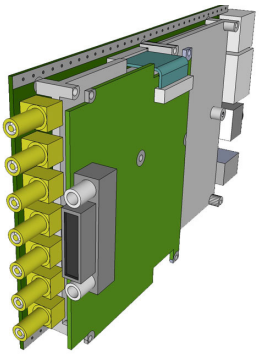
The ADQ14 is equipped with an powerful Xilinx Kintex 7 K325T FPGA which is partly available for customized real-time applications. Teledyne SP Devices' ADQ14 Development Kit is an optional FPGA design project that enables custom real-time signal processing of streaming data. More details about this product can be found in the datasheet for the ADQ Development Kit.

There are ADQ14 Development Kits available for the firmware options –FWDAQ, –FWPD, and –FWSDR. Note that the ADQ14 Development Kit is individual for each firmware option and purchased separately.

TRIG and SYNC can be used as GPIO

Connector for –GPIO option

ADQ14DC–4C–VG–PXIE



GPIO for connecting to external equipment

The General Purpose Digital Input Output (GPIO) is intended for communication with external equipment. It is accessed from the software through register read and write commands. Thereby, it can be used for creating a link between the external equipment and the user's software application.

Real-time interaction with the data flow is also possible through the ADQ14 Development Kit. Here, the GPIO signals are available in the User Logic area and can be used for interacting with the data in real-time.

The standard version of ADQ14 has GPIO as a software selectable function on the trigger and sync connectors. The options –GPIO and –VG offers 12 digital bi-directional signals in addition to the standard GPIO (TRIG and SYNC). The direction and value of each pin is set individually. On the form factor option –MTCA, the dedicated GPIO port is always included.

Expansion board design kit

If the –GPIO option is not enough for the current application, an expansion board with design kit is available to create custom hardware solutions tightly connected to the FPGA on ADQ14. For details, see datasheet "15-1413 ADQ14 expansion board design kit".

Teledyne SP Devices' design service is also available for supporting custom designs. Please contact a Teledyne SP Devices' sales representative for more information.

Swept-Source OCT front panel (–OCT)

The ADQ14–SSPCIE can be equipped with at front panel adaptation for Swept-source OCT. The translation is in the table below.

Note that the external clock reference input is not available.

Note that the SYNC output is not available.

Standard	–OCT function	–OCT label
TRIG	A-SCAN	A-TR
SYNC	B-SCAN	B-TR
CHANNEL A	OCT data input	OCT
CHANNEL B	K-clock input	KCLK

17 Data interface options

ADQ14-4C-USB

Stand-alone operation with USB3.0 interface (–USB)

The SuperSpeed USB3.0 interface is intended for stand-alone operation and allows the ADQ14 to be physically integrated with the detector rather than the host PC. This means that the cable between the detector and the digitizer is kept as short as possible for optimized signal quality. The USB box includes flanges for fastening of the box and screw attachment of the USB cable.

With the USB3.0 interface, the digitizer is easily connected to any computer. The sustained data rate can be above 200 MBytes/s and combined with on-board signal processing, an efficient solution is obtained.

ADQ14DC–2X–VG–10GBE

Stand alone operation with 10 GbE (–10GBE)

The 10 GbE interface offers the same advantages as the USB3.0 interface. In addition to that the data rate is higher (1 GBytes/s), the distance to the host is longer and there is an electrical isolation from the PC. The protocol is UDP. The data transfer require a point-to-point connection. Please, note that the SFP+ optical module is not included.

ADQ14DC–4C–VG–PXIE

Modular instrumentation with cPCIe / PXIe (–PXIE)

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The ADQ14 can operate in Compact PCI Express or PXI Express chassis. Using the multi-unit sync function, multi-channels systems can be achieved.

Use streaming at up to 3.2 GBytes/s for sending data to the CPU for processing or storing at a disk.

An additional feature that comes with the PXIe form factor is that the clock reference from the backplane in the chassis can be used as clock reference for the digitizer.

ADQ14DC–2X-PCIE ADQ14DC–2X–SSPCIE

Systems integration with PCIe (–PCIE, –SSPCIE)

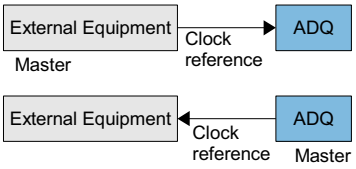
The PCIe form factor is for integration into the host PC. The board is available as half length double slot (–PCIE) or 237 mm length single slot (–SSPCIE) to suit different PC cabinets.

ADQ14DC–4C–MTCA

Large scale integration with Micro-TCA.4 (–MTCA)

The Micro-TCA.4 form factor is intended for integration into a chassis for modular instrumentation or large scale data acquisition. Note that the Micro-TCA.4 card is equipped with the –GPIO option as standard and that the gain setting option –VG is not available.

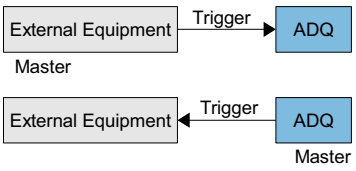
18 Synchronization support[1]



Clock reference input and output

Sharing clock reference guarantees a common time base.

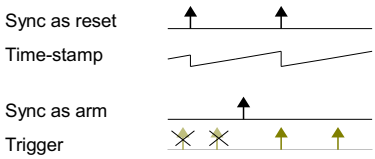
When outputting the internal clock reference, the ADQ14 can act as master. On the other hand, when the external equipment supplies the clock reference, the clock reference input can be used to achieve a common time base.



Trigger input and output

The trigger starts the operation simultaneously.

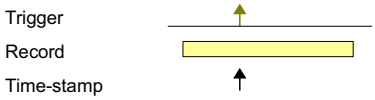
The trigger marks the start of an operation. The ADQ14 can generate a trigger to start external equipment. It can also take a trigger as input to start the acquisition.



Synchronization input and output

Extra trigger to mark beginning of a sequence.

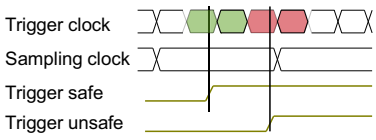
The sync pin is used for resetting the time-stamp to mark the beginning of a sequence. The sync can also be used for broadcasting an arm command to several ADQ14 units.



Time-stamp

A real-time value for each trigger.

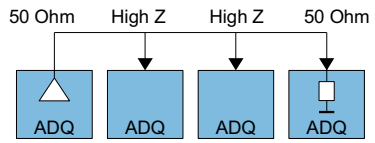
The time-stamp is a real-time value for each trigger event. It can be used for comparing timing between events from the same board or from multiple boards.



Sub-sample precision time-stamp

Automatic checking of trigger set-up and hold.

The subsample precision of the time-stamp allows for automatic analysis of trigger signal timing.



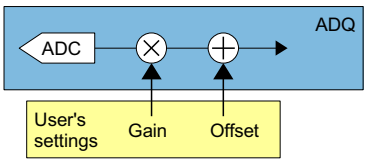
Bussed connection

Save cabling by bussed connections.

The sync, trig and clock reference can be set in high impedance mode to enable bussed connections. Note that the cable length has to be minimized to handle reflections.

1. See application note 15-1583 for more details.

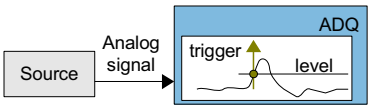
19 Built-in signal processing



Gain and offset calibration

Digital signal tuning in the FPGA.

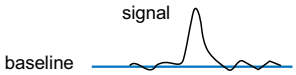
The gain and offset calibration can be used for optimizing the signal properties gain and offset in the FPGA to off-load the host computer.



Level trigger

Data driven acquisition.

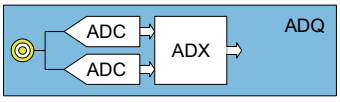
The standard firmware –FWDAQ contains a level trigger for data driven triggering and acquisition. For applications requiring advanced pulse detection and data analysis, the firmware option –FWPDis recommended.



Digital baseline stabilizer (DBS)

Enabling accurate pulse detection.

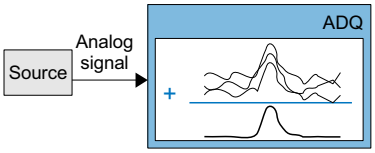
Teledyne SP Devices' proprietary technology for digital baseline stabilization (DBS), tracks baseline variations to suppress, for example, temperature drift in the detectoror power supply fluctuations. The precision is as high as 22 bits, which efficiently suppresses e.g. pattern noise in time interleaved solutions. DBS is available in options –FWDAQ, –FWPD, and –FWATD.



ADX interleaving technology

Improving wide-band spectral purity.

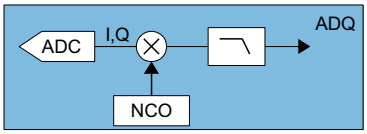
Teledyne SP Devices' proprietary interleaving technology ADX is available in the firmware option –FWSDR. ADX dynamically suppresses interleaving artifacts to produce a clean spectrum.



Waveform averaging

Data reduction in scheduled repeated measurements.

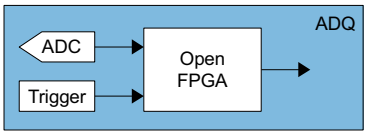
The firmware option –FWATD offers averaging of waveforms for repeated measurements.



DDC for SDR

Quadrature Mixer and decimation.

The firmware option –FWSDR is a software defined radio firmware that reduces the data rate by exclusively focusing on the actual signal band of interest. The DDC consist of a quadrature mixer, a low-pass decimation filter and sample skip.



Custom real-time processing

Efficient algorithm implementation and short time-to-market.

The ADQ14 Development Kit opens the FPGA for custom implementation of real-time algorithms. Use Teledyne SP Devices' Design Service[1] for short time-to-market.

1. Contact a Teledyne SP Devices' sales representative for more information.

20 Appendix

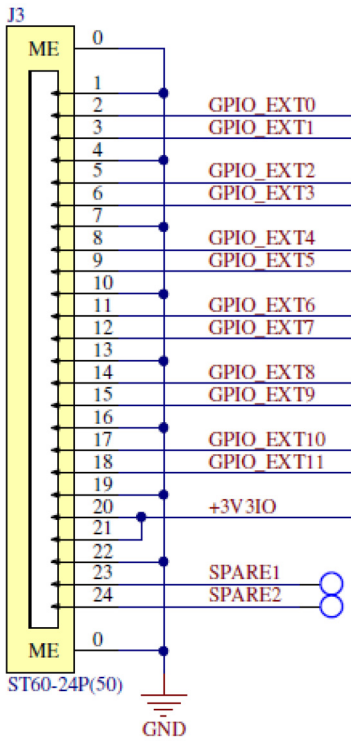
20.1 Cable attachment

All cables have a lock function so that no cable should fall out unintentionally.

FUNCTION	CONNECTOR	–USB	–PCIE	–PXIE	–MTCA	–10GBE	LOCK FUNCTION
Analog	SMA	✓	✓	✓	✓	✓	Screw
Trigger	SMA	✓	✓	✓	✓	✓	Screw
Clock ref	SMA	✓	✓	✓	✓	✓	Screw
Sync IN/ OUT	SMA	✓		✓	✓	✓	Screw
Sync IN	MCX		✓				Snap lock placed inside PC chassis
Sync OUT	MCX		✓				Snap lock placed inside PC chassis
Power	DIN	✓				✓	Snap lock
Power	Backplane			✓	✓		Screw attached board in chassis
Power	PCIe Aux		✓				Snap lock
GPIO	Hirose	✓[1]	✓[1]	✓[1]	✓	✓[1]	Snap lock
Data/control	USB3.0	✓					Screw attachment vision USB standard[2]
Data/control	Backplane		✓	✓	✓		Screw attach board in chassis
Data/control	Ethernet					✓	Snap lock of SFP+ module

1. Requires option –VG or –GPIO.
2. Optional cable solution. Not included in standard shipment.

20.2 GPIO connector for option –VG, option –GPIO, and form factor –MTCA



The 12 pin GPIO connector is available on the –VG option and on the –GPIO option. It is also available as standard on the –MTCA form factor.

There are 12 individually controlled single ended bi-directional signals available. There is also a 3.3 V power output for driving a limited load. See **Table 8** for specification.

A suitable cable is available as an accessory (order number 108-004-003)

20.3 LED definitions

COLOR	NAME	FUNCTION	STATE
Green	Power	Power on	On: Power on and FPGA is operating
Yellow	Ready	Waiting for trigger	Set up to accept trigger and waiting for the trigger
Red	Status	Overheat	Flashing means overheating or fan fault.
Blue	User	Custom	On during initialization of the board. Available for custom implementation in ADQ14 Development Kit
Red	Attention	Attention LED for PXIe	Attention LED for PXIe only

20.4 Host interface option –USB

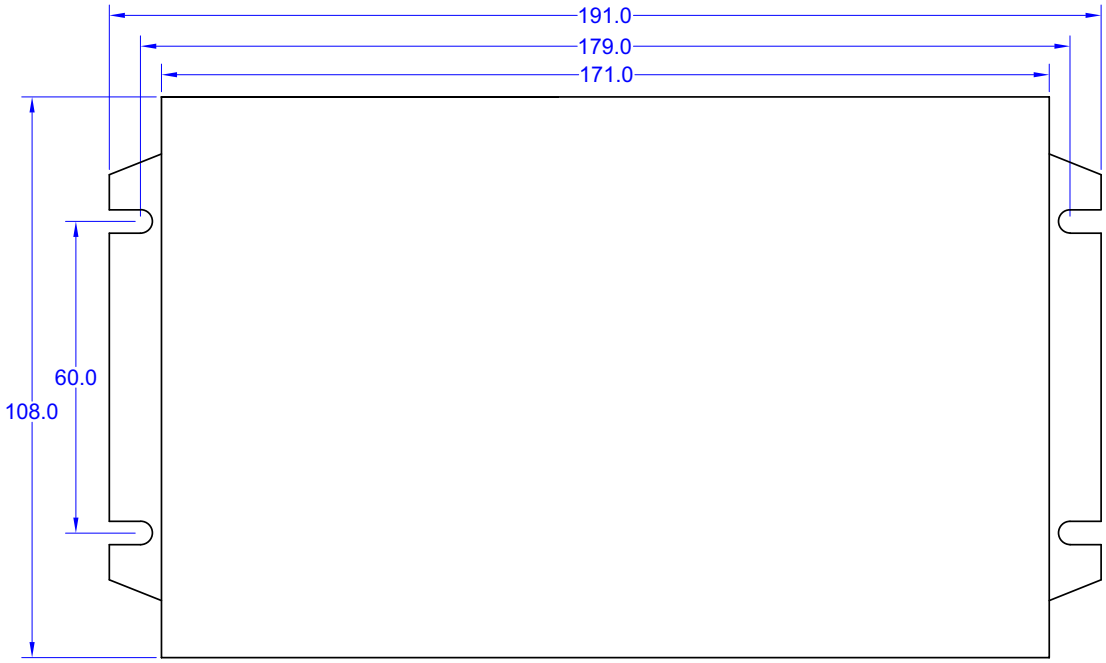


Figure 20: Fastening of USB box.

Figure 20 is a drawing of the flanges for fastening of the USB box.

The USB version is shipped wIth an external a desktop power supply. The version of power supply is depending on the end-user's location.

20.5 Host interface –10GBE

The ADQ14–10GBE is equipped with an SFP+ cage that takes and SFP+ module. The interface is tested with these modules:

- Avago AFBR-709SMZ
- Intel SFP+ E10GSFPSR

Correct operation can only be guaranteed with these modules. The modules are not included.

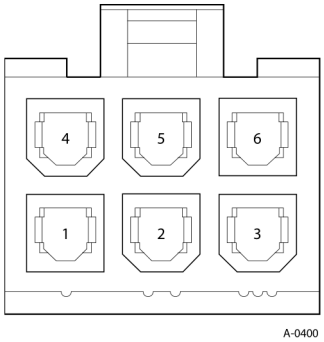
For box drawing see Figure 20 and add 40,7 mm to the length (over all length is thus 231,7 mm).

20.6 Host interface –PXIE

No additional information available.

20.7 Host interface –PCIE

The ADQ14–PCIE is powered from the power supply of the PC via a PCI Express 6-pin (2x3) auxiliary 75W power supply connector, **Figure 22**. The connection in the cable should be as in **Figure 21**. It is important that the axillary power supply is turned on immediately when the PC start. Otherwise, the digitizer will not be recognized on the PCI Express bus.



(a) Cable connection

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

(b) Pin-out table

Figure 21: Power supply of –PCIE

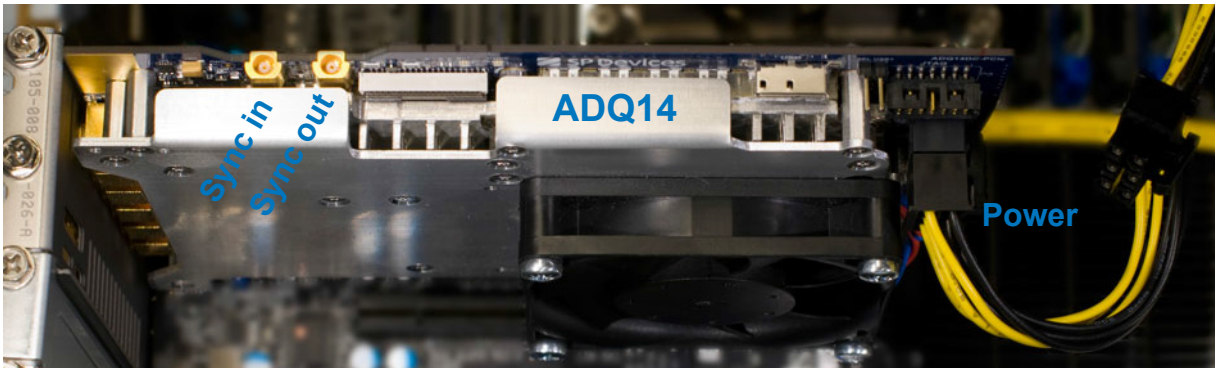


Figure 22: ADQ14 installed in a PC.

20.8 Micro-TCA backplane connectors

PORT	FUNCTION	SIGNALING	ADQ14–MTCA AVAILABILITY
0, 1	1 GbE	N/A	N/A
2, 3	SAS/SATA	N/A	N/A
4, 5, 6, 7	PCIe	PCIe Gen2 x4	Main data and control interface.
8, 9, 10, 11	SRIO	N/A	N/A
12, 13, 14, 15	P-t-P	High speed serial	Available through ADQ14 Development Kit only[1].
16	TCLKC/D	N/A	N/A
17, 18, 19, 20	Tr/clk/int	LVDS	Available through ADQ14 Development Kit only[1].
Clk 1	TCLKA	LVPECL	Clock reference selected from API.
Clk 2	TCLKB	LVPECL	Clock reference selected from API.
Clk 3	FCLKA	PCIe clock	PCIe interface reference clock.

1. There is no function defined in the standard firmware. The electrical signals are available for inclusion in custom firmware in the FPGA. The custom firmware is designed using the ADQ14 Development Kit.

Ordering information

ORDERING INFORMATION	
ADQ14 AC-coupled	ADQ14AC
ADQ14 DC-coupled	ADQ14DC
AVAILABLE OPTIONS	
Host PC interface	–USB, –PCIE, –SSPCIE, –PXIE, –MTCA, –10GBE
Analog front-end options	–2A, –2C, –1X, –4A,–4C, –2X, –VG
Firmware options	–FWDAQ, –FWATD, –FWPD, –FWSDR
GPIO option	–GPIO
Front panel option	–OCT
USB Power supply for US	–PWRUS
USB Power supply for EU	–PWREU
Warranty extension to 5 years[1]	–W5Y
RELATED PRODUCTS	
ADQ14 Development Kit for –FWDAQ	ADQ14 Development Kit –FWDAQ
ADQ14 Development Kit for –FWPD	ADQ14 Development Kit –FWPD
ADQ14 Development Kit for –FWSDR	ADQ14 Development Kit –FWSDR
ADQ14 expansion board kit	ADQ14 –EXPANSION
ADQ14–GPIO cable assembly, 1m, 2 connectors	108-004-003
USB3.0 cable with screw lock	108-002-006

1. Warranty extension must be ordered before included 3 years warranty is expired.

References

15-1593 ADQ14 manual

14-1397 ADQ14-FWATD datasheet

15-1455 ADQ14-FWPD datasheet

15-1469 ADQ14-FWSDR datasheet

15-1413 ADQ14 Expansion module design kit

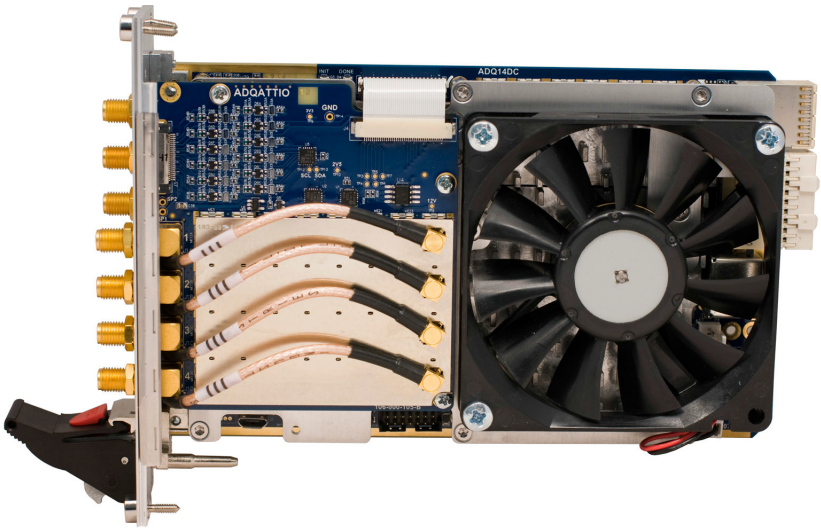
15-1583 ADQ14 synchronizing several units application note

14-1351 ADQAPI reference guide

20-2381 Digitzer Studio Datasheet

20-2382 Digitzer Studio User Guide

20-2465 Streaming



Important Information

Teledyne Signal Processing Devices Sweden AB (Teledyne SP Devices) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Teledyne SP Devices' general terms and conditions supplied at the time of order acknowledgment.

Teledyne SP Devices warrants that each product will be free of defects in materials and workmanship, and conform to specifications set forth in published data sheets, for a period of three (3) years. The warranty commences on the date the product is shipped by Teledyne SP Devices. Teledyne SP Devices' sole liability and responsibility under this warranty is to repair or replace any product which is returned to it by Buyer and which Teledyne SP Devices determines does not conform to the warranty. Product returned to Teledyne SP Devices for warranty service will be shipped to Teledyne SP Devices at Buyer's expense and will be returned to Buyer at Teledyne SP Devices' expense. Teledyne SP Devices will have no obligation under this warranty for any products which (i) has been improperly installed; (ii) has been used other than as recommended in Teledyne SP Devices' installation or operation instructions or specifications; or (iii) has been repaired, altered or modified by entities other than Teledyne SP Devices. The warranty of replacement products shall terminate with the warranty of the product. Buyer shall not return any products for any reason without the prior written authorization of Teledyne SP Devices.

In no event shall Teledyne SP Devices be liable for any damages arising out of or related to this document or the information contained in it.

TELEDYNE SP DEVICES' EXPRESS WARRANTY TO BUYER CONSTITUTES TELEDYNE SP DEVICES' SOLE LIABILITY AND THE BUYER'S SOLE REMEDY WITH RESPECT TO THE PRODUCTS AND IS IN LIEU OF ALL OTHER WARRANTIES, LIABILITIES AND REMEDIES. EXCEPT AS THUS PROVIDED, TELEDYNE SP DEVICES DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT.

TELEDYNE SP DEVICES DOES NOT INDEMNIFY, NOR HOLD THE BUYER HARMLESS, AGAINST ANY LIABILITIES, LOSSES, DAMAGES AND EXPENSES (INCLUDING ATTORNEY'S FEES) RELATING TO ANY CLAIMS WHATSOEVER. IN NO EVENT SHALL TELEDYNE SP DEVICES BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFIT, LOST DATA AND THE LIKE, DUE TO ANY CAUSE WHATSOEVER. NO SUIT OR ACTION SHALL BE BROUGHT AGAINST TELEDYNE SP DEVICES MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS ACCRUED. IN NO EVENT SHALL THE ACCRUED TOTAL LIABILITY OF TELEDYNE SP DEVICES FROM ANY LAWSUIT, CLAIM, WARRANTY OR INDEMNITY EXCEED THE AGGREGATE SUM PAID TO SP BY BUYER UNDER THE ORDER THAT GIVES RISE TO SUCH LAWSUIT, CLAIM, WARRANTY OR INDEMNITY.

Worldwide Sales and Technical Support

www.spdevices.com

Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com