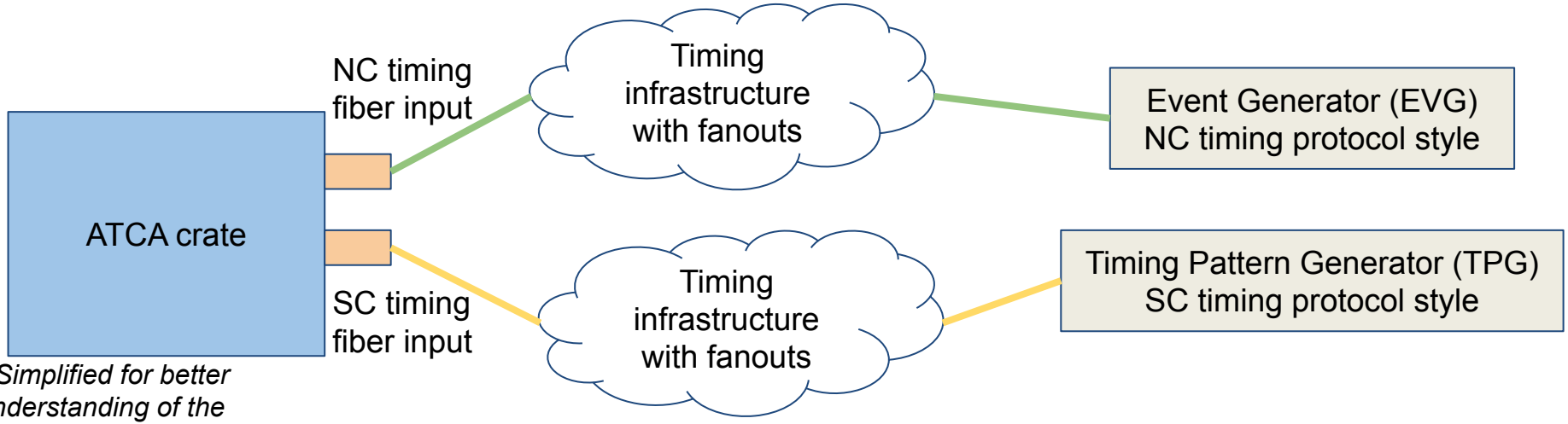
Timing

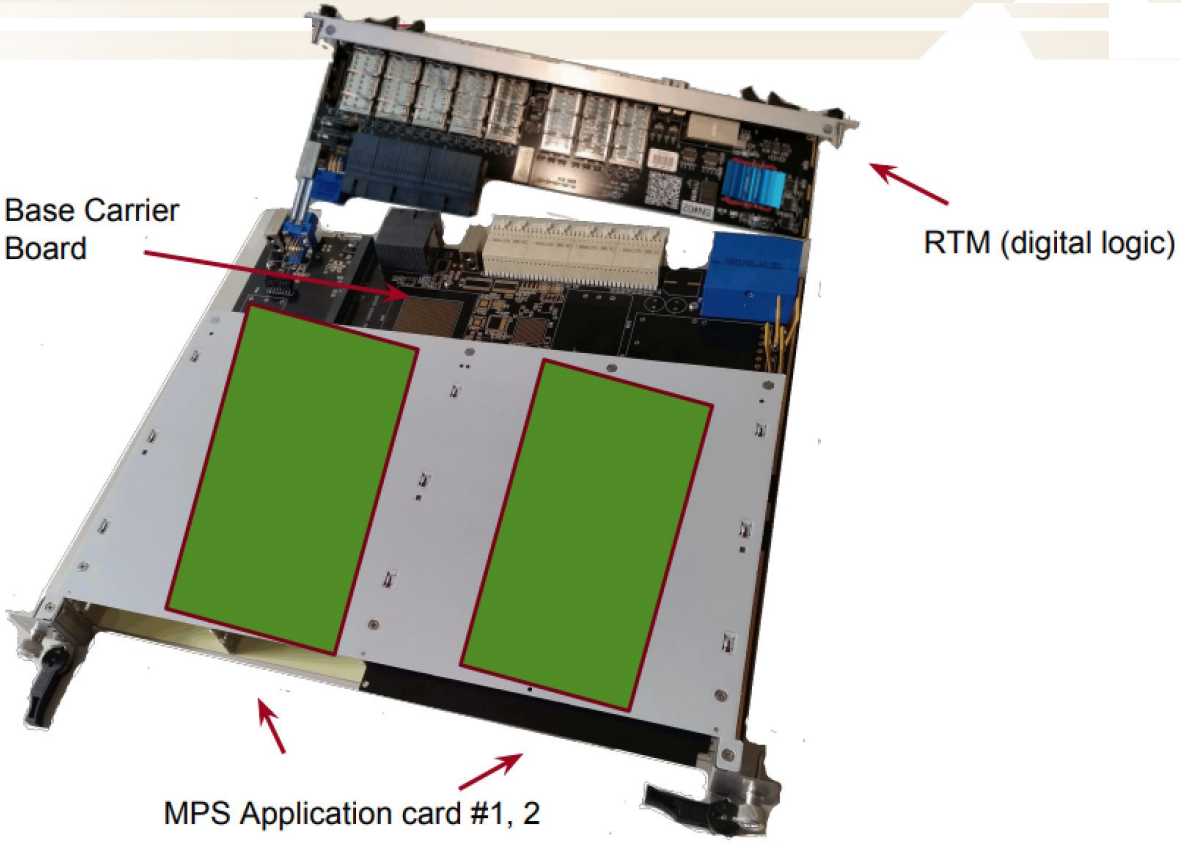


** Simplified for better understanding of the concepts. This diagram will be completed next.*

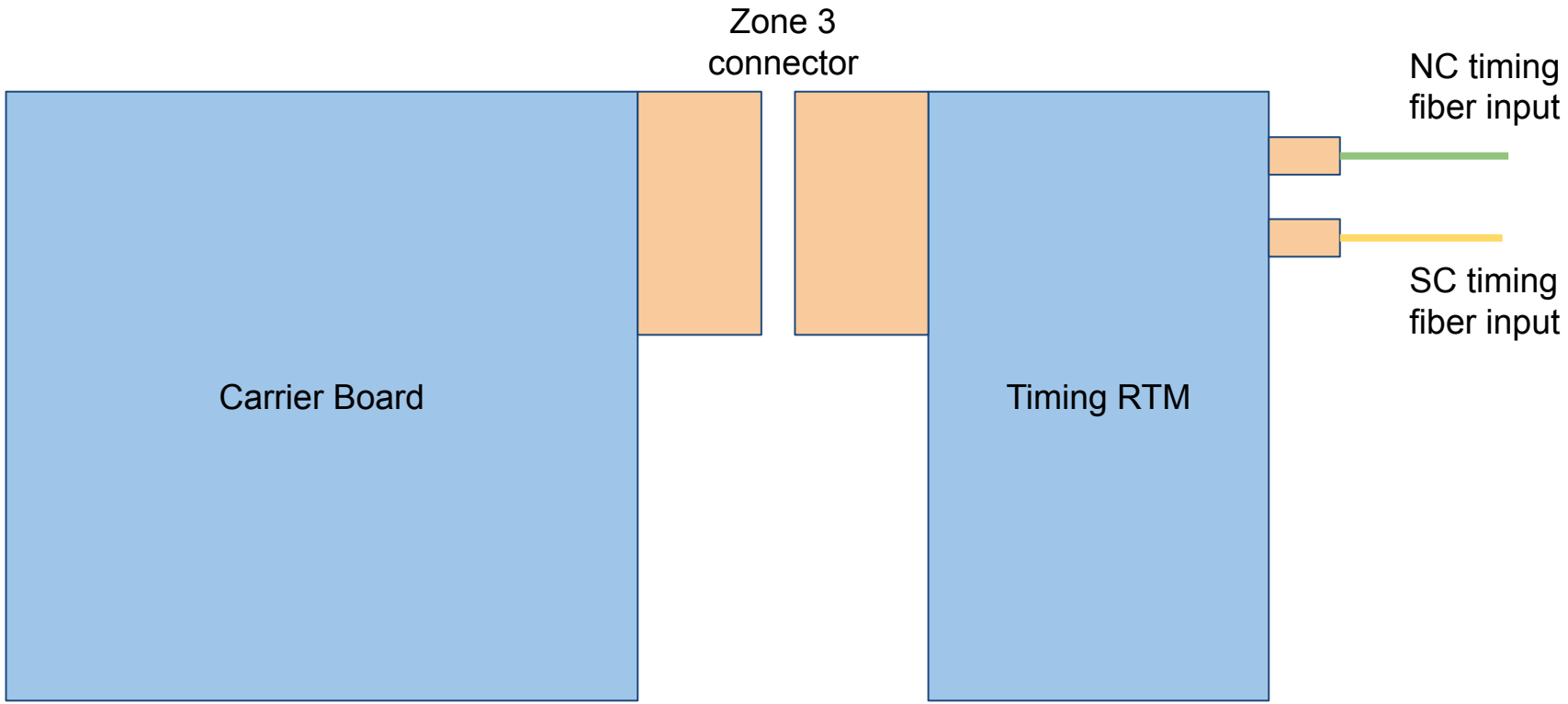
Most Used MPS/Timing RTM

MPS/Timing Rear Transition Module

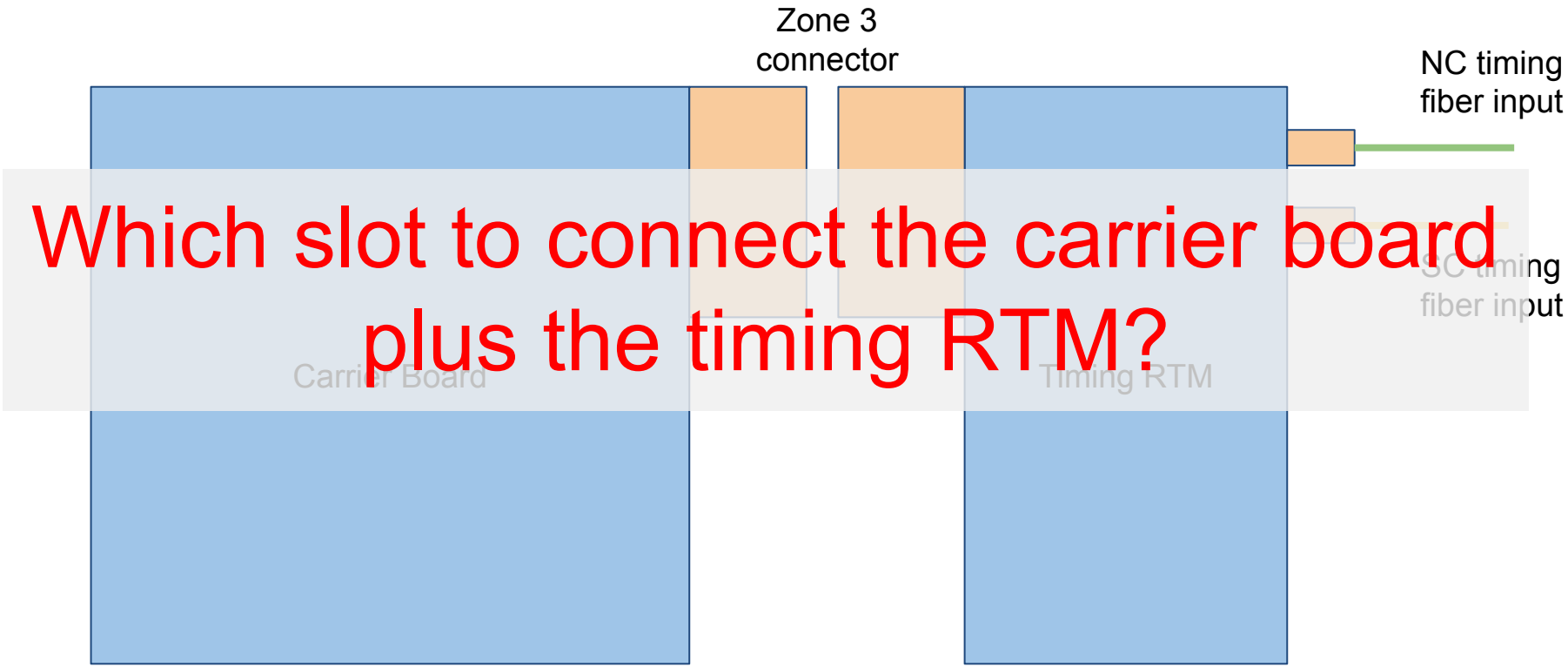
Most Used MPS/Timing RTM



Timing


Zone 3
connector
NC timing
fiber input
SC timing
fiber input
Carrier Board
Timing RTM

Timing

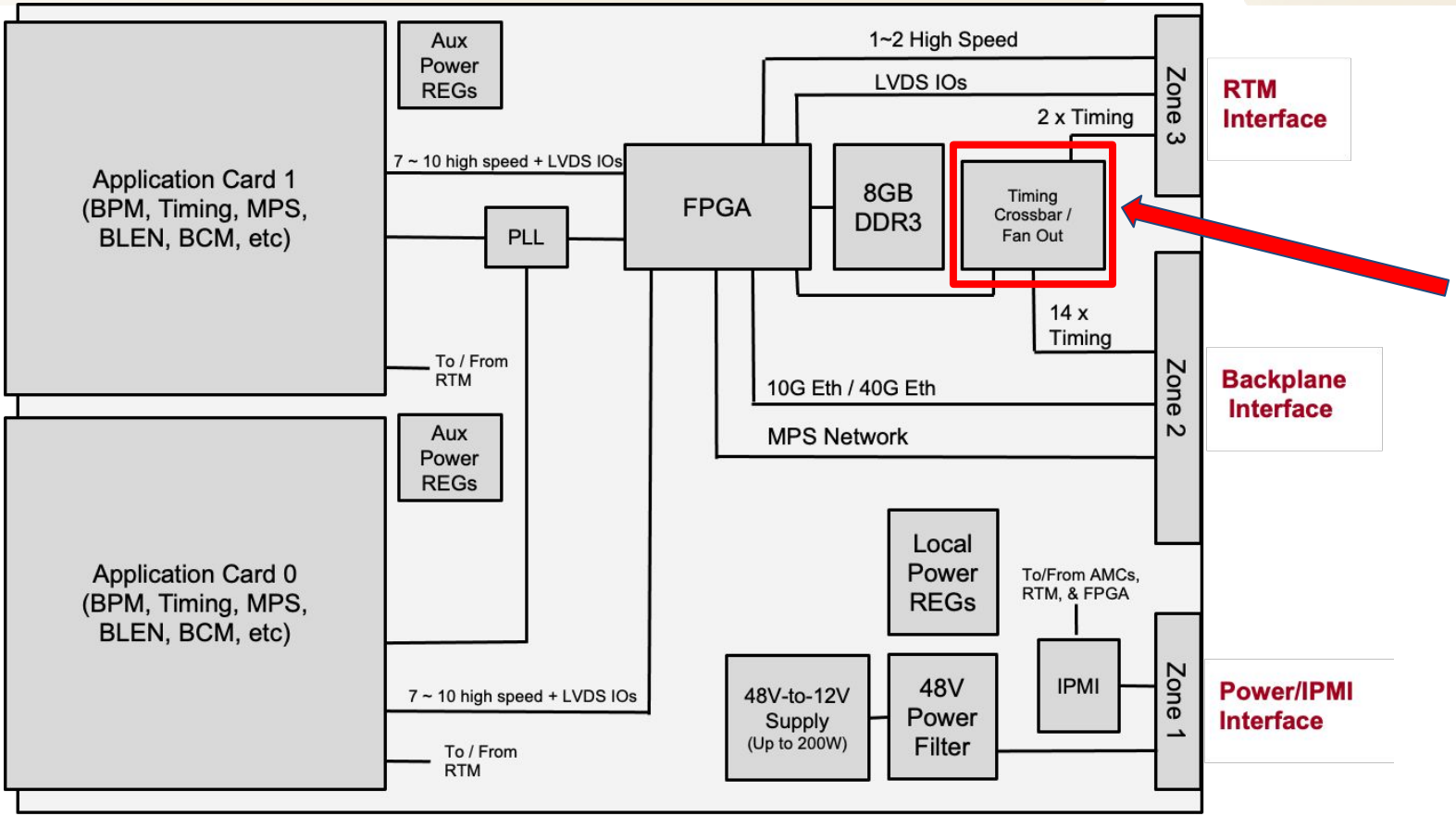


Which slot to connect the carrier board plus the timing RTM?

Timing

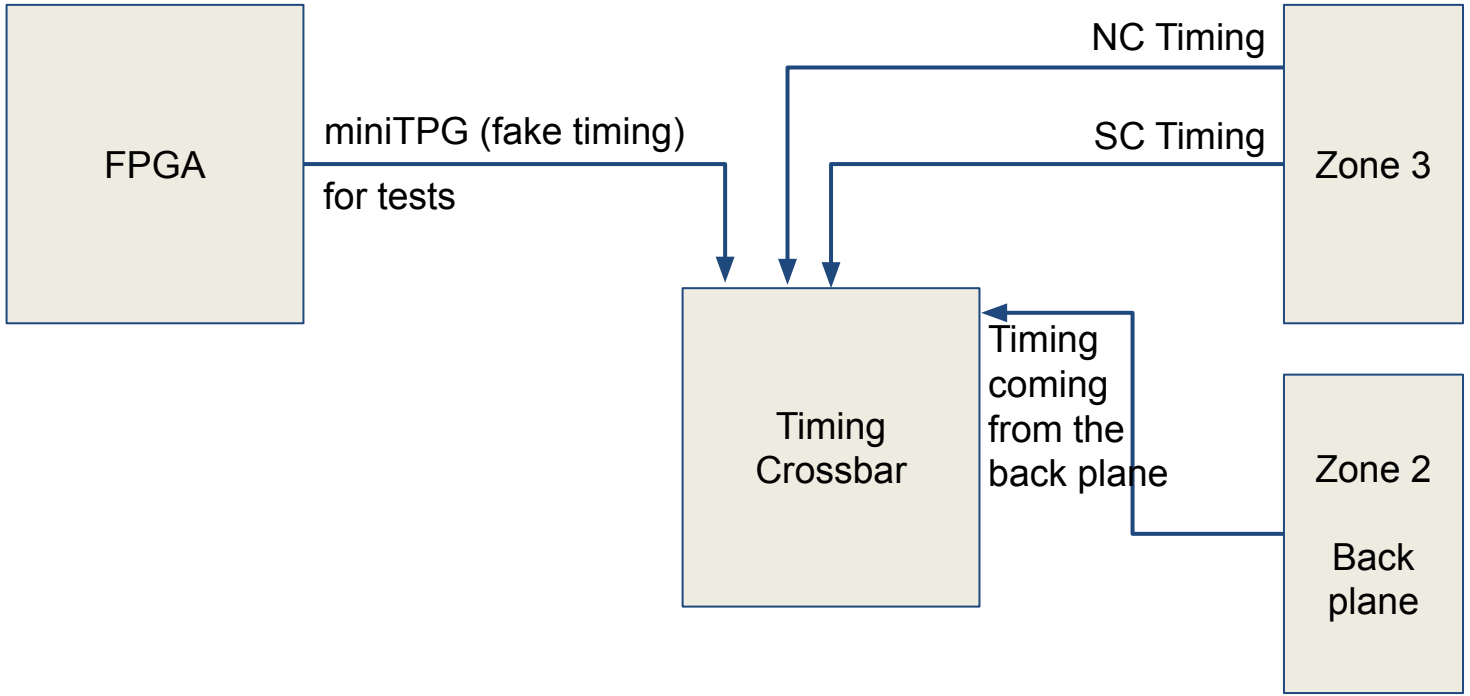
- Timing data must be consumed by all carrier boards.
- Ideally we should use one single RTM to receive timing as opposed to connecting timing RTMs to each slot.
  - Saves money in RTM boards and fibers.
  - Make space for application specific RTMs.
- As seen, only slots 1 and 2 are connected to all other slots.
- Slot 1 is already reserved to the Ethernet switch.
- So, the only way is to connect the timing RTM to the carrier board at slot 2.

AMC Carrier Board



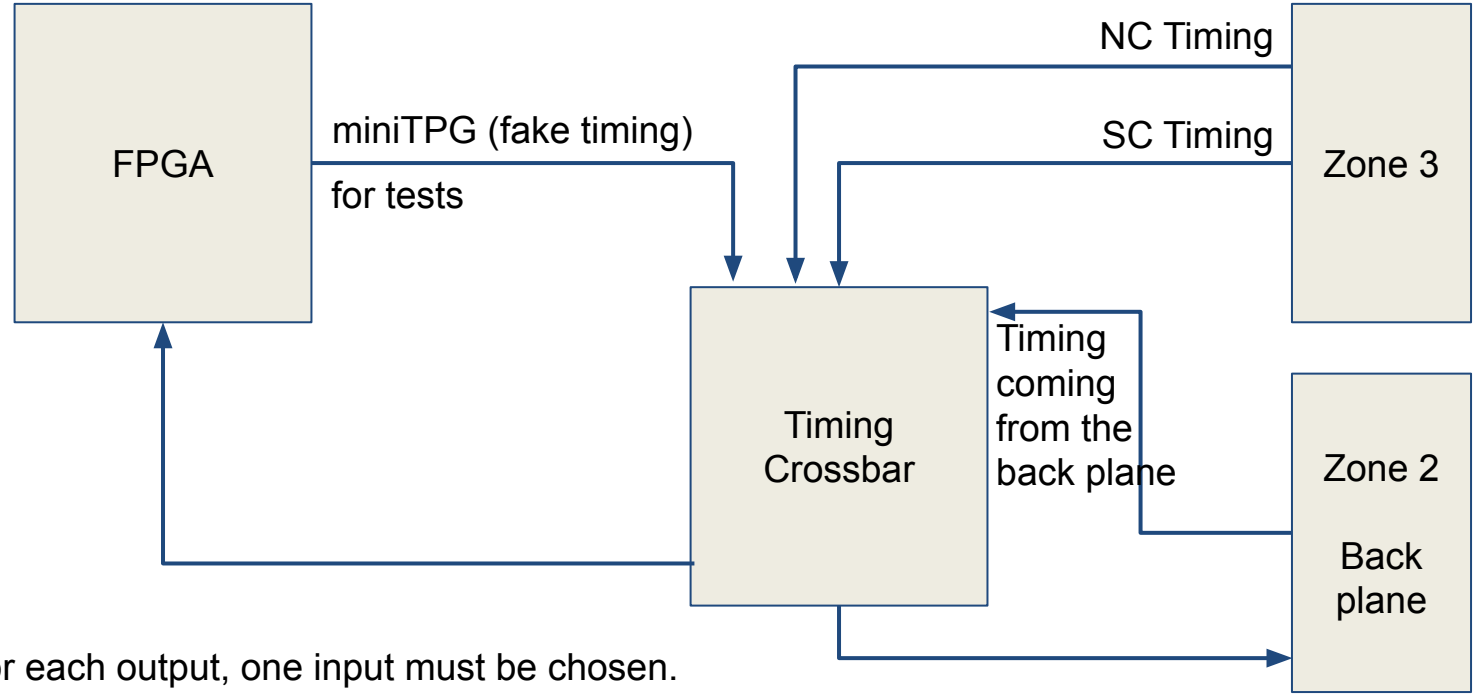
Timing Crossbar

4 sources of input



Timing Crossbar

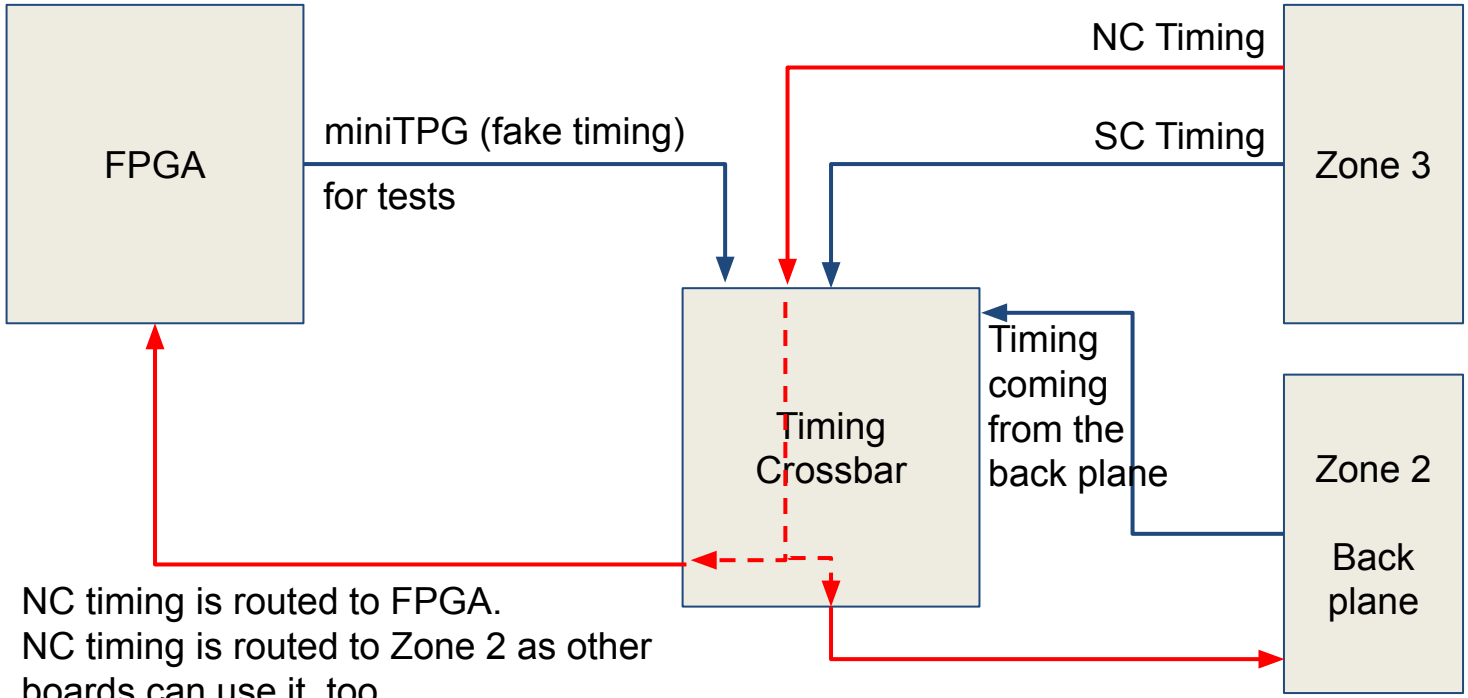
There are 4 sources of output, but only 2 are used in fact. (the other 2 go back to zone 3)



For each output, one input must be chosen.

Timing Crossbar

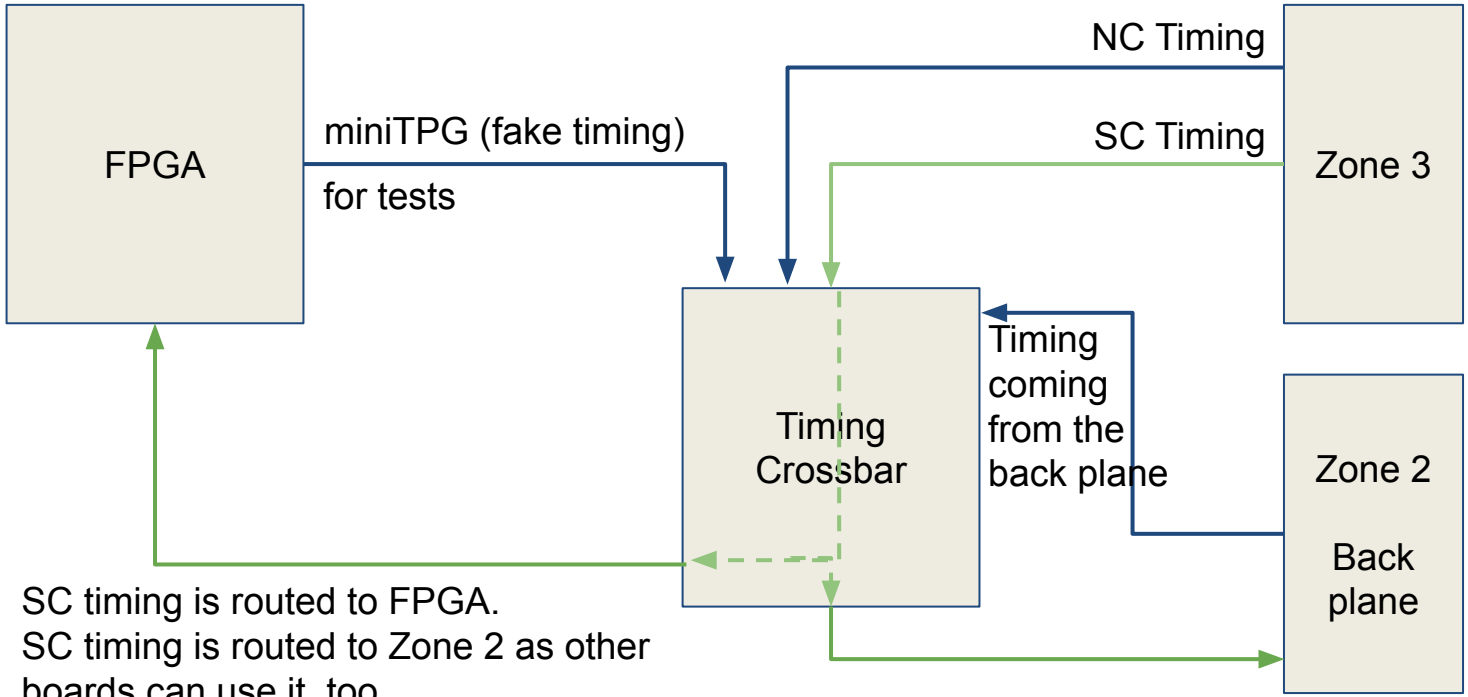
Configuration for carrier in slot 2 using NC timing



1. NC timing is routed to FPGA.
2. NC timing is routed to Zone 2 as other boards can use it, too

Timing Crossbar

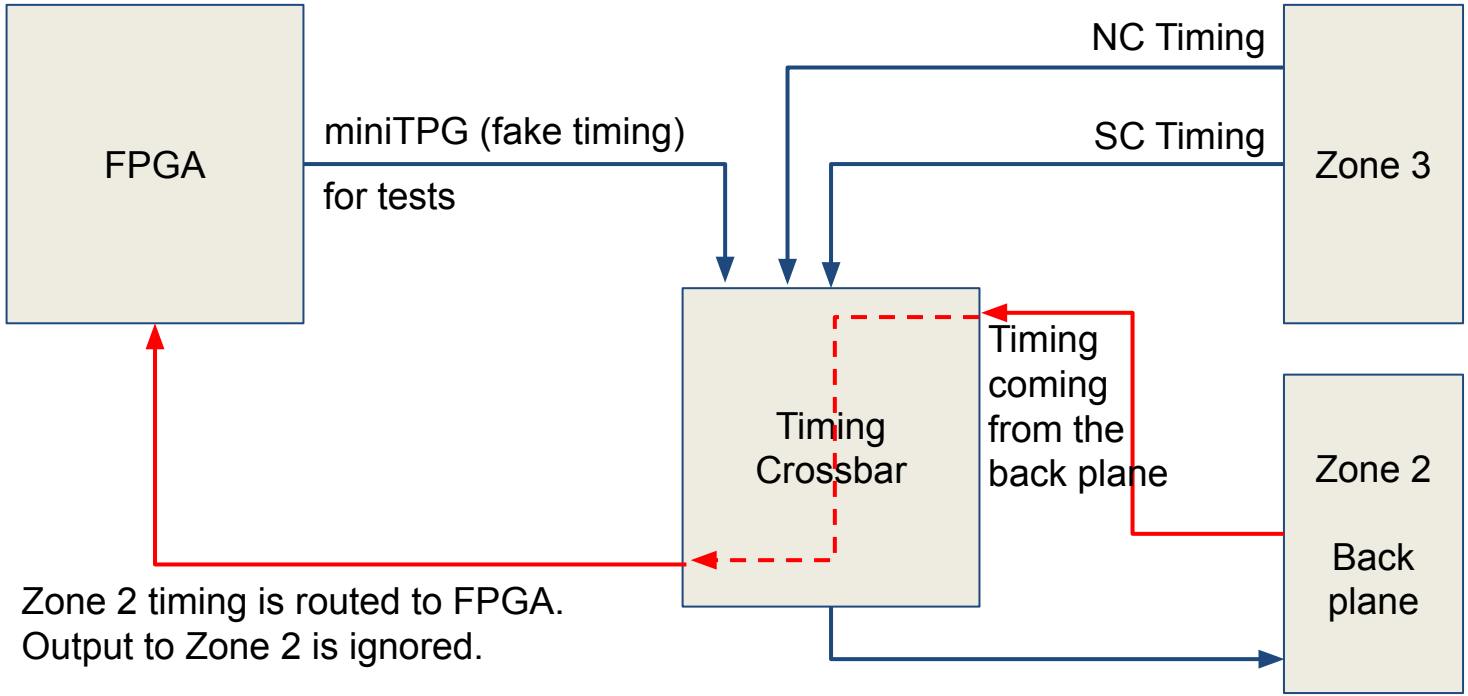
Configuration for carrier in slot 2 using SC timing



1. SC timing is routed to FPGA.
2. SC timing is routed to Zone 2 as other boards can use it, too

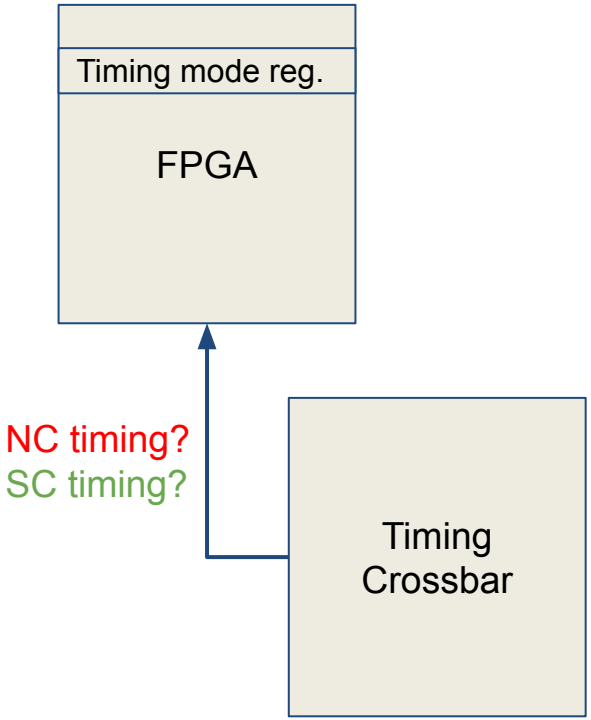
Timing Crossbar

Configuration for carrier in other slots



1. Zone 2 timing is routed to FPGA.
2. Output to Zone 2 is ignored.

Timing Crossbar



The timing mode is not auto-discovered by the FPGA. There is a register that needs to be set to make the firmware to interpret the protocol correctly.

When changing the timing mode, a few actions are needed:

1. Change timing mode register in the FPGA of all carrier boards installed.
2. Slot 2 crossbar must be set to route the correct timing mode to its own FPGA.
3. Slot 2 crossbar must be set to route the correct timing mode to Zone 2 as the other boards can receive them from the back plane.